TSB41BA3/A Errata

1 S100B Failed Connection Issue

1.1 Description

An S100B port of a TSB41BA3/A sometimes fails to make an active connection to an S100B port of another TSB41BA3/A after power up. The other ports on the TSB41BA3/A devices have active, functioning connections. The failed connection can occur across a CAT5 cable with TSB17BA1s and magnetics installed or it can occur on direct connections between two TSB41BA3/A devices.

Reading the registers of the TSB41BA3/As on either side of the failed connection reveals that both devices mark the failed connection with Loop_disable set in the page-0 port status register at Dh. A loop is not present in the system. A bus reset or series of bus resets does not re-enable the connection. A hard reset of one or both TSB41BA3/A devices may re-enable the connection in some cases.

It should be noted that once an active connection is made between two TSB41BA3/A devices, the connection is never dropped during normal operation or after a bus reset or even a hard reset due to this issue.

1.2 Cause

The S100B port transmit clock circuitry is not properly reset at power up, occasionally allowing the clock to initialize into an invalid state, thereby generating an incorrect frequency for S100B connections.

1.3 Workarounds

This issue will be fixed in an upcoming release of the TSB41BA3/A device: the TSB41BA3B. In the interim, there are some workaround possibilities:

1.3.1 Software Workaround

1. Set the TSB41BA3A mode so that all S100B connections are now set as S400B. For example, a mode-4 device would become a mode-6 device and a mode-12 device would become a mode-14 device. For this workaround, the mode change is permanent.
2. At power up, use the CSEL bit, which is located in the page-7 register, to force both PLLs on. This step must occur before any port connections are made, within ~600 ms of power up.
3. Set Max_Port_Speed to S100B for CAT5 ports. This step must be repeated after every hard reset.
4. As long as the preceding step is performed before the port connection is made (within ~600 ms of power up), no disabling/re-enabling of the ports is necessary.

1.3.2 Software/Hardware Workaround

1. Set the TSB41BA3A mode so that all S100B connections are set as S400B. For example, a mode-4 device would become a mode-6 device and a mode-12 device would become a mode-14 device.
2. At power up, use the CSEL bit, which is located in the page-7 register, to force both PLLs on. This step must occur before any port connections are made (within ~600 ms of power up).
3. Set the TSB41BA3A mode back to S100B.
4. Generate a hard reset via $\overline{\text{RESET}}$.

1.3.3 Hardware Workaround

This workaround is for active S100B ports only. It does not work for ports connected after power up.

1. Set the TSB41BA3A mode so that all S100B connections are now set as S400B. For example, a mode-4 device would become a mode-6 device, and a mode-12 device would become a mode-14 device.
2. Wait ~1 second to allow the active connections to fail (speed negotiation and training must complete). This requires both sides of the CAT5 connection to be configured to S400B to force the system to attempt to transmit at S400B.
3. Set the TSB41BA3A mode back to S100B in hardware.
4. Generate a hard reset via $\overline{\text{RESET}}$.

2 Disappearing IDLE in a Beta system Issue

2.1 Description

Disappearing IDLE in a Beta system results in max arbitration state timeout and bus reset. Specifically in Beta systems with more than four cable hops, unwanted bus resets may occur.

2.2 Cause

A short IDLE between a data packet and an arbitration grant disappears.

As signals propagate across the 1394 network, the IDLE between a data packet and an arbitration grant shortens since the time needed to repeat a data packet is longer than the time needed to repeat a grant.

2.3 Workaround

Add a 1394A PHY to the system to force legacy gap timing on the 1394 bus.

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