APPLYING THE UCC3570 VOLTAGE-MODE PWM CONTROLLER TO BOTH OFF-LINE AND DC/DC CONVERTER DESIGNS

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Abstract

BiCMOS processing provides the key to a new integrated PWM controller which offers higher switching frequencies at lower quiescent current drain while including new innovations in both performance and protection features. Its versatility is demonstrated with the description of a 50W, wide input voltage range, off-line inverter and a 48-to-5V isolated DC/DC converter, both of which feature efficiencies in the range of 80 percent.

INTRODUCTION

Over the years, our industry continues to see a steady evolution in power control technologies as new circuit topologies offer performance improvements over those achievable with older designs. For instance, current-mode control has become today's dominant control algorithm as its introduction brought such benefits as:

- Instant response to line variation
- Inherent pulse-by-pulse current limiting
- Faster loop response

These characteristics were quite significant when compared to the voltage-mode circuits built with the technology of the early 1980's when current-mode IC's were first introduced. However, both circuit design and IC process developments during the intervening years have shown that these capabilities are not necessarily limited to current-mode control. And along with the benefits of current-mode control have come several difficulties which have notably complicated the power supply designer's tasks. Among these are:

- Dealing with the current waveform's leading-edge spike
- Eliminating the effects of ringing or other noise sources
- Adding the appropriate amount of slope compensation
- Analyzing circuit performance with two feedback loops
- Providing good regulation with multiple outputs
- Stabilizing PWM operation with low amplitude ramp waveforms

Although solutions can and have been found for all the above issues, these difficulties have inspired a re-evaluation of voltage-mode control in the light of today's technology. In particular, it seemed desirable to incorporate some newer circuit concepts - such as voltage feed-forward, programmable duty-cycle limiting, and sophisticated fault protection - into a design which could also benefit from low-current BiCMOS processing. These circuit and process innovations have resulted in a new IC controller equally at home in wide voltage range off-line inverters and highly efficient isolated DC/DC converters.

INTRODUCING THE UCC3570

The overall block diagram for the UCC3570 is shown in Figure 1. While this architecture may look relatively complex, it is not because of the pulse-width modulation circuitry. Although this may be the heart of the controller, it is implemented with only the comparator, OR-gate, latch, and output driver shown across the center of the diagram. Since the UCC3570 is intended for isolated applications, there is no error amplifier, anticipating that this function will be on the opposite side of the isolation boundary.

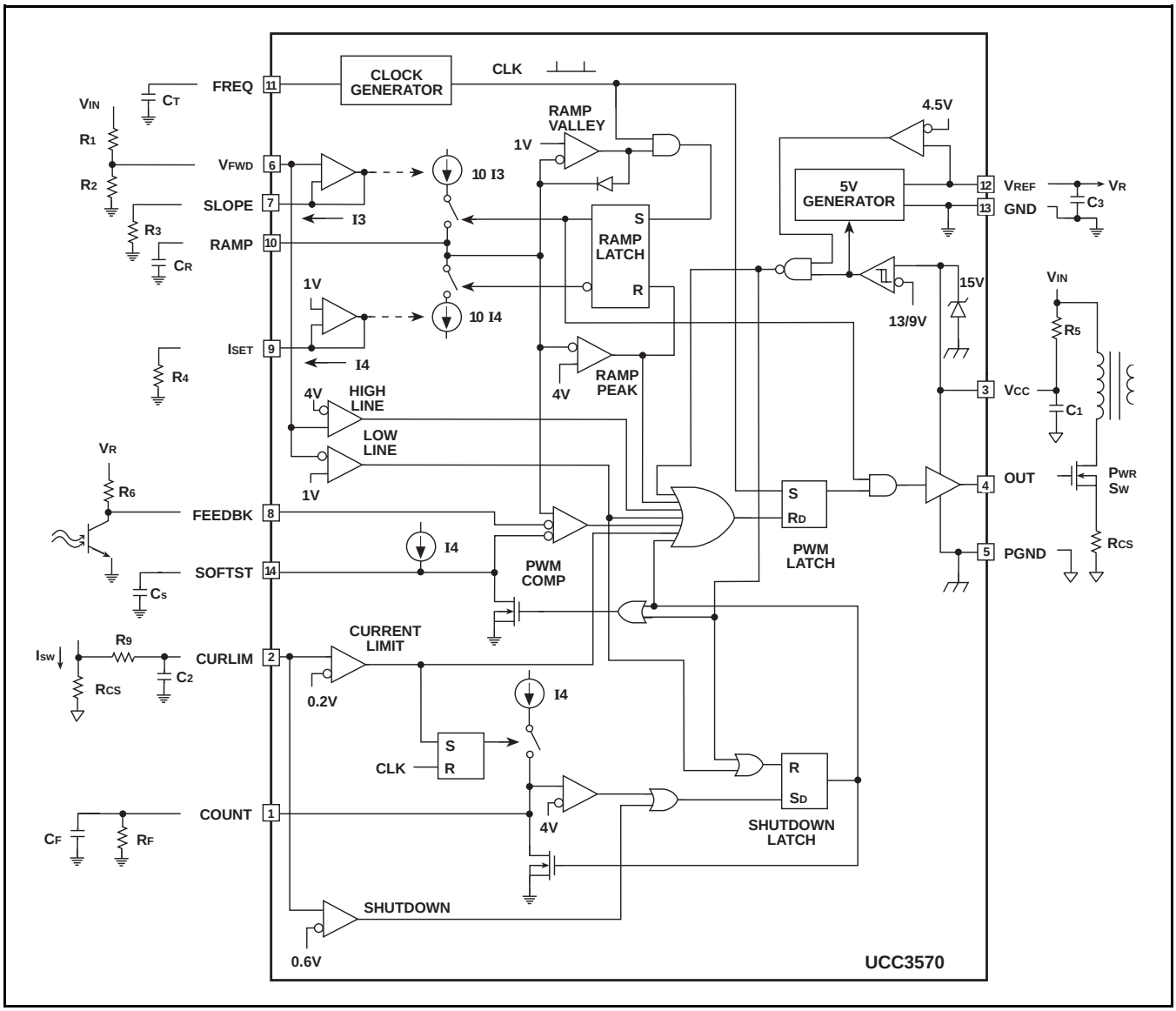

Figure 1. The overall block diagram of the UCC3570 showing connections to typical external components.

The emphasis given to programming and protection is indicated by the multiple-input OR-gate in the PWM path. This gate will terminate or prevent an output pulse if any of its inputs are high. The input signals to this gate are derived from the remainder of the circuitry. These other circuits can be divided into three sections which are described below: Ramp generation, Power sequencing, and Fault protection.

RAMP GENERATION CIRCUITRY

An important circuit feature incorporated into the design of the UCC3570 is a unique PWM ramp generator which combines voltage feed-forward, duty-cycle clamping, and fixed frequency operation. While all of these characteristics have individually been used before, combining them into a control which will automatically and linearly provide an open-loop PWM correction for large input voltage variations, and allow a maximum duty-cycle clamp to be user-set over a 20%-to-80% range, while maintaining constant switching frequency, was a challenge met with the circuitry shown separately in Figure 2.

The ramp voltage waveform is formed by charging an external capacitor with a current source made proportional to the input line voltage, and discharging it with a programmable current sink which determines the minimum deadtime. Switching between the charging and discharging currents is commanded by a flip-flop which is set with a constant-frequency clock signal, and reset when the ramp reaches four volts. To insure constant ramp amplitude, the bottom of the ramp is held at one volt while awaiting the clock command to start the next charge cycle. If the ramp discharge has not returned to one volt at the end of the period, the clock is blocked, forcing the circuit to wait through the next period before charging again by accepting the following clock signal.

These relationships are shown in Figure 3 which compares the ramp waveform with three different levels of input voltage.

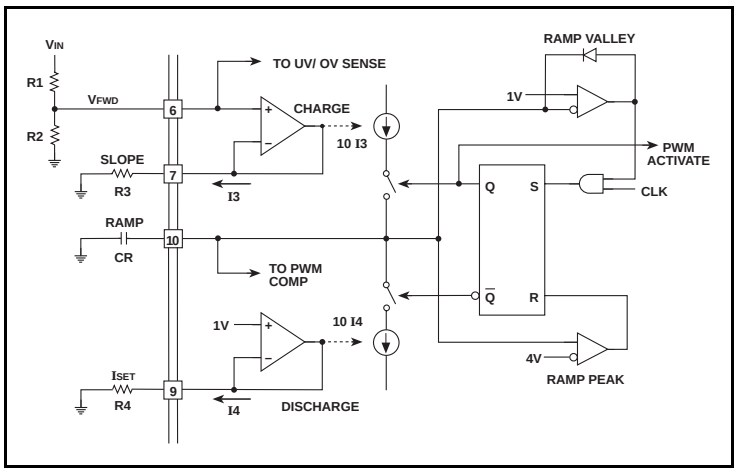

Figure 2. The ramp generation portion of the UCC3570 with independent rise-time, fall-time, and frequency control.

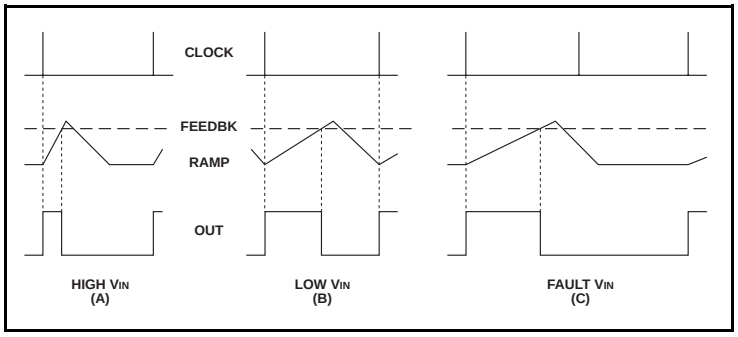

Figure 3. Effects of line voltage on the ramp waveform showing a variable slope rise, constant fall, and guaranteed minimum off-time.

PROGRAMMING AND PROTECTION

The power sequencing features of the UCC3570 are highly optimized for off-line operation beginning with the fact that the BiCMOS process yields very low operating currents for this device - one milliamp to run and less than 100 microamps prior to starting. In addition, there are two pins which sense the line voltage and provide turn-on/turn-off functions. VCC provides chip power and has a UVLO circuit which sets turn-on at 13 volts with a 4-volt hysteresis. VFWD is primarily intended to provide voltage feed-forward by adjusting the ramp slope, but this pin is also monitored by over and under-voltage sensing comparators which terminate output pulses if the line voltage is outside its defined operating range. Because VCC will normally require an energy storage capacitor, it will respond more slowly than VFWD and since both must be above a minimum for operation, turn-on will typically be initiated by VCC while a collapsing voltage on VFWD will provide a faster turn-off. Turn-on is further controlled by a Soft-Start circuit which minimizes both starting currents and output voltage overshoot.

Another valuable circuit feature is an over-current fault protection technique which provides fast pulse-by-pulse current limiting with the ability to accept a definable period of over-current operation and then shut the system down if the fault is continuous. Referring again to Figure 1, the Current Limit pin is shown monitored by two comparators with thresholds of 0.2 and 0.6 volts. (It might be noted that noise filtering here has no impact on the feedback control loop as it would with current-mode control.) When the 0.2V threshold is exceeded, the output is commanded off within 100nsec. In addition, each time this occurs, an increment of charge is added to the capacitor on the COUNT pin and should the voltage on this pin rise to 4V, a Shutdown Latch is activated. This latch is also triggered immediately if the current limit signal crosses the 0.6V threshold. Reset of the Shutdown Latch occurs when either VCC or VFWD falls below its lower threshold which allow a variety of options for either manual or automatic restart but, in either case, reset initiates a normal soft-start.

WARNING

Off-line AC power supplies are intrinsically hazardous!!!

The power supply described herein contains dangerous voltages!

Never allow human contact with any part of the input circuitry of any power supply, including the input ground connections, if it is not connected through an isolation transformer, whether the supply is turned on or off.

The supply described herein uses and can produce voltages which are potentially lethal! It should be serviced or tested only by experienced, qualified personnel, with proper techniques and equipment!

WARNING

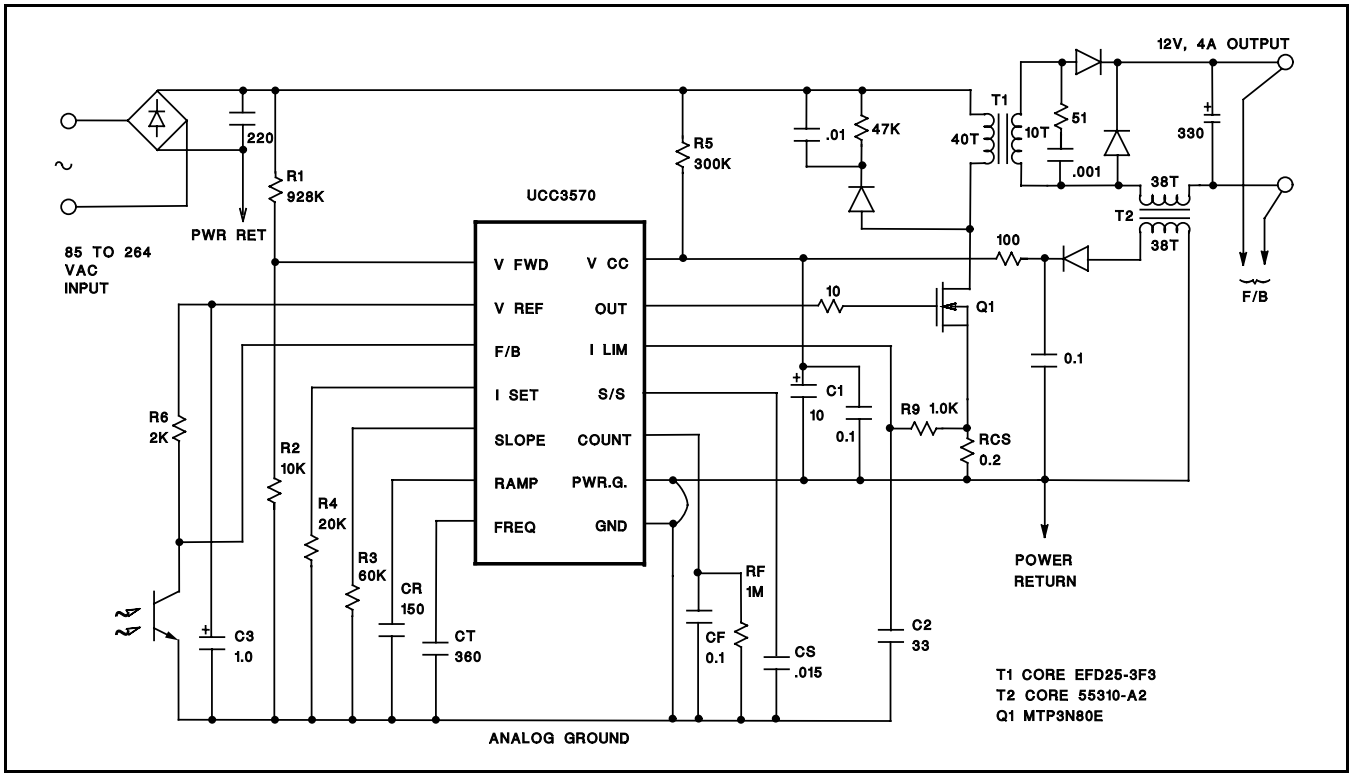

Figure 4. A simplified schematic for a 50 Watt, off-line power converter with full fault protection applicable to worldwide line voltages.

AN OFF-LINE APPLICATION

The 50 Watt off-line supply shown in Figure 4 is presented to illustrate a typical use for this controller. This application is intended for highly cost-sensitive markets requiring operation over world-wide line voltages. Its forward topology provides good regulation with low output ripple and it takes advantage of the low current requirement of the UCC3570 to allow simple interfacing to the high voltage line with minimal power loss. The switching frequency is 225kHz with the allowable duty-cycle range set to a maximum of 67% - a value which keeps the peak switch current low while still insuring a finite reset time for the transformer. The design steps which follow, while perhaps less rigorous than some might wish, should still provide a check list of items for the designer to consider when applying the UCC3570, regardless of the specific application.

TRANSFORMER RESET

In any single-ended power stage design, the plan for transformer reset is one of the first design decisions needed. In providing a power pulse to the output, the transformer is driven in one polarity for a finite number of volt-seconds. To prevent saturation, the same number of volt-seconds must be provided in the opposite polarity between the termination of one power pulse and the beginning of the next one. Since it is the volt-second product which must be met, many compromises can be made between the amount of reset voltage allowed and the time allocated. The UCC3570 simplifies this analysis to the extent that the worst case situation will always be at the lowest operating voltage. This is because, when properly set up, the voltage feed-forward feature will automatically increase the minimum off-time as the input voltage increases.

While most single-ended converters allocate 50% of the switching period for transformer reset, in the interests of allowing a lower peak input current, the maximum duty-cycle for this application was extended to 67%, allowing only one-third of the period for reset. This precluded using a reset winding on the power transformer with a 1-to-1 turns ratio. While a higher turns ratio could have been used, that would have offered the choice of either recycling the reset energy to the source and thereby requiring a much higher voltage power switch, or wasting all the reset energy in a lower voltage clamping circuit.

Since neither choice was particularly attractive - and to save the cost of a separate reset winding on the transformer - the solution for this design was to use an R-C-D snubber for reset. This passive resistor-capacitor-diode network will generate a variable clamp voltage - high at minimum V_{IN} since the capacitor has less time when it is not charging, and lower at high V_{IN} since the shorter on-time provides more discharge time for the capacitor. An obvious benefit of this solution is simplicity - only three passive components and no reset winding on the transformer. The disadvantage is that there is some reset energy lost in the resistor but in this case it was only approximately 0.5W. Using this R-C-D clamp

allowed setting the maximum duty cycle at 67% at low line, while still clamping the maximum drain voltage of the switch to 500 volts under high line conditions. These drain voltage waveforms are shown in Figure 5.

TRANSFORMER DESIGN

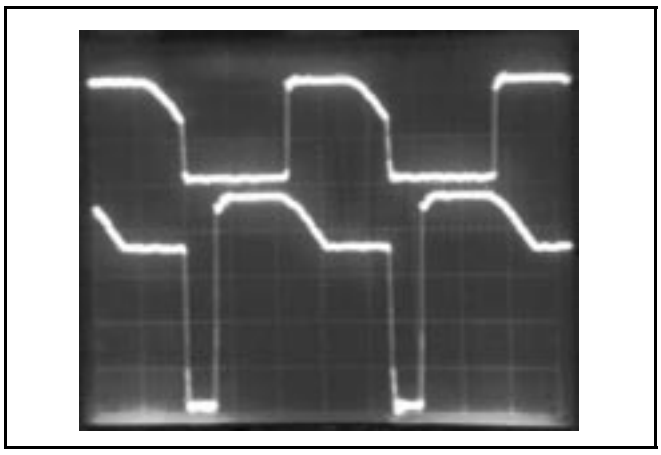

Figure 5. FET drain voltage at full load with V_{IN} = 85 VAC (top trace) and V_{IN} = 264 VAC (lower trace) V = 100V/div, H = 1.0µs/div.

Since this power supply is intended for world-wide operation, the line voltage range was established as 85-264 VAC. This means the peak rectified DC input voltage could be assumed to range from 120 to 373 VDC, but allowing 25 volts of ripple at low line brings the lower limit down to 95 volts. With a switching frequency of 225kHz, the maximum on-time would be 67% of 4.44µsec, or 2.9µsec at the lowest input voltage.

For reasons of cost and size, a Philips EFD-25 ferrite core (3F3 material) was selected through an iterative process of determining a flux swing from the high-frequency core loss characteristics of an assumed core size, using Faraday's law to calculate the number of turns, and then verifying that these turns would fit onto that core size. The EFD-25 core structure is shown in Figure 6 and its size yields a core area of 0.58cm^2 and a volume of 3.3cm^3. If the flux swing is less than 1.25kG at 225kHz, the core loss should be less than 0.25 Watt. The number of turns are calculated from

$$V_{IN} = \frac{N\,\Delta B\,Ae}{T_{ON}\,10^8} \qquad \text{or}$$

$$N = \frac{95V \bullet 2.9\mu s \bullet 10^8}{1250G \bullet 0.58cm^2} = 38t$$

which was rounded up to 40 turns.

The number of secondary turns is calculated from

$$V_O = [V_{IN} \bullet \frac{Nsec}{Npri} - Rect\ drop] \bullet Duty\ Cycle, \text{ or}$$

$$12 = [95 \bullet \frac{Nsec}{40} - 1.0V\,]\ 0.67, \text{ which yields}$$

Nsec = 8 turns. (10 turns was used in this example to provide added operating margin.)

The final transformer design, which is illustrated in Figure 7, incorporated 40 turns of #24 wire wound in two sections to sandwich the secondary, which consisted of 10 turns of four strands of #26 wire. The DC resistance of the primary calculated 0.16 Ohm while the secondary amounted to 0.016 Ohm. Using these values and the core loss curves, the total power loss was calculated as:

Primary loss	=	153mW
Secondary loss	=	243mW
Core loss	=	165mW

Total loss	=	561mW

which, in consideration of the transformer's volume of approximately four cm^3, should experience a maximum temperature rise of less than 20^{o}C.

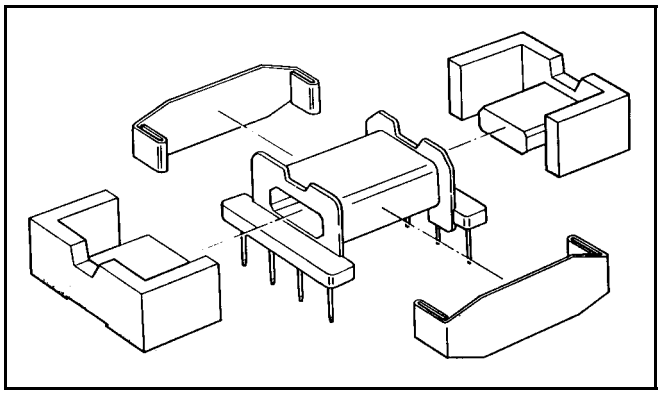

Figure 6. The Philips EFD core assembly optimized for low board profile.

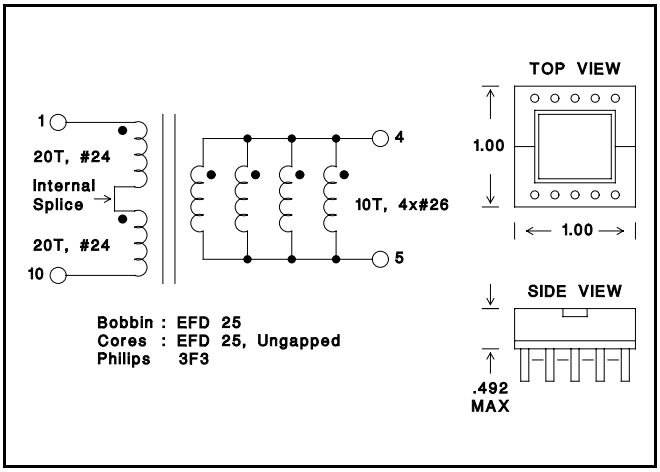

Figure 7. Power transformer schematic and physical dimensions.

OUTPUT INDUCTOR DESIGN

The output inductor must be designed to handle the maximum DC load current without saturating while maintaining continuous conduction at the minimum load. This minimum load was arbitrarily set at 5% of the full 4 Amp load. The worst-case light-load condition occurs at high line where the duty-cycle is calculated to be 0.13 which gives an off-time of 3.9µsec. The minimum value of inductance can then be calculated as

$$L = V\ dt/di, \text{ or } \frac{13V \bullet 3.9\mu s}{0.4A} = 127\mu H$$

The number of turns is calculated from the core characteristics, picking a core large enough to retain adequate inductance at maximum load. In this case, these goals were met with a Mag Inc toroidal 55310-A2 core and 38 turns of #20 wire. Since the control bootstrap voltage and the output can be equal in this case, a second 38 turns of #34 wire powers the control circuit. Power lost in the inductor is calculated as 92mW in the core and 630mW in the wire resistance for a total of approximately 0.75 Watt.

CONTROL CIRCUIT POWER

Another early question to be answered in the design of an off-line power supply is the method used to power the control circuit. Two obvious possibilities are often ruled out: using a separate 60Hz step-down transformer is costly overhead in a low power application; and powering the primary circuitry directly from the high bulk voltage will require a series dropping resistor whose power dissipation is usually unacceptable. While BiCMOS control circuits require very little quiescent current, the determining factor is now usually the power MOSFET gate drive energy. The average gate current for a power MOSFET can be approximated by

$$Ig(ave) = Qt \bullet f$$

where Qt is the total gate charge and f is the switching frequency. Note that this current is relatively unaffected by input voltage, duty-cycle, or output loading. Therefore, I_{CC} for the UCC3570 can be assumed to have three distinct fixed values: pre-startup, active but with no output switching, and operating the power switch.

The most common method for supplying primary control power is the use of a low voltage "bootstrap" winding from the high frequency power transformer. Since this power source is only active when the circuit is switching, start-up energy must still come from the bulk voltage and it must be recognized that anything which stops the switching will cause the control circuit to lose power. When using a separate winding on the transformer with a forward topology, the peak voltage will vary with input voltage which could result in some power loss if the control voltage must be clamped. This application solves that problem by taking power from a second winding in the output inductor. The polarity is such that this winding conducts during flyback when it has the output voltage (times the turns ratio) across it.

POWER MOSFET SELECTION

While the choice of power switch is primarily determined by the input voltage and current, secondary considerations must include the balancing of conductive losses - determined by $R_{DS}(on)$ - against the switching losses which are largely related to the gate charge requirements and the capability of the drive circuitry. The device selected for this supply is the Motorola MTP4N80E which has the following key specifications:

Drain-source voltage.....800 Volts

Continuous drain current .....3 Amps

$R_{DS}(on)$ at 25°C.....1.95 Typ, 3.0 Max Ohms

Total gate charge .....36 Typ, 80 Max nC

Drain-source capacitance 200pF

With a 40:10 transformer turns ratio, the input current will be approximately one Amp. The conductive loss is calculated from the input current (adding a factor to account for less than 100% efficiency), the drain-source resistance (accounting for its positive temperature coefficient), and the maximum duty cycle.

The switching losses are best determined empirically but they can be estimated with a knowledge of the switching times, calculated from the total gate charge divided by the peak gate current. These times are typically less than 50nsec since the UCC3570 can deliver up to one Amp of gate current.

In this design, the total power loss estimates for the MOSFET are

Conductive loss..... 2.0 Watts

Switching losses ..... 4.7 Watts

With a total of 6.7W, this device will have the highest dissipation within the supply and heatsinking the TO-220 package will be required.

UCC3570 PROGRAMMING

Establishing the operating parameters for the UCC3570 requires a very straight-forward series of independent calculations which are well described in the data sheet for this device. The following is merely a simple overview, listing the recommended sequence of calculations. The block diagram of Figure 1 should be referenced for all component designations and it should be assumed that all equations are first-order approximations with more exact values to be defined empirically.

1. Set chip operating current : $I_{SET} = 1V / R4 = I4$

2. Set switching frequency : $fs = 1.8 / (R4 \bullet C_T)$

3. Set minimum deadtime : $td = 0.3 \bullet R4 \bullet C_R$

4.Set feed-forward range : The UCC3570 establishes this range as 4:1 by the 4V and 1V limits set for V_{FWD}. Therefore,

$V_{IN}(Max) = 4 \bullet (R1 + R2) / R2$, and
$V_{IN}(Min) = 1 \bullet (R1 + R2) / R2$.

Note that if a greater range is required, or a voltage range different from that of the duty cycle, it can be accommodated by raising R2 and R3 off ground by a small bias voltage, 0 < Vb < 1V, or by using the equivalent circuit shown in Figure 8.

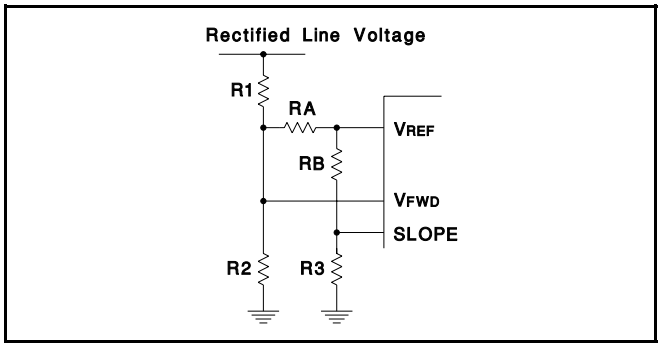

Figure 8. Modifying the 4:1 the input voltage ratio. RA works with R2 to increase the voltage range and RB works with R3 to change the feed-forward gain.

5.Set feed-forward slope : The up-slope of the ramp waveform is

$dV / dt = 10 \bullet V_{FWD} / (R3 \bullet C_R)$.

This can be used to define

$t_{ON}(Max) = 0.3 \bullet R3 \bullet C_R / 1V$, and
$t_{ON}(Min) = 0.3 \bullet R3 \bullet C_R / 4V$.

6.Set current fault parameters : The value for the current sensing resistor is established by the 200mV threshold for the CURLIM pin. Shutdown will occur when the circuit is operating in current limit mode for a time determined by

Time to S/D = $4V \bullet C_F \bullet R4 \bullet (T / t_{OFF})$

Note that this time will be extended by the current which is drained away from C_F by the action of R_F.

The total schematic and parts list for this application are given in Appendix A (see page 10) and some representative waveform photographs of its performance are shown in Figures 9 through 12. While this converter design could find many practical applications as shown, many additional options are possible. For example, reducing the value of the start-up resistor (R5 in Figure 1) such that V_{CC} will not fall below 9 volts after shutdown interrupts the bootstrap voltage, will provide a positive latch-off from a fault. Output over-voltage shutdown can easily be added by a sensing circuit on the secondary driving the COUNT pin through a second optocoupler. And, of course, it should be easy to reconfigure this design to further optimize efficiency, size, cost, or power level to meet a different set of priorities.

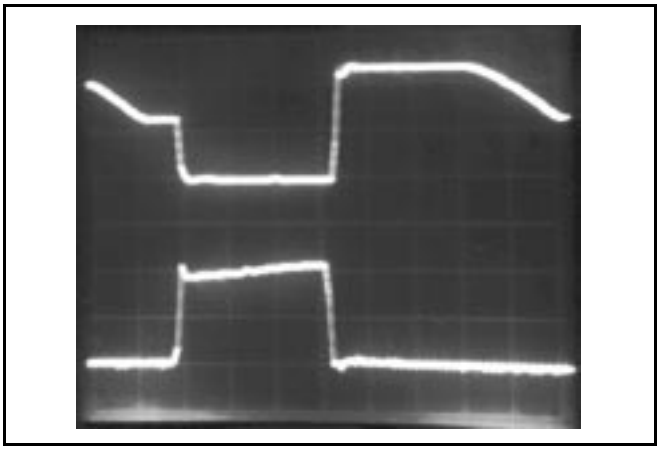

Figure 9. Drain voltage and current at 115VAC and full load. V1 = 100V/div, V2 = 0.5A/div, H = 0.5µsec/div.

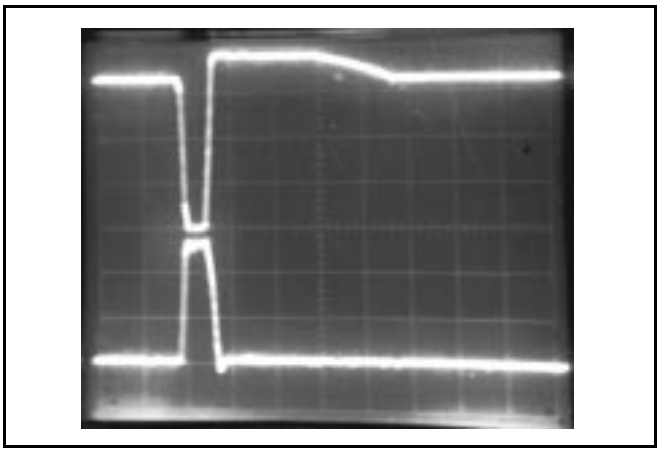

Figure 10. Drain voltage and current under short circuit conditions at 264VAC input. V1 = 100V/div, V2 = 0.5A/div, H= 0.5µsec/div.

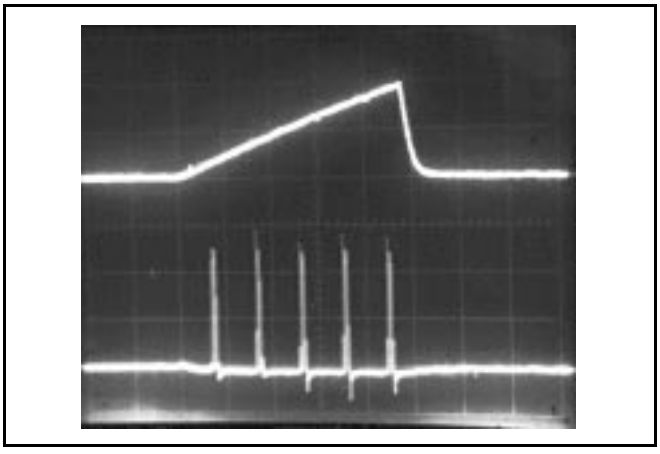

Figure 11. Count voltage with a continuous short circuit (current waveform is aliased) V = 2V/div, H = 2msec/div.

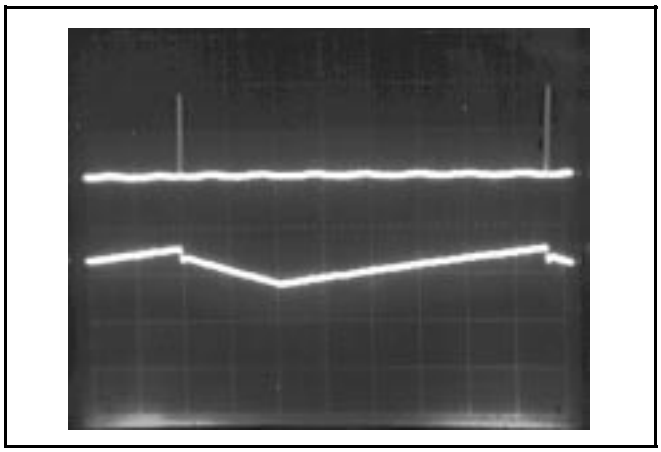

Figure 12. Auto recycle with the output shorted. V1 is count waveform at 2V/div, V2 is VCC at 5V/div, H = 0.2 seconds/div.

A SIMPLE DC/DC CONVERTER

A second application for the UCC3570 illustrates its use in an isolated DC-to-DC converter designed for a load module in a distributed power system architecture or as a telecom power source. This 20 Watt design, as shown in Figure 13, will accept an input voltage from 30V to 60V while maintaining a constant 5V output. A unique element of this design is the controller's ability to get its supply current from only the input voltage, eliminating the need for a low-voltage bootstrap supply driven from the power transformer. This is made practical by both the low operating current of the UCC3570 and by driving a low-gate charge FET at less than maximum frequency. The IRF630 has a total gate charge requirement of only 30nC maximum which, at 100kHz, means only 3mA of average gate current. Add 1mA for the IC, another for miscellaneous programming resistors, and 5mA is all that is needed for the total primary circuitry. This can readily be taken directly from the input voltage but, for improved efficiency, a simple current source has been added to keep this current constant with changing input voltage levels.

Without a bootstrap voltage source to collapse and recycle VCC after a fault-activated shutdown, this design would normally require a manual restart; however, several other options are possible. For example, adding a diode from the VFWD to Soft-Start pins will provide a hiccup operating mode but with a relatively short off-time. For a low duty-cycle mode, a delayed restart can

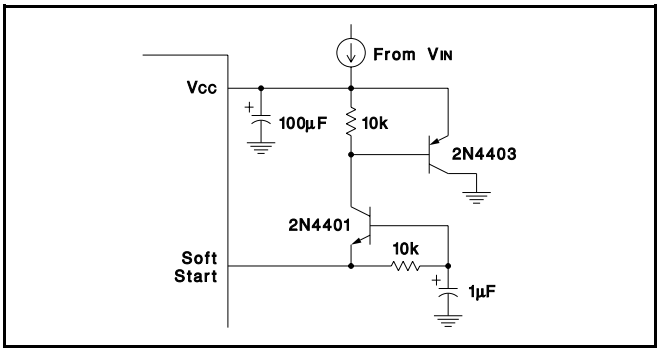

Figure 14. Two transistors will provide an external auto-restart by recycling VCC when Soft-Start is reset.

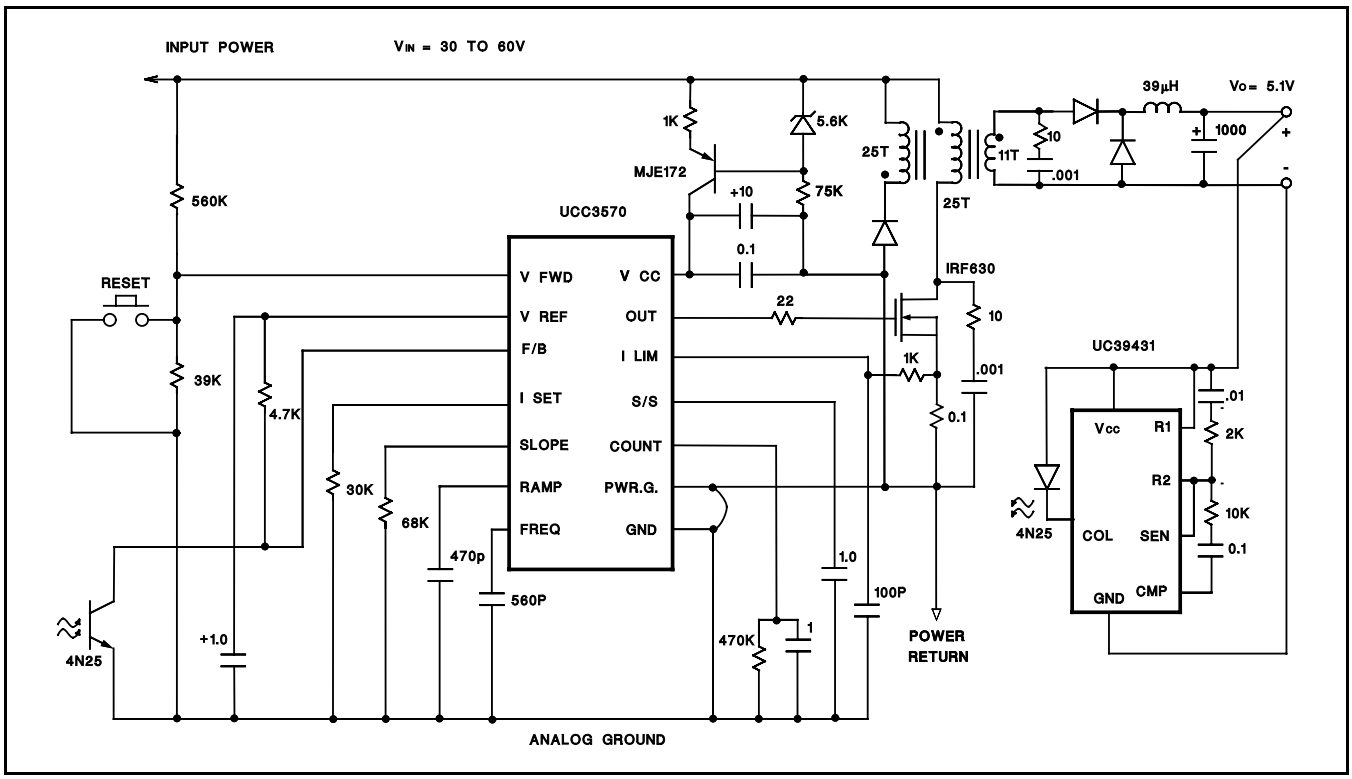

Figure 13. An isolated 25W, 48V to 5V converter including the UC39431 as an optocoupled feedback generator.

be accomplished with the two-transistor circuit shown in Figure 14. This circuit uses the energy in the soft-start capacitor to discharge the V_{CC} capacitor which gives a turn-on delay equivalent to normal start up. The operation of this circuit is illustrated in Figure 15.

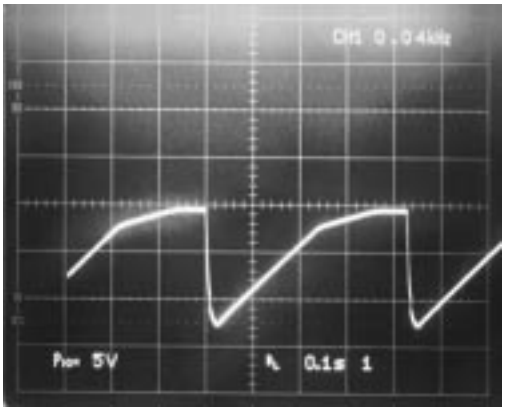

Figure 15. With auto re-start, a shorted output recycles V_{CC} with a 0.4 second delay.

Another option for eliminating a latched shutdown is to simply short the COUNT pin to ground which will prevent activation of the Shutdown Latch unless the Current Limit threshold of 600mV is exceeded - an unlikely event considering the 80nsec response of the pulse-by-pulse current protection. Figure 16 shows operation in this mode with a continuous shorted output.

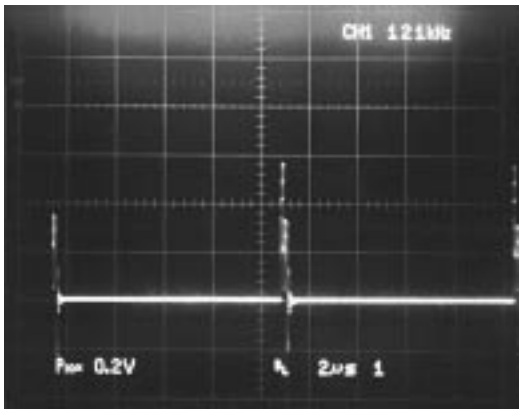

Figure 16. With the Fault Count function disabled, a shorted output reduces the current pulse width such that the peak across R_{CS} remains below shutdown threshold.

This converter design illustrates another characteristic of the UCC3570 which provides both added safety and better utilization of the transformer magnetics. With an input voltage range specified as 30 to 60 Volts, If the OV clamp is set for 60V, the controller will continue to operate down to 15V (1/4 of 60V). However, if the maximum duty-cycle clamp is set for 50% at 30V, the ramp waveform will cause the output to skip pulses at voltages less than 30V insuring against saturation of the power transformer.

The rest of the circuit details for this application can be deduced from the information presented above and the complete schematic and parts list given in Appendix B (see page 12).

SUMMARY

With the minimal need for additional external components and support functions which these two quite different applications have shown, the versatility of the UCC3570 has been demonstrated. Not shown, but equally important is this device's ability to provide the same protection and programmability with power stages scaled up to several hundred Watts, and to efficiently operate at switching frequencies above 500kHz. Thus, once again it has been demonstrated that one can never close the door to "older" technologies and, in this case, revisiting voltage-mode control has yielded a new controller combining efficient operation, stable performance, and ease of application highly attuned to meeting today's stringent requirements for cost-effective power systems.

REFERENCES

Leu, Hua, Lee, and Zhou, "Analysis and Design of R-C-D Clamp Forward Converter" VPEC, Virginia Tech and Delta Power Electronics Lab, Blacksburg, VA.

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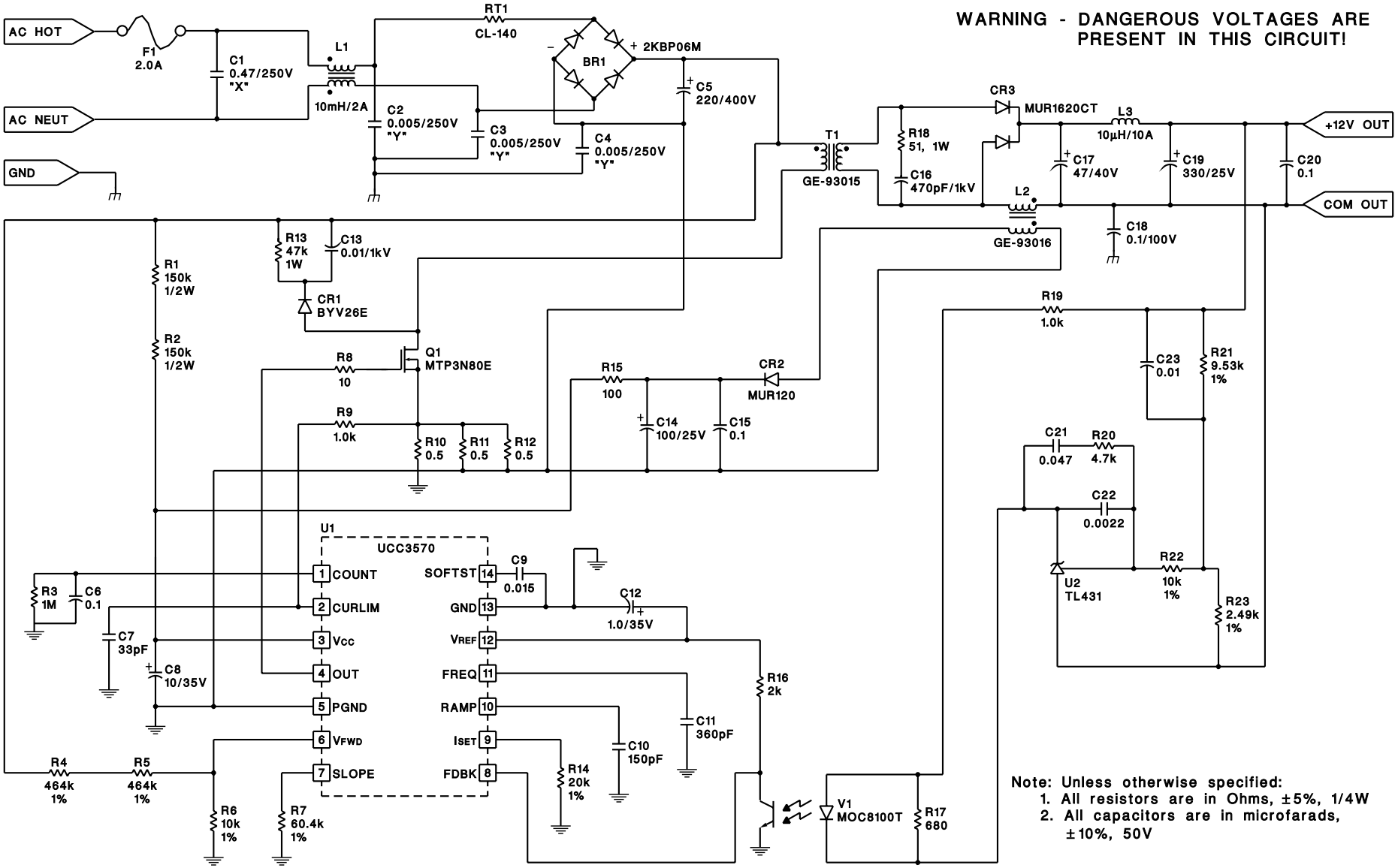
APPENDIX - A
12 VOLT, 50 WATT POWER SUPPLY



48V - 5V, 20W DC/DC CONVERTER
BILL OF MATERIALS

ITEM	QUANTITY	REFERENCE	PART DEFINITION	SOURCE
1	1	CR1	1N752, 5.6V	
2	1	CR2	MUR120	Motorola
3	1	CR3	MBR2045	Motorola
4	1	Q1	MJE172	Motorola
5	1	Q2	IRF630	Int. Rect.
6	1	U1	UCC3570	Unitrode
7	1	U2	4N25	
8	1	U3	UC39431	Unitrode
9	1	T1	Transformer	Custom
10	1	L1	38µH, 5A	Custom
11	1	L2	3µH, 5A	Toko
12	1	C1	3.3µF, 6V	Solid Tantalum
13	4	C2, 5, 16, 18	0.1	
14	1	C3	470pF	
15	1	C4	560pF	
16	1	C6	100µF, 16V	Solid Tantalum
17	1	C7	1.0µF, 12V	Solid Tantalum
18	1	C8	1000µF, 63V	
19	1	C9	1.0µF	
20	1	C10	100pF	

ITEM	QUANTITY	REFERENCE	PART DEFINITION	SOURCE
21	1	C11	.001µF, 500V	
22	1	C12	.001µF	
23	1	C13	0.1µF, 100V	
24	2	C14, 15	1000µF, 10V	
25	1	C17	.01µF	
26	1	R1	560k, 1%	
27	1	R2	39k, 1%	
28	1	R3	4.7k	
29	1	R4	30k,1%	
30	1	R5	68k, 1%	
31	1	R6	1.0k	
32	1	R7	75k	
33	1	R8	470k	
34	1	R9	22Ω	
35	1	R10	1.0k	
36	1	R11	0.1Ω	
37	1	R12	1.2k	
38	2	R13, 14	10Ω, 1/2W	
39	1	R15	2k	
40	1	R16	10k	

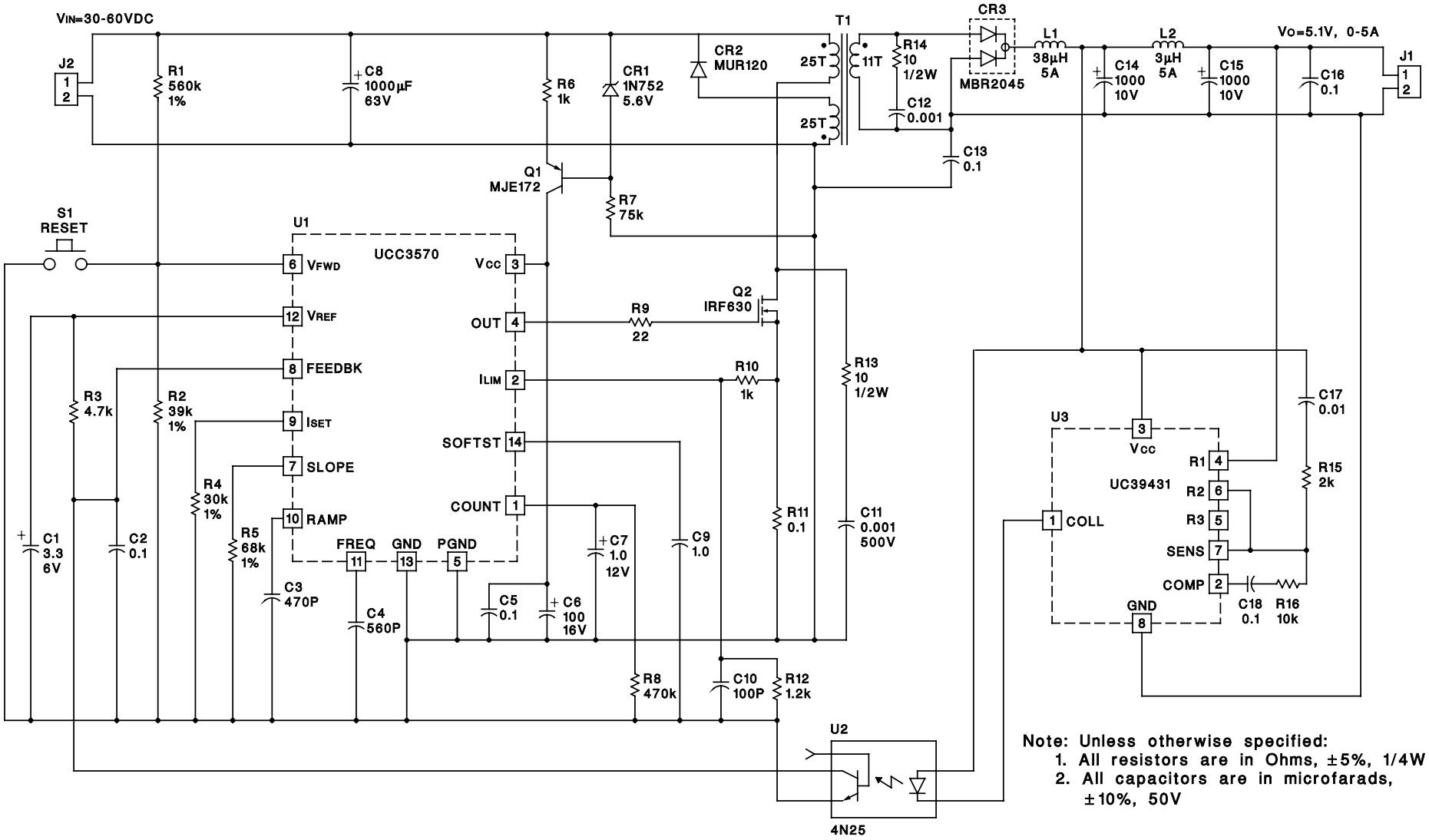
Magnetics Winding Information

T1:
Core: EI187-3C80 (Philips)
Primary: 25 Turns Bifilar = 26AWG
Reset: 25 Turns = 31AWG (Wound with Primary)
Secondary: 11 Turns Quadfilar = 25AWG

L1:
Core: T68-52D (Micrometals)
Winding: 21 Turns = 20AWG

L2:
Toko 262LYF-0077M

APPENDIX - B
48V - 5V, 20W DC/DC CONVERTER



Note: Unless otherwise specified:
1. All resistors are in Ohms, ±5%, 1/4W
2. All capacitors are in microfarads, ±10%, 50V

12 VOLT, 50 WATT POWER SUPPLY
BILL OF MATERIALS

ITEM	QUANTITY	REFER-ENCE	PART DEFINITION	SOURCE
1	1	BR1	2KBP06M	General Inst.
2	1	CR1	BYV26E	Philips
3	1	CR2	MUR120	Motorola
4	1	CR3	MUR1620CT	Motorola
5	1	Q1	MTP3N80E	Motorola
6	1	V1	MOC8100T	Motorola
7	1	U1	UCC3570N	Unitrode
8	1	U2	TL431	
9	1	T1	GE-93015	GFS Mfg.
10	1	L1	10mH/2A	Coilcraft
11	1	L2	GE-93016	GFS Mfg.
12	1	L3	10µH/10A	Coiltronics
13	1	F1	2.0A Fuse	
14	1	C1	0.47µF, 250V, "X"	Roederstein
15	1	C2	.005µF, 250V, "Y"	Roederstein
16	1	C3	.005µF, 250V, "Y"	Roederstein
17	1	C4	.005µF, 250V, "Y"	Roederstein
18	1	C5	220µF/400V	Panasonic
19	1	C6	0.1µF/50V	Polyester
20	1	C7	33pF/100V	Ceramic NPO
21	1	C8	10µF/35V	Solid Tantalum
22	1	C9	0.015/50V	Ceramic X7R
23	1	C10	150pF/100V	Ceramic NPO
24	1	C11	360pF/100V	Ceramic NPO
25	1	C12	1.0µF/35V	Solid Tantalum
26	1	C13	0.01µF/1kV	Ceramic X5F
27	1	C14	100µF/25V	Aluminum
28	1	C15	0.1µF/100V	Polyester

ITEM	QUANTITY	REFER-ENCE	PART DEFINITION	SOURCE
29	1	C16	470pF/1kV	Ceramic YSF
30	1	C17	47µF/40V	Aluminum
31	1	C18	0.1µF/100V	Polyester
32	2	C19	330µF/25V	Aluminum
33	1	C20	0.1µF/100V	Polyester
34	1	C21	0.047µF/100V	Ceramic X7R
35	1	C22	.0022µF/100V	Ceramic X7R
36	1	C23	0.01µF/100V	Ceramic X7R
37	1	RT1	CL-140	Keystone
38	2	R1, R2	150k, 1/2W	
39	1	R3	1M	
40	2	R4, R5	464k, 1%	RN55D
41	1	R6	10k, 1%	RN55D
42	1	R7	60.4k, 1%	RN55D
43	1	R8	10Ω	
44	1	R9	1.0k	
45	3	R10,11,12	0.5Ω	Carbon Film
46	1	R13	47k, 1W	
47	1	R14	20k, 1%	RN55D
48	1	R15	100Ω	
49	1	R16	2.0k	
50	1	R17	680Ω	
51	1	R18	51Ω, 1W	
52	1	R19	1.0k	
53	1	R20	4.7k	
54	1	R21	9.53k, 1%	RN55D
55	1	R22	10k, 1%	RN55D
56	1	R23	2.49k, 1%	RN55D

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