200-W Interleaved Forward Converter Design Review Using TI's UCC28221 PWM Controller

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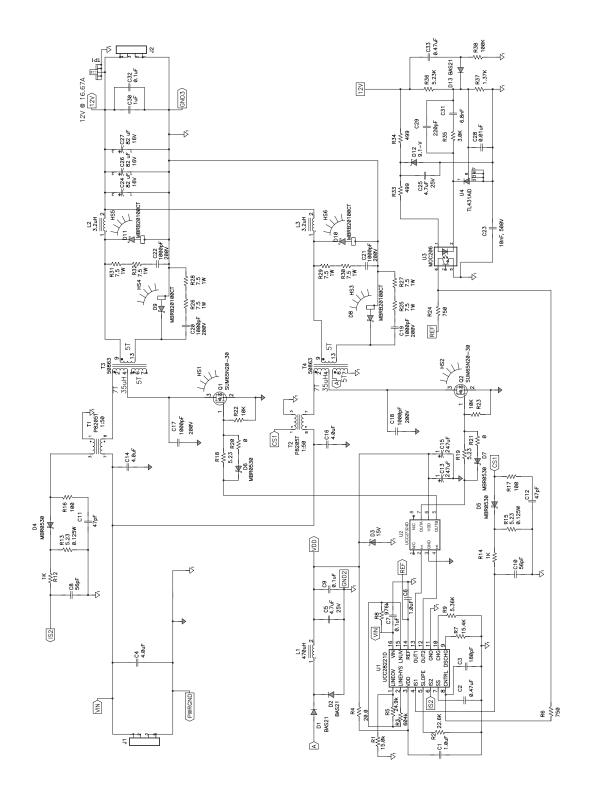
ABSTRACT

Interleaved buck converters are widely used in the personal computer industry in voltage regulation module (VRM) applications to power central processing units, CPUs, like the Pentium 4™ and Athlon™. This topology is widely used due to the reduced input and output capacitor ripple current that is gained by interleaving the converters as compared to a single buck power stage. The reduction in input and output capacitor RMS currents allows the designer to reduce the input and output capacitor banks that are required for the design. The same benefits that are gained from interleaving buck converters can be gained from interleaving forward converters. In high current applications such as telecom dc-to-dc converters reducing the input and output capacitor banks can reduce the size and cost of the design. This application note reviews the design of a telecom converter that converts a telecom input range of 36 V to 75 V dc down to a regulated 12-V, 200-W dc output. The design information in this application note is used in the design of the UCC28221 Evaluation Module (EVM) HPA035 [5].

Table 1. Applicable Devices

	MIN	TYP	MAX	UNITS
Input voltage (V_{IN})	36		75	V
Output voltage (V_{OUT})	11.4	12	12.6	V
Output power (P_{OUT})	50		200	W
Switching frequency (f_S)		500		kHz
Efficiency at maximum output power (η)	85%			
Maximum duty cycle (D_{MAX})			50%	
Input voltage ripple ($V_{IN(ripple)}$)		1		V
Output voltage ripple ($V_{OUT(ripple)}$)		200		mV

NOTES:This design was based on typical design values.

1   Schematic

Figure 1. Typical Application Diagram

2   Power Stage Design

2.1   Transformer Turns Ratio (T3 and T4)

The first step is to calculate the required transformer turns ratio required for the design. The following equations are used to calculate the approximate transformer turns ratio. With a maximum duty cycle of 0.5 at minimum input voltage ($V_{IN(min)}$) the calculated turns ratio for the design is roughly 1.4.

$$a = \frac{N_P}{N_S}$$

$$a = D_{MAX} \frac{V_{IN(min)} - 1\ V}{V_{OUT} + 1\ V} \approx 1.4$$

2.2   Output Inductor Selection (L2 and L3)

The output inductor was sized based on the worst case ripple current that occurs at minimum duty cycle, D_{MIN}, and a maximum output power, $P_{OUT(max)}$, of 200 W. The output capacitor ripple current cancellation of interleaving two forward converters allowed the output inductors L_{OUT} to be designed for a ripple current that was roughly 60% of the maximum load current. For this design we used 3.2-µH low profile inductors from Vishay, part number IHLP–5050FD–RZ–3R3–M–01.

$$D_{MIN} = a\left(\frac{V_{OUT} + 1\ V}{V_{IN(max)} - 1\ V}\right)$$

$$L_{OUT} = \frac{V_{OUT}\left(1 - D_{MIN}\right)}{\left(0.6 \dfrac{P_{OUT(max)}}{V_{OUT} \times 2} f_S\right)}$$

2.3   Selecting Semiconductor Devices for the Design (Q1, Q2, D8, D9, D10, D11)

Before selecting electrical components for output diodes and FETs a power budget needs to be set for each component, P_{SEMI}, to ensure that the efficiency goal (η) of 85% can be achieved. To achieve this design goal a power budget was set for each semiconductor device to dissipate less than one sixth the maximum allowable losses, which for this design was roughly 5 W.

$$P_{SEMI} \le P_{OUT(max)}\left(\frac{1 - \eta}{6}\right) \approx 5\ W$$

2.4 Forward FET Selection (Q1 and Q2)

Finding the proper FETs for the design to achieve the efficiency goal is always a trial and error process. The following equations will help you estimate the maximum drain to source voltage of the FET ($V_{DS(max)}$) and the power dissipated by the FET. $I_{PEAK(Q1)}$ is the peak FET current. P_{SWITCH} is estimated transitional losses of the FET, where ton and toff are the rise and fall times of the FET. P_{GATE} is the losses generated by driving the gate of the FET. P_{COSS} is the FET capacitance (C_{OSS}) losses. The sum of all of these losses (P_{Q1}) gives a good estimation of total FET losses. For this design we selected a Vishay FET part number SUM65N20–30, which is a 200-V FET that had an estimated loss off roughly 6.8 W, this loss was slightly higher than what was budgeted and left a little less room for the losses of the output rectifiers.

$$V_{DS(max)} = \left[V_{IN(max)} \frac{D_{MAX}}{\left(1 - D_{MAX}\right)} \right] \frac{\pi}{2} + V_{IN(max)}$$

$$I_{PEAK(Q1)} = \left[\frac{P_{OUT(max)}}{2 \times V_{IN(min)} \times D_{MAX}} \right]$$

$$P_{SWITCH} = \left(\frac{V_{IN(max)}}{2} \right) \left(I_{PEAK(Q1)} \right) \left(t_{ON} + t_{OFF} \right) f_S$$

$$P_{GATE} = Q_G \times V_{GATE} \times f_S$$

$$P_{RDS(on)} = \left(I_{PEAK} \times \sqrt{D_{MAX}} \right)^2 \times R_{DS(on)}$$

$$P_{COSS} = \frac{1}{2} C_{OSS} \times V_{IN(max)}{}^2 f_S$$

$$P_{Q1} = P_{Q2} = P_{SWITCH} + P_{GATE} + P_{RDS(on)} + P_{COSS}$$

2.5 Output Rectifier Selection (D8, D9, D10, D11)

The power budget that is remaining for the output rectifier selection is roughly 16.4 W. The following equations will estimate the maximum reverse voltage on the output rectifiers, $V_{D(max)}$, and the maximum power dissipated by all the diodes combined $P_{D(max)}$. The diodes used in this design had roughly 0.75-V forward voltage drop and at this power level the 4 diodes would dissipate roughly 12.5 W. 100-V Schottky rectifiers are needed to withstand a maximum reverse voltage of 85 V.

$$V_{D(max)} = \left[\frac{V_{IN(max)} \times D_{MAX}}{\left(1 - D_{MAX}\right)} \right] \frac{\pi}{2} \times \frac{1}{a}$$

$$P_{D(max)} = \frac{P_{OUT} \times Vf}{V_{OUT}}$$

2.6 Review of the Benefits of a Two Phase Interleaved Forward Converter

A two phase interleaved forward converter is just simply two forward converters operating 180 degrees out of phase. The two key benefits of interleaving are reduced input and output capacitor ripple currents as compared to a standard forward converter. The waveforms in Figure 3 show the filter capacitor ripple currents at 50% duty cycle (D).

The input capacitor C_{IN} needs to filter out the ac portion of the transformer load currents. The input capacitor current (I_{CIN}) is the dc input current, I_{IN}, less the two transformer currents (It1+It2). As D approaches 50% the sum of the transformer load currents approach a dc input current. The input capacitor only needs to filter reflected output inductor current and transformer magnetizing current.

The output capacitor C_{OUT} needs to filter the ac portion of the inductor currents. The ac current is the dc load current (I_{OUT}) less the two inductor ripple currents (I1+I2). At 50% duty cycle the two inductor currents are 180 degrees out of phase and the inductor currents are symmetrical. The sum of these two currents is a dc current and the filter capacitor ideally would not have to filter any inductor current.
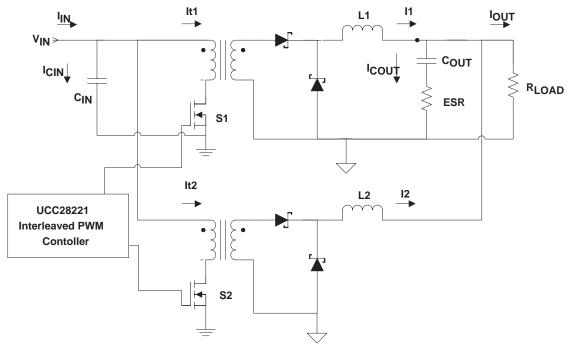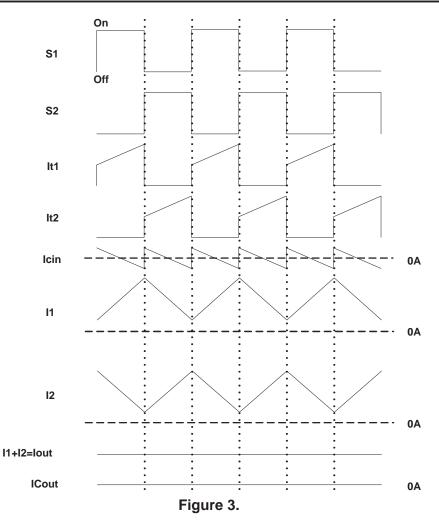

Figure 2. Interleaved Forward Converter

Figure 3.

The input and output capacitance ripple current varies with duty cycle. As the duty cycle varies from 50% the input current becomes more discontinuous due to varying transformer loading. The output inductor ripple currents also become less symmetrical as the duty cycle varies from 50% and the inductor ripple currents do not cancel as well. To design an interleaved forward converter the designer must be aware of this circuit behavior to select input and output filter capacitors.
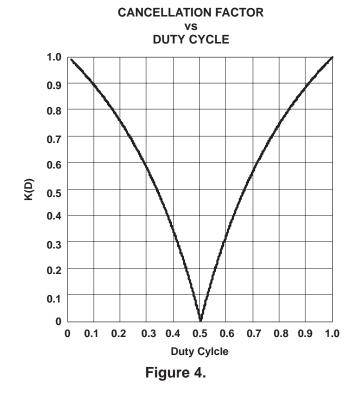
2.7 Output Capacitance Selection

Selecting the output capacitor is similar to selecting an output capacitor for a forward converter. The capacitor needs to be selected to meet an output voltage ripple requirement that is dependent on the amount of ac inductor ripple current that needs to be filtered. It is required that the worst case output capacitor current be calculated. The graph in Figure 4 and the following calculations show how the ratio of capacitor ripple current and inductor ripple current vary with D. In this design the duty cycle varies from 0.25 to 0.5. From the graph it can be observed that the worst case ripple current occurs at 25% duty cycle. For this design the worst case ripple current was roughly 4 A.

$$K(D) = \frac{\Delta I_{COUT}}{\Delta IL_{OUT}}$$

$$K(D) = \left| \frac{1 - 2D}{1 - D} \right| \text{ if } D \leq 0.5$$

$$K(D) = \left| \frac{1 - 2 \times (1 - D)}{1 - (1 - D)} \right| \text{ if } D > 0.5$$

CANCELLATION FACTOR
vs
DUTY CYCLE

Figure 4.

The following equations can be used to size the output capacitance (C_{OUT}) and maximum allowable equivalent series resistance (ESR) for the design. For this design the maximum allowable ESR was roughly 21 mΩ and the minimum output capacitance required for the design was roughly 12 μF.

$$ESR = \frac{V_{RIPPLE} \times 0.4}{\Delta I_{COUT}} = 0.021 \; \Omega$$

$$C_{OUT} = \frac{\Delta I_{COUT} \times D_{MIN}}{8 \times V_{RIPPLE} \times 0.1 \times f_S} \approx 12 \, \mu F$$

The calculation for output capacitance RMS current is straight forward and can be calculated as follows.

$$I_{RMS} = \frac{\Delta I_{COUT}}{\sqrt{3}} \approx 2.1 \; A$$

2.8 Input Capacitance Selection (C4, C14, C16)

Selecting the input capacitor is similar to selecting the input capacitor on a forward converter. It is dependent on ripple voltage requirements and capacitor ripple current. The first step is to calculate the worst case capacitor ripple current. The following equations and Figure 5 show how the input capacitor RMS current ($I_{CIN(rms)}$) varies with duty cycle. In this design D varies from 0.25 to 0.5, from the graph it can be observed that the worst case input ripple current occurs at a duty cycle of 25%. The worst case RMS current for this design was roughly 3 A.

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}}$$

$$IC_{IN(rms)} = \left| \frac{I_{OUT}}{2 \times a} \times \sqrt{2 \times D \times (1 - 2 \times D)} \right| \text{ if } D \leq 0.5$$

$$IC_{IN(rms)} = \frac{I_{OUT}}{2 \times a} \times \sqrt{2 \times (D - 0.5) \times [1 - 2 \times (D - 0.5)]} \text{ if } D > 0.5$$
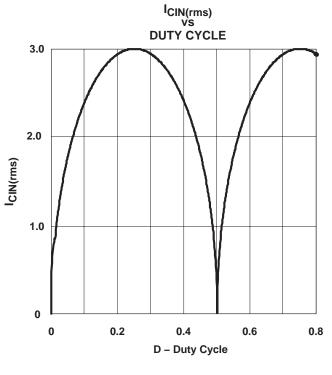
$$\textbf{I}_{\textbf{CIN(rms)}}$$
$$\textbf{vs}$$
$$\textbf{DUTY CYCLE}$$

Figure 5.

The following equations were used to select the minimum input capacitance (C_{IN}) and the maximum allowable ESR_{CIN} for the design. $V_{RIPPLE(in)}$ is the input voltage ripple requirement which was 3% of the minimum input voltage $V_{IN(min)}$. The peak input capacitor current, $I_{PEAK(cin)}$, for this design was roughly 8 A and the maximum allowable ESR for the design was roughly 135 mΩ.

$$I_{PEAK(cin)} = \left[\frac{P_{OUT}}{2 \times V_{OUT}} + \frac{\Delta IL_{OUT}}{2} \right] \frac{1}{a}$$

$$ESR_{CIN} = \frac{V_{RIPPLE(in)}}{I_{PEAK(cin)}}$$

To select the minimum input capacitance requires calculating the duty cycle ratio D where the RMS current is at its peak. For this design the largest amount of ripple current occurs at D of 0.25 and would require a minimum input capacitance of roughly 12 µF to meet ripple requirements.

$$C_{IN} = \frac{- \left[\frac{I_{OUT} \times D}{a} - \frac{I_{OUT}}{2a} \right] D}{V_{RIPPLE(in)} \times f_S} \quad \text{if } D \leq 0.5$$

$$C_{IN} = \frac{- \left[\frac{I_{OUT} \times D}{a} - \frac{I_{OUT}}{a} \right] 1 - D}{V_{RIPPLE(in)} \times f_S} \quad \text{if } D > 0.5$$

2.9 Transformer Design Requirements (T3 and T4)

To reset the transformer the self resonant technique was used. To get the reset technique to work requires that the input magnetizing inductance (L_M) be selected based on total capacitance at the transformer switch node. The following calculations were used to calculate the total capacitance at the switch node (C_{TOTAL}) and the maximum allowable magnetizing inductance. C_D is the reflected junction capacitance of an output rectifier diode (D11). C_{PCB} is the estimated board capacitance and CT_R is the estimated inter winding capacitance of the transformer. To calculate the average drain to source capacitance ($C_{OSS(avg)}$) of the switching FET requires information in the data sheet concerning the specified C_{OSS} capacitance ($C_{OSS(spec)}$) and the drain to source voltage ($V_{DS(spec)}$) where $C_{OSS(spec)}$ is specified. With an off voltage across the FET, $V_{DS(off)}$, of 36 V the average total capacitance (C_{TOTAL}) was roughly 1.6 nF which resulted in a maximum allowable magnetizing inductance (L_M) of roughly 54 μH. To make the design easier we used a transformer manufactured from Payton part number 50863, which had a turn's ratio of 1.4 and a magnetizing inductance of 35 μH.

$$C_D = \frac{C_{DIODE}}{a^2}$$

$$C_{PCB} = 100 \; pF$$

$$CT_R = 100 \; pF$$

$$C_{OSS(avg)} = 2 \times C_{OSS(spec)} \times \sqrt{\frac{V_{DS(spec)}}{V_{DS(off)}}}$$

$$C_{TOTAL} = C_D + C_{PCB} + CT_R + C_{OSS(avg)}$$

$$L_M = \left(\frac{T_{RESET}}{\pi}\right)^2 \frac{1}{C_{TOTAL}} \approx 54 \; \mu H$$

2.10 Slope Compensation Resistor (R2) Selection

To meet the power requirements a current sense transformer with a turn's ratio of (acs) of 1:50 was used in the design. To ensure loop stability, part of the inductor down slope (I_{SLOPE}) needed to be added to the current sense signal. The UCC28221 PWM controller has internal slope compensation that can be set up by selecting an external resistor (R_{SLOPE}). Once the inductor down slope current is calculated, $I_{SLOPE,}$ the amount of voltage needed to add to the current sense signal can be calculated (V_{SLOPE}) and R_{SLOPE} can be selected.

$$I_{SLOPE} = \frac{V_{OUT}(1 - D_{MIN})}{L_{OUT} \times f_S \times a}$$

$$V_{SLOPE} = I_{SLOPE} \times acs \times R_{SENSE}$$

$$R_{SLOPE} = R2 = \frac{2.5 \; V}{25 \times 10 \; pF \times V_{SLOPE} \times f_S}$$

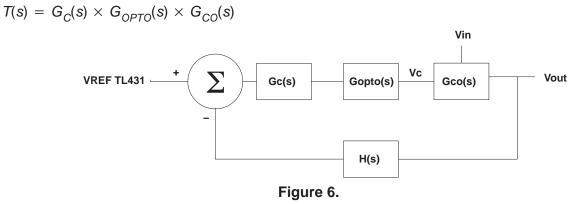## 2.11 Current Sense Resistor Selection (R13 and R15)

To size the current sense resistor (R_{SENSE}) requires the calculation of reflected output inductor current ($I_{REFLECTED}$) as well as, transformer magnetizing inductance current, I_M. For this design based on the transformer magnetizing current and reflected output inductor current, required current sense resistors are roughly 5.25 Ω.

$$I_{REFLECTED} = \left(\frac{P_{OUT}}{2 \times V_{OUT}} + \frac{V_{OUT}(1 - D_{MIN})}{L_{OUT} \times f_S \times 2} \right) \frac{1}{a}$$

$$I_M = \frac{V_{IN(min)} \times D_{MAX}}{L_M \times f_S}$$

$$R_{SENSE} = \frac{1.5\ V}{\left(I_{REFLECTED} \times 1.3 + I_{SLOPE} + I_M \right) \times acs} \approx 5.25\ \Omega$$

3   Voltage Loop Compensation

Figure 6 show the control block diagram for the power converter. To compensate the voltage feedback loop (T(s)) requires a basic understanding of the small signal characteristics of the control to output gain of the power stage ($G_{CO}(s)$) and the small signal characteristics of the compensation network, $G_C(s)$, and the opto isolator, $G_{OPTO}(s)$.

$$T(s) = G_C(s) \times G_{OPTO}(s) \times G_{CO}(s)$$

Figure 6.

The compensation network consisted of a TL431 (U4) used as an operational amplifier and electrical components R36 and R37 set up the dc output voltage. Components R35, C31 and C29 are used to compensate the loop. To select the voltage divider H(s) it is required that the designer pre-select R37 and know the internal reference of the TL431 shunt regulator (V_{REF}).

$$R36 = R37 \times \frac{(V_{OUT} - V_{REF})}{V_{REF}}$$

$$H(s) = \frac{R37}{R36 + R37}$$

$$s = j2 \times \pi \times f$$

$$G_{CO}(s) = \frac{\Delta V_{OUT}}{\Delta V_C} = \frac{a}{acs} \times \frac{RL}{R_{SENSE}} \times \frac{(I + s \times ESR \times C_{OUT})}{(I + s \times RL \times C_{OUT})}$$

$$G_{COdB}(s) = 20 \times \log\left(\left|G_{CO}(s)\right|\right)$$

Opto isolators are generally used in telecom applications to isolate the input from the output. However, these are not ideal devices and can affect your loop compensation. It is a good idea to look at the opto's small signal characteristics. The opto used in the design had the following small signal characteristics $G_{OPTO(s)}$ with a double pole (f_P) of 50 kHz and a Q of roughly 1. This varies depending on the opto that is used in the design.

$$G_{OPTO}(s) = \frac{R24}{R33} \times \frac{1}{\left(1 + \frac{s}{2\pi f p Q} + \left(\frac{s}{2\pi f p}\right)^2\right)}$$

$$G_{OPTOdB}(s) = 20 \times \log\left(\left|G_{CO}(s)\right|\right)$$

The following equation describes the small signal transfer function of the TL431 compensation feedback scheme $G_C(s)$.

- $R_F = R35$

- $R_I = R36$

- $C_Z = C31$

- $C_P = C29$

$$G_C(s) = \frac{\left(s \times R_F \times C_Z + 1\right)}{s \times \left(C_Z\right) \times R_I \times \left(s \times R_F \times C_P + 1\right)}$$

$$G_{CdB}(s) = 20 \times \log\left(\left|G_C(s)\right|\right)$$

In general the voltage loop needs to crossover (f_C) below one sixth of the switching frequency and also needs to be below the opto pole (f_P) [2]. This converter was designed for a crossover frequency (f_C) of 8 kHz to meet these requirements. To select the feedback resistor (R_F) frequires the calculation of the control to output gain ($G_{CODB}(s1)$) and the dB opto gain, $G_{OPTOdB}(s1)$, at the desired crossover frequency (f_C).

$$s1 = J2 \times \pi \times f_C$$

$$R_F = R35 \times 10^{\frac{-\left(G_{OPTOB}(sS1) + G_{CODB}(s1)\right)}{20}} = 3\ k\Omega$$
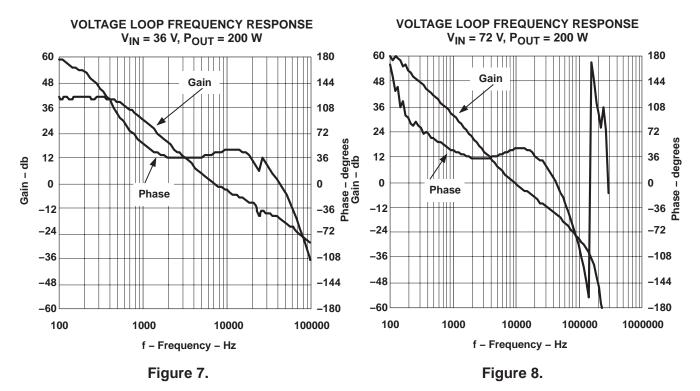
To ensure at least 45 degrees of phase margin (PM) a zero is added in the compensation loop at the desired crossover frequency by selecting capacitor C_Z in the compensation network.

$$C_Z = C31 = \frac{1}{2 \times \pi \times f_C \times R_F} \approx 6.8 \; nF$$

To ensure loop stability another pole is added at half the switching frequency (f_S) to attenuate the high frequency gain. This can be accomplished by selecting the pole capacitor C_P in the compensation network.

$$C_P = C31 = \frac{1}{2 \times \pi \times \frac{f_S}{2} \times R_F} \approx 220 \; pF$$

The bode plots of Figure 7 and 8 show the voltage loop ($T_{dB}(s)$) frequency response of the power converter at minimum and maximum input voltage at maximum load. From these graphs it can be observed that the power converter's voltage loop at minimum input of 36 V had a crossover frequency of roughly 7 kHz with a phase margin of 42 degrees. At the maximum input of 75 V the voltage loop crossed over at roughly 9 kHz with a phase margin of roughly 46 degrees.

Figure 7.

Figure 8.

Design Performance

Figure 9 shows the overall system efficiency of the converter. From the graph it can be observed that at maximum load the efficiency of the converters was between 87% and 90% which met the design goal of 85%.
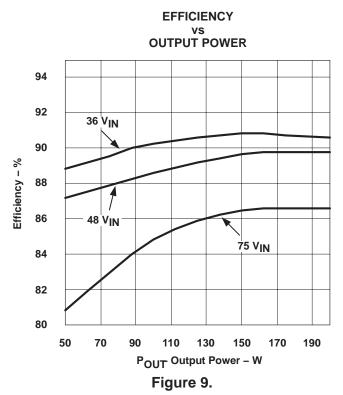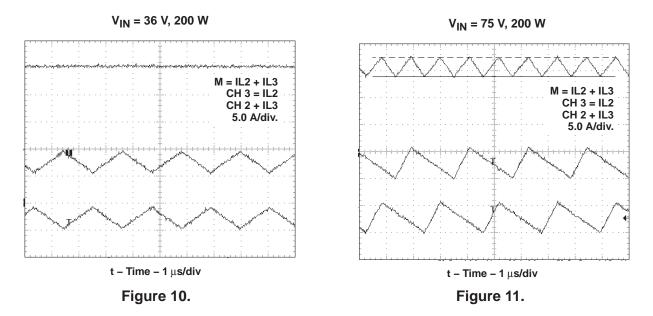
EFFICIENCY
vs
OUTPUT POWER

Figure 9.

Figure 10 shows the output capacitor ripple current cancellation at a miminum input voltage of 36 V and output power of 200 W. The power converter's duty cycle at minimum input voltage is roughly 50% and the module has the least amount of capacitor ripple current. From the oscilloscope graph below it can be observed when the converter is operating at 50% duty cycle the sum of the two inductor currents is roughly a dc current and 100% of the inductor current is being delivered to the load. The output capacitor at minimum input voltage does not have to filter any of the inductor ripple current.

Figure 11 shows the output capacitor ripple current cancellation at a maximum input voltage of 75 V and an output power of 200 W. The power converter's duty cycle at maximum input voltage is roughly 25% and the module has the greatest amount of capacitor ripple current. At 25% duty cycle the sum of the two inductor currents which is fed to the output has a ripple current of roughly 65% of a single inductor's ripple current. The inductor ripple current that the output capacitor has to filter is 35% less than it would have been using a single phase forward converter. In high current applications this can dramatically reduce the amount of filter capacitance needed, reducing the cost and size of the design.

V_{IN} = 36 V, 200 W

V_{IN} = 36 V, 200 W

M = IL2 + IL3
CH 3 = IL2
CH 2 + IL3
5.0 A/div.

t – Time – 1 μs/div

Figure 10.

V_{IN} = 75 V, 200 W

M = IL2 + IL3
CH 3 = IL2
CH 2 + IL3
5.0 A/div.

t – Time – 1 μs/div

Figure 11.

4 Conclusion

The major benefits of interleaving forward converters are reduced input and output capacitor ripple currents. This allows the design to use smaller input and output capacitor banks to meet ripple voltage requirements. By using two output inductors the peak currents in the circuit are reduced by a factor of two which in turn reduces the EMI signature for these designs. Reducing the size of filter capacitance banks will reduce the cost and size of the design. The UCC28221 control device was designed for this application. The UCC28221 has internal start up circuitry that removes the need for a boot strap resistor reducing component count and cost.

5 References

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3. Brian Shafer, *Interleaving Contributes Unique Benefits to Forward Converters and Flyback Converters*, Texas Instrument Power Supply Design Seminar, Topic 4, SEM 1600, 2004

4. *UCC28220/1 Dual Interleave PWM Controller*, Data Sheet, Instruments Literature Number SLUS544, September 2003

5. *UCC28221 200W Evaluation Module (EVM)*, Evaluation Module User's Guide, Texas Instruments Literature Number SLUU173A, December 2003

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