Application Report
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Cell Balancing With the bq77PL900

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ABSTRACT

The bq77PL900 five to ten series cell lithium-ion or lithium-polymer battery protection and AFE IC includes a cell-balancing function. This document describes how to use the cell-balancing feature of the part in a battery pack application. Boosting the current capability of the IC using external FETs is described. The algorithm for balancing in stand-alone mode is described as well as considerations for implementing a host-controlled balancing algorithm which avoids damage to the IC.

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1 Cell Balancing

Cells are usually matched during the manufacturing of a battery pack. Over time, an imbalance in the state of charge may develop between cells and reduce the overall capacity of the pack. Cell balancing that equalizes the cells allows the pack to operate longer.

The bq77PL900 provides a bypass method of balancing. Some of the current which would charge the cell is diverted through a parallel path. Cell balancing operates during on a 50-ms nominal period. Voltage monitoring occurs during approximately 10 ms of this interval, a balancing FET internal to the IC is switched on during the remaining 40 ms of the period to provide a bypass path. The FET is switched off again at the end of the balancing interval to measure the cell voltage.

2 Description of Internal Cell-Balancing Circuit

Cell balancing of a particular cell consists of enabling an NMOS switch across the cell. The configuration effectively looks like Figure 1(a) and Figure 1(b).

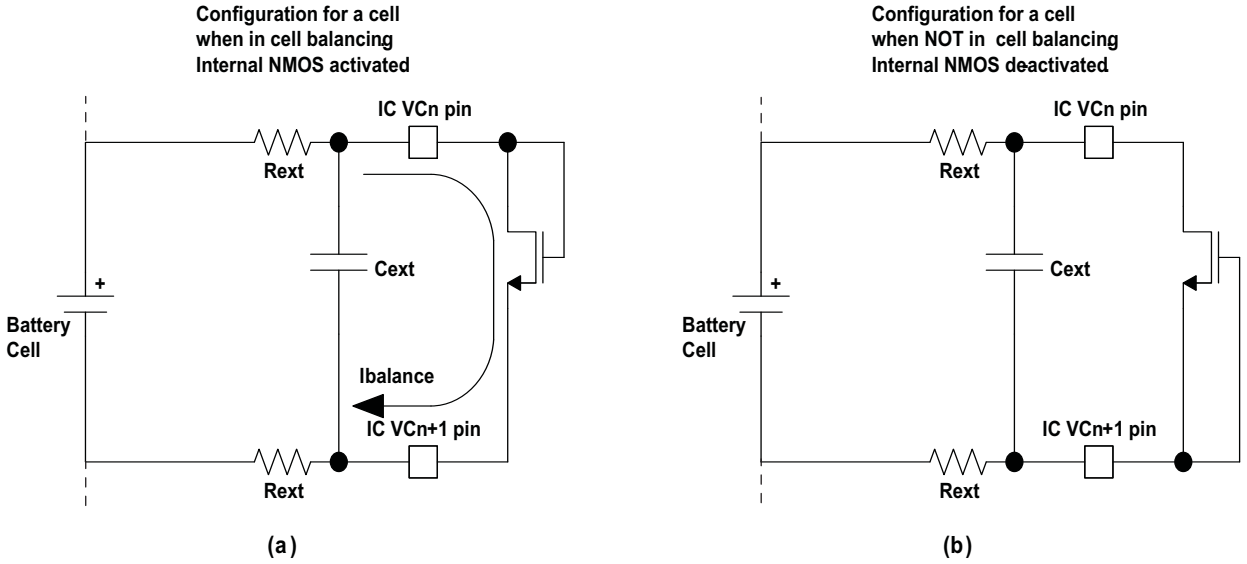

Figure 1. Internal Cell-Balancing Circuit

As can be seen by examining the circuit in Figure 1(a), when the cell is enabled for balancing, the gate of the NMOS device is connected to the drain. Because of the threshold voltage (Vt) of the NMOS, a certain amount of voltage across the IC pin Vcn to Vcn+1 is required to activate the NMOS. This limits the external resistor values which can be used, as well as the lowest cell voltage which can effectively be balanced. Figure 1(b) shows the internal NMOS configuration when the NMOS is off (no cell balancing).

2.1 Internal Cell-Balancing Circuit Design

The internal FETs are used for cell balancing through the same RC network used for cell voltage measurement. The cell-balancing current flows through the internal FET. The resistors (Rext as shown in Figure 1) should be in the 400-Ω to 1000-Ω range as indicated in the data sheet. This limits the balancing current available. Cext should be chosen to provide filtering for cell balancing. The time constant of the resulting network must be small enough to allow the cell voltage to stabilize fully during the 10-ms nonbalancing time prior to measurement of the cell voltage. Example values are 500 Ω for Rext and 0.1 µF for Cext.

2.2 External Cell-Balancing Circuit Design

When balancing currents higher than the internal FETs can support are desired, external FETs can be used to provide the cell-balancing current. A higher resistance is used for Rext to provide a sense path to the IC for the cell voltages, and FETs are connected with current-limit resistors. This reduces the current in the internal FET to a bias current used to turn on the external FET. Vgs for the external FET is developed by the bias current across the resistor Rext between the VCn+1 pin and the bottom of the cell. Due to the symmetry of the circuit, the same voltage is developed between the top of the cell and the VCn pin. The balance current flows through a series current-limit resistor and the external FET drain. The circuit for this looks like Figure 2.

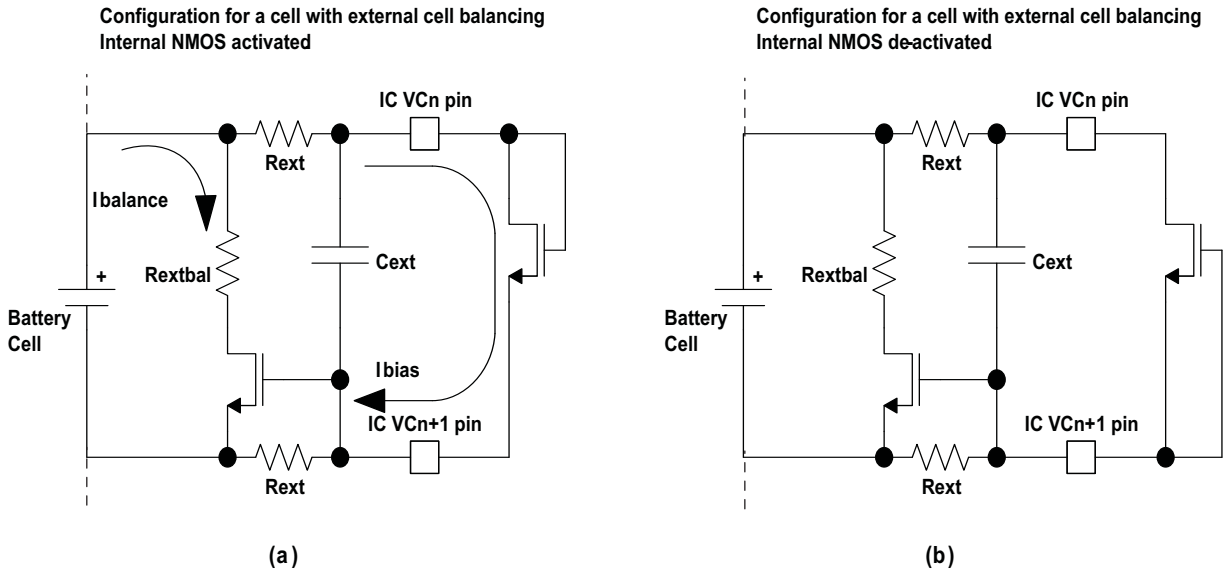

Figure 2. External Cell-Balancing Circuit

The external NMOS requires a certain amount of Vgs (typically approximately 1 V to 1.5 V). The internal NMOS requires approximately 1.25 V to 1.5 V (depending on the values of the external resistors selected). Thus, the minimum cell voltage which activates the external and internal NMOS devices effectively is approximately 2 × 1 V + 1.25 V = 3.25 V. This can be as high as 2 × 1.5 V + 1.5 V = 4.5 V if the external NMOS has a high Vgs, and the internal NMOS is required to drive a large current due to lower external resistor values.

The nominal current versus voltage of the internal NMOS device at –40°C, 25°C, and 140°C junction temperatures is shown in Figure 3.

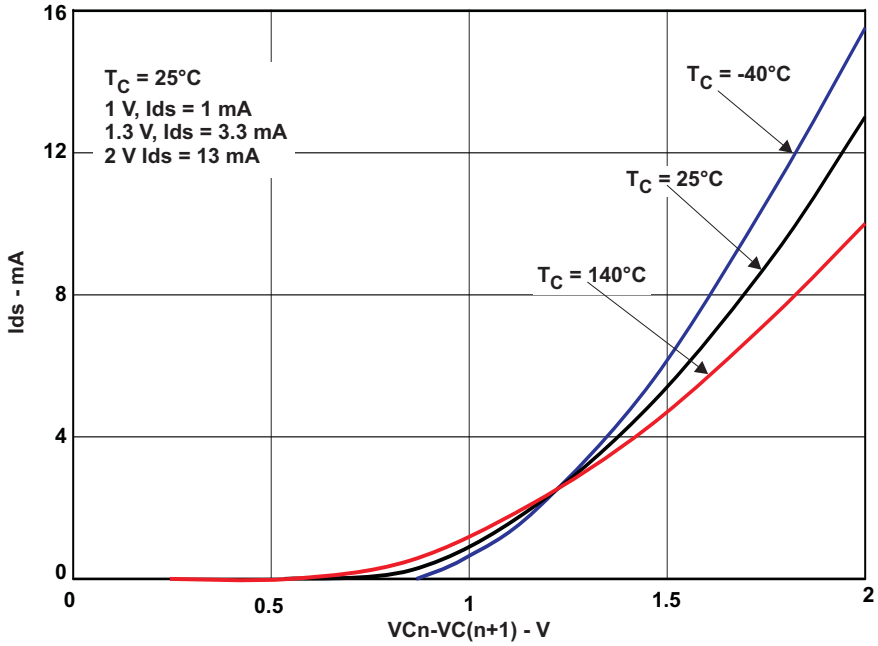

Figure 3. Internal FET Characteristic

The selection of the external NMOS to give the proper Vt and driving Vgs, as well as the values of the external resistors, requires some attention to ensure achieving the desired cell balancing. The external resistors should be large enough to reduce the bias current to minimize the voltage across the internal

FET and maximize the voltage to drive the external FET Vgs. The external FET should have a low threshold voltage and be able to sustain the desired drain current at the available Vgs. The external balance resistor should be sized to limit the balance current and handle the power dissipated. Example values might be 10 kΩ for the cell monitor resistors, 0.01 µF for Cext, 1/2 of a Si1034X for Qext, and 100 Ω for the balance resistor. The external balancing components must be located to keep dissipated heat away from sensitive circuits.

3 Stand-alone Balancing Algorithm

In stand-alone mode, cell balancing is controlled using the CBEN EEPROM bit, bit 7 in the OCD_CFG register (0x09). When CBEN is 1, cell balancing is enabled; when 0, cell balancing is disabled.

When cell balancing is enabled and a cell reaches the overvoltage threshold, the balancing mechanism works to equalize the cell voltages at the overvoltage threshold as described in the data sheet. Balancing operates on the 50-ms interval previously described, alternating sampling the voltage and enabling the balancing FET. When the cell voltage drops below the overvoltage hysteresis threshold, cell balancing stops.

If several cells are allowed to cell balance at the same time, it is possible to exceed the voltage rating across one or more of the internal NMOS devices. The Vcn-to-Vcn+1 voltage has a low absolute maximum voltage. To keep this voltage from being exceeded, the cell balancing is accomplished by preventing too many cells from going into balancing at the same time.

Note: In the examples that follow, cells are numbered from lowest voltage to highest voltage as 0 to 9. This corresponds to the CELL_BALANCE register bit number for the lowest eight cells, not to the CBALn bit name. Be aware of the notation and other possible cell-numbering conventions.

In stand-alone mode, the particular cells to be balanced are selected based on *no-adjacent-cell* and *no-every-other-cell* exclusions. For example, if all cells are in overvoltage (OV) at the same time, only cells 0,3,6,and 9 are balanced. Once these cells are brought back to a non-OV condition, then cells 1,4,and 7 are balanced. Once these cells are non-OV, then cells 2,5,and 8 are balanced. This prevents several adjacent cells from creating an overvoltage stress condition on a cell which is not balancing. The balancing always starts with the lowest numbered cell possible and progresses upward.

Table 1 shows various configurations of OV and cell balancing in stand-alone mode (and recommended for host mode).

Table 1. Stand-alone Balancing Algorithm

Cell No.	Cells OV	First Cells Balanced	Second Set Balanced	Third Set Balanced		Cell No.	Cells OV	First Cells Balanced	Second Set Balanced	Third Set Balanced
9	X	X				9	X	X		
8	X			X		8	X		X	
7	X		X			7				
6	X	X				6	X	X		
5	X			X		5	X		X	
4	X		X			4				
3	X	X				3	X	X		
2	X			X		2	X		X	
1	X		X			1				
0	X	X				0	X	X		

Table 1. Stand-alone Balancing Algorithm (continued)

Cell No.	Cells OV	First Cells Balanced	Second Set Balanced	Third Set Balanced		Cell No.	Cells OV	First Cells Balanced	Second Set Balanced	Third Set Balanced
9						9				
8						8	X			X
7						7	X		X	
6						6	X	X		
5						5				
4						4				
3	X	X				3	X			X
2	X			X		2	X		X	
1	X		X			1	X	X		
0	X	X				0				
9	X	X				9	X	X		
8	X			X		8	X		X	
7	X		X			7	X			X
6	X	X				6	X	X		
5						5	X		X	
4						4				
3						3	X	X		
2						2				
1						1	X		X	
0						0	X	X		

As an example of a cell-balancing configuration which would create internal overvoltage stress on the IC, assume the following conditions of cells: cells 0,1,2,and 3 are cell-balancing, cell 4 is not balancing, cells 5,6,7,and 8 are balancing, and cell 9 is not balancing. Also assume that each battery cell is at 4.2 V. With 1-kΩ external resistors, the following voltage conditions exist: the internal NMOS devices that are on would have about 1.5-V drop. The voltages are distributed as shown in the diagram in Figure 4.

As can be seen from Figure 4, if adjacent cells are allowed to be balanced, overvoltage stress occurs on some of the IC cell input pins, causing damage to the internal NMOS device. If external cell balance FETs are used, the voltages may exceed the maximum Vgs of some low-threshold voltage parts. Resulting voltages on IC inputs for cells 4 and 9 are shown in Table 2 for some voltage-resistance combinations.

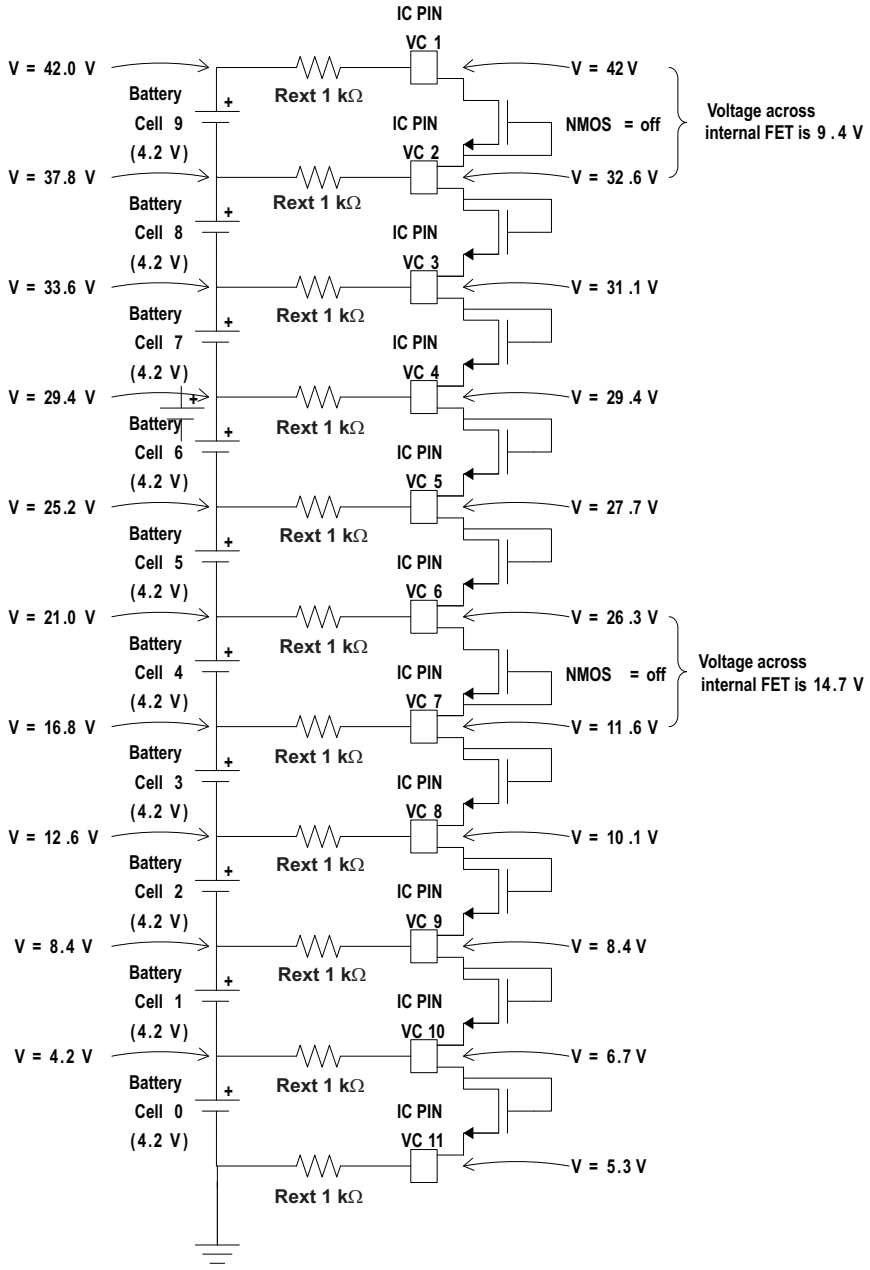

Figure 4. Improper Cell-Balancing Configuration Which Results in Damage to the IC

Table 2. Damaging Input Voltages With Improper Cell Balancing (0,1,2,3,5,6,7,8 balancing)

CELL VOLTAGE (all cells)	CELL SENSE RESISTOR, Rext (Ω)	VOLTAGE at IC VC1–VC2	VOLTAGE at IC VC6–VC7
4.2	1K	9.4	14.7
4.5	1K	10.26	16.02
4.2	10K	10.65	17.11
4.5	10K	11.53	18.56

Figure 5 shows an example of a condition where all cells are OV but a proper cell-balance configuration is applied. In this case, cells 0,3,6,and 9 are in cell balance. Table 3 shows voltages imposed on the nonbalancing cell IC pins for several voltage-resistance conditions.

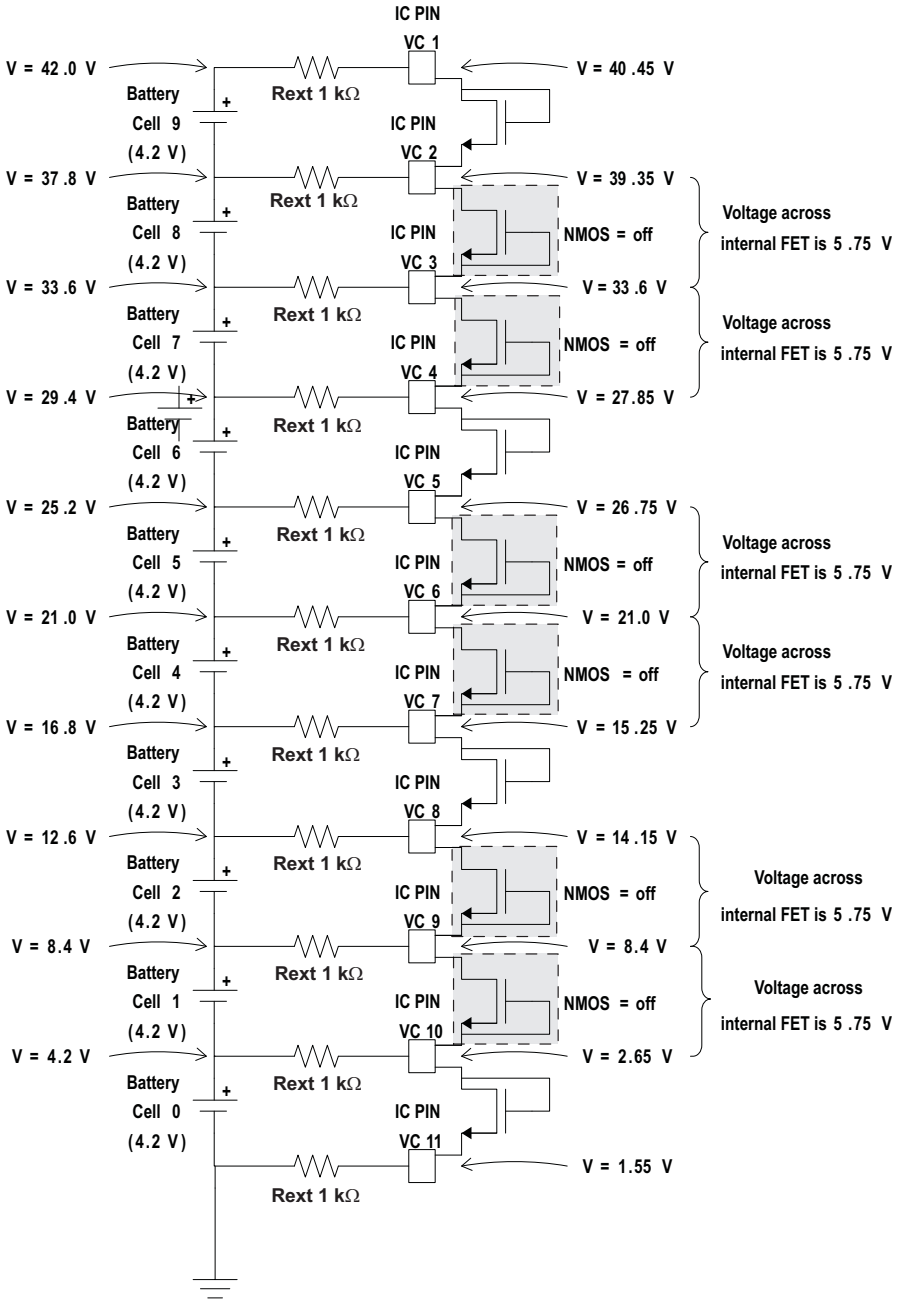

Figure 5. Proper Cell-Balancing Configuration Which Avoids Damage to the IC

Table 3. Example Cell Voltages With Proper Balancing

CELL VOLTAGE (All Cells)	CELL SENSE RESISTOR, Rext (Ω)	VOLTAGE AT NONBALANCING IC CELL INPUTS
4.2	1K	5.75
4.5	1K	6.19
4.2	10K	5.90
4.5	10K	6.34

4 Considerations for a Host-Balancing Algorithm

CAUTION

Improper setting of the cell-balancing control bits may damage the IC.

In host mode, the system designer has more flexibility in the cell-balancing function but must understand its operation to provide an effective balancing function safe for the IC. The automatic bit protections described for stand-alone operation are not used and the operator must take care to avoid damage. Cells can be balanced at any time, regardless of the setting of CBEN. The controller must determine when cells are to be balanced and set the proper *CBALn* bits in registers 0x03 and 0x04. The controller must clear the bits when balancing must be stopped.

Because cells can be balanced at any time in host mode, the controller can read cell voltages and determine when to begin and end balancing. This allows implementation of a balancing scheme which could operate through much of the charge time and not have to reach the overvoltage limit set in the IC. This allows a shorter balancing operation as well as balancing for applications or cells which do not operate to that voltage limit.

When the cell voltages are above the level where the application balancing circuit will work, appropriate bits can be set to balance those cells according to the implemented algorithm. Balancing one cell at a time is safe, but may increase the time to balance the pack. The stand-alone algorithm previously described is a good example of which cells to balance. Follow the recommendations described in the *Stand-alone Cell Balancing* section of this document to avoid damage to the IC.

Zener diodes may be used to prevent overvoltage to the IC pins. If external cell balancing is used, the designer must confirm that any cell balance patterns used do not exceed the Vgs of the external FETs. Additionally, if balancing is enabled on adjacent cells with external balancing FETs, approximately equal current flows through the internal cell balance FETs and little current flows in the Rext between the cells. Thus, only the lower cell's external FET may turn on.

Because the balancing is a drain balance, balancing is not recommended during discharge because it is a loss of charge. The system designer must specifically stop the balancing by clearing the balancing bits. If the design uses the charge FETs or has control of the charger, charging can be interrupted while allowing the balancing to continue on the selected cells. The controller needs to stop the balancing at a suitable threshold and continue charge, or end charge and balancing if the last cells have been balanced and the charge completed. Again, the host must turn off the cell balance by clearing the bits, or the balance circuit will drain the enabled cells.

Board test must be considered as well as normal operation. If any test patterns are written to the cell-balance registers, these must exclude any patterns that can cause damaging voltages to the IC. During normal application operation, periodic test patterns cause a drain on the selected cells and are to be avoided.

In summary, a good list of things to consider in the design of host balancing includes:

- Balance during charge
- Stop balancing during discharge
- Balance when cell voltages are high enough to allow the application circuit to work properly
- Design the algorithm to prevent damage to the cells during any allowed combination
  - Do not simultaneously balance adjacent cells
  - Do not simultaneously balance cells on opposite sides of a cell
- Do not allow register test patterns on cell-balancing bits which could cause damage.

5 Additional Timing Information

Cell balancing always begins at the end of a sampling of the cell voltages. In stand-alone mode, the balancing operates for the full 40-ms balance window. In host mode, if the set of cells to be balanced is changed by the host, the cells being balanced change immediately if commanded during the 40-ms balance window. If the host changes the cells to be balanced during the 10-ms nonbalance time, the IC does not begin balancing the new cells selected until at the end of the 10-ms window.

If a transition occurs from stand-alone mode to host mode or from host mode to stand-alone mode during the 40 ms when the IC is in cell balance, the set of cells changes immediately as determined by the host or by the IC state machine. If the transition from stand-alone mode to host mode or from host mode to stand-alone mode occurs during the 10-ms nonbalancing window, the new cell-balancing configuration does not begin until at the end of the 10-ms time window.

A special condition for transition from host mode to stand-alone mode or from stand-alone mode to host mode occurs if while in the first mode no cells were selected for balancing. For this configuration, when changed from one mode to another mode (if within the 40-ms balancing window), the cell balancing does not begin until the 40-ms window has completed, a 10-ms nonbalancing window has occurred, and then the normal balancing begins. The practical effect of this is that a delay of 50 ms or less occurs after a transition from host to stand-alone or stand-alone to host before cell-balancing changes will occur, but there should never be more than a 50-ms delay.

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