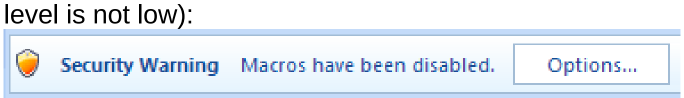
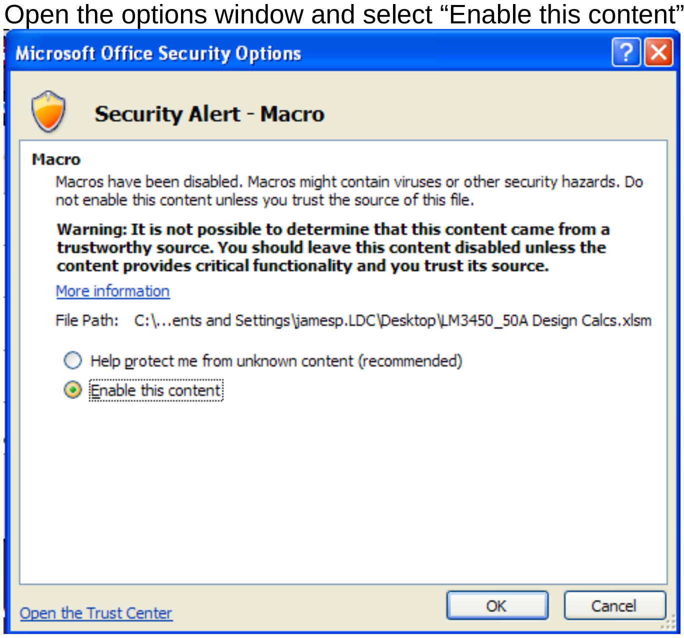
LM3450/LM3450A Design Calculator Instruction Guide Rev 1.0

SETUP INSTRUCTIONS

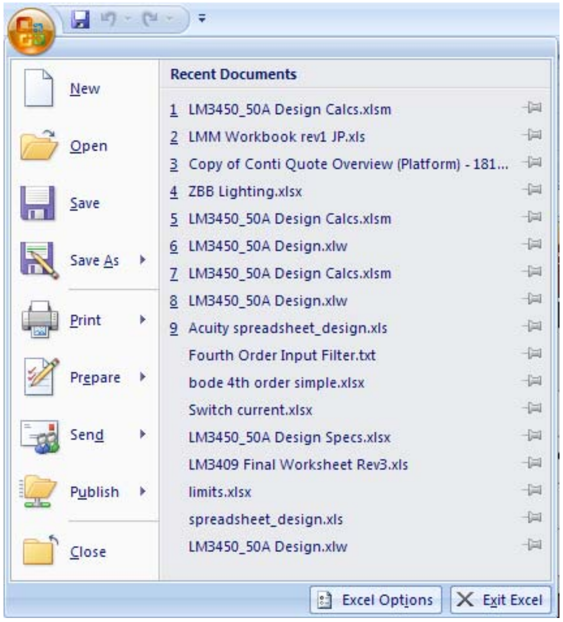
1. Download Macro-enabled Excel Workbook "LM3450_50A Design Calcs.xlsm"
2. Open Workbook using Microsoft Excel (.xlsm files only supported in 2007 and 2010)
3. If Excel prompts the user about macros (will happen if macro security level is not low):



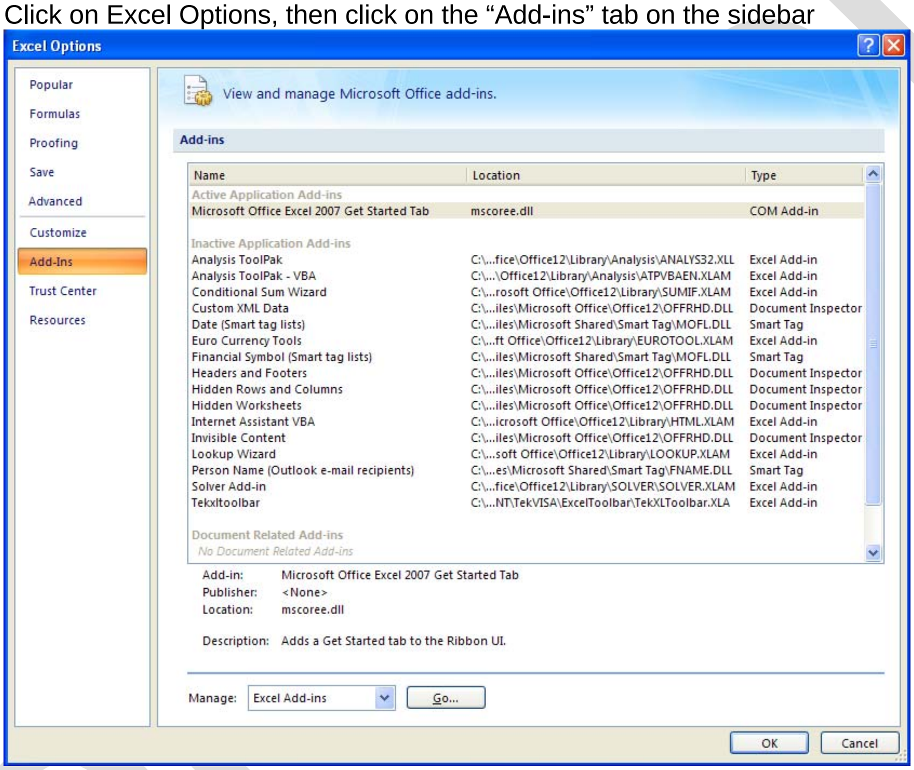
Open the options window and select "Enable this content"



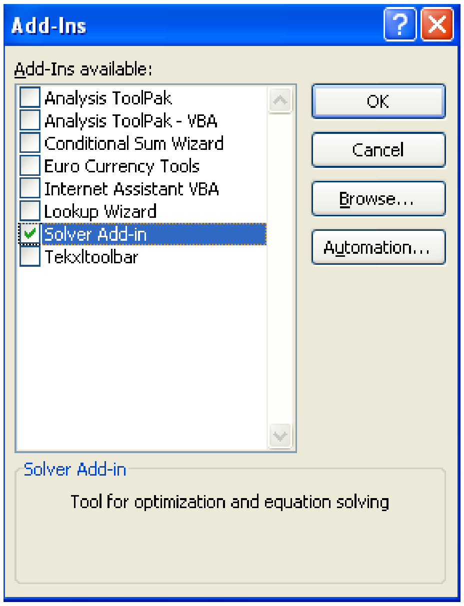
4. Lastly, the "Solver" add-in needs to be enabled: Open the Start Button



Click on Excel Options, then click on the “Add-ins” tab on the sidebar



Click on the Go button at the bottom to “Manage Excel Add-ins”



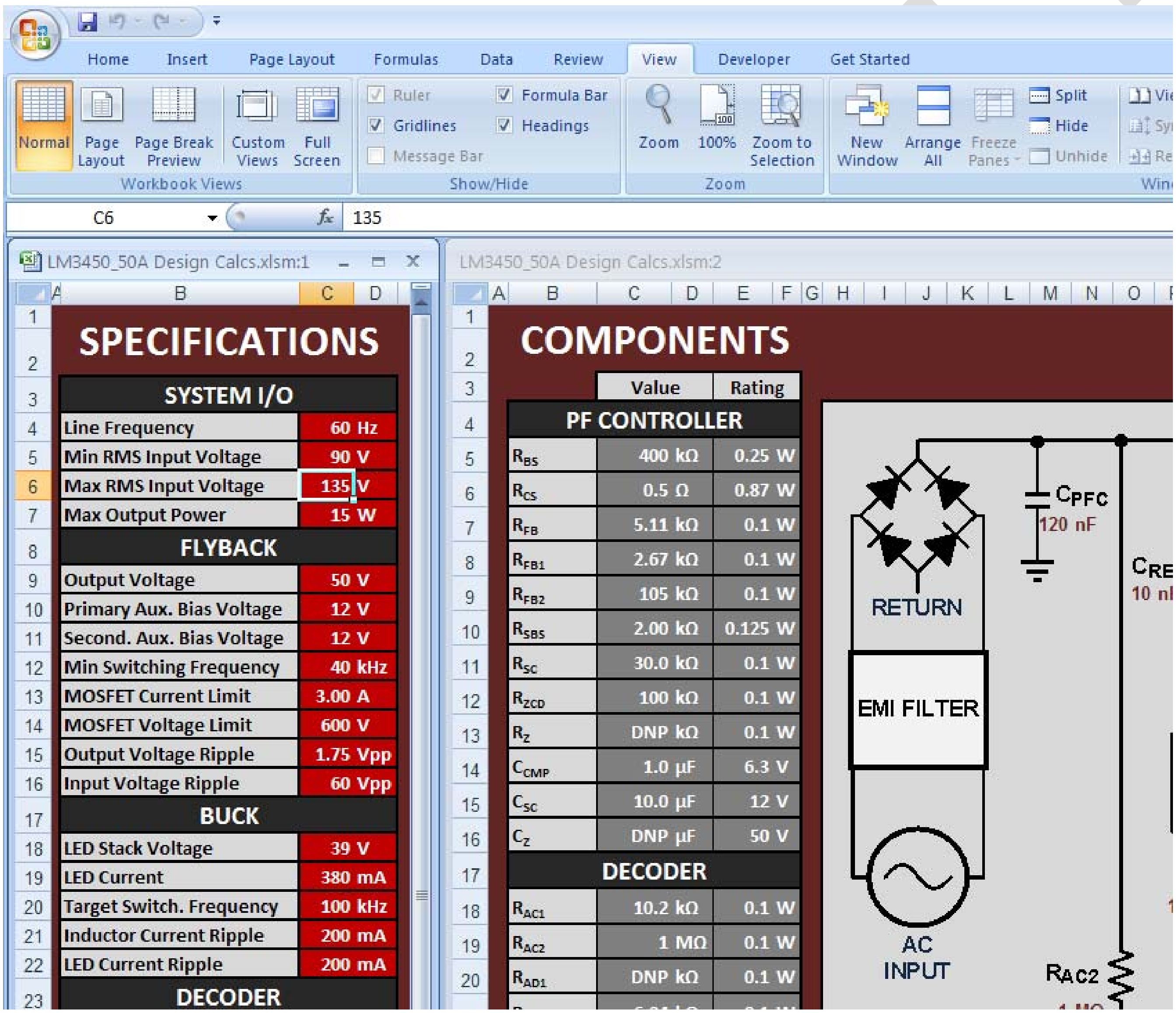
Check the “Solver Add-in” box and click OK.

GENERAL GUIDELINE FOR USING THE SPREADSHEET

All red cells are inputs that are either straight numerical inputs or selectable form a drop-down menu. All other cells are calculations, plots, etc…. and are not editable.

Start the design at the leftmost “Readme” tab to understand the design flow. Then work your way sequentially from left to right across the tabs (i.e. Specs, Xformer, Flyback, PFC, Buck, EMI, and then Dimming)

You might find it helpful to open a copy of the workbook with the Specs tab open all the time. This can be done by selecting the “View” tab and clicking on “New Window”. Then you can position the windows as shown below with the Specs worksheet open in one copy (small on the side) and the second copy can be used to work through each worksheet. Changes made to either copy will be save-able when you close.



OUTLINE OF EACH WORKSHEET

1. **Specs:** This worksheet is fairly straight-forward. It only contains inputs and very basic operating point calculations. These inputs are used throughout the worksheet therefore keeping a copy open at all times is useful as mentioned previously. Here is a summary of the user inputs:
   a. System I/O
      i. Line Frequency – AC frequency of 50 or 60 Hz (regional spec)
      ii. Min RMS Input Voltage – AC voltage range minimum
      iii. Max RMS Input Voltage – AC voltage range maximum
      iv. Max Output Power – max is used mainly for transformer design
   b. Flyback Converter
      i. Output Voltage – regulated output of flyback, serves as input to buck stage
      ii. Primary Aux. Bias Voltage – desired voltage for primary bias supply
      iii. Secondary Aux. Bias Voltage – desired voltage for secondary bias supply
      iv. Min Switching Frequency – min is used for sizing inductance on transformer
      v. MOSFET Current Limit – desired current limit to protect FET (not necessarily FET rating)
      vi. MOSFET Voltage Limit – rated max voltage for chosen FET
      vii. Output Voltage Ripple – desired peak-to-peak ripple voltage at flyback output
      viii. Input Voltage Ripple – desired peak-to-peak ripple voltage on PFC cap
   c. Buck Converter
      i. LED Stack Voltage – nominal output voltage of stack
      ii. LED Current – regulated output current
      iii. Target Switching Frequency – desired frequency at nominal conditions
      iv. Inductor Current Ripple – desired peak-to-peak ripple current in inductor
      v. LED Current Ripple – desired peak-to-peak ripple current in LED
   d. Dimming Decoder
      i. FLT1/FLT2 Frequency – yields effective speed of dimming translation (2-10Hz is range)
   e. PassFET
      i. Max Power Dissipation – power capability of chosen passFET package (DPAK~1W)

2. **Xformer:** The transformer design is highly iterative, however, this worksheet is meant to limit to the amount of iterations and focus the designers' efforts. Here's a basic design flow:
   a. Enter the desired "Primary to Secondary Turns Ratio that keeps the "Reflected Voltage" below the stated inequality. This, along with the previously entered specifications, will calculate the "Primary Inductance" necessary:

Primary to Secondary Turns Ratio	Reflected Voltage	Primary Inductance
n	Vr < 139	Lp
2 : 1	100 V	1016 uH

   b. Choose the desired "Core Type/Size" from the drop-down menu and the "Chosen Core Information" will auto-populate:

CHOSEN CORE INFORMATION							
Core Type/Size	AL value	Ploss_density	Ve	Ae	Wa	Ww	MLT
E25/13/7 (EF25)	160 nH/t^2	100 kW/m^3	2990 mm^3	52.0 mm^2	63.3 mm^2	15.5 mm	52.8 mm

c. Change the AL value until the desired maximum flux density “Bmax” is achieved without violating the stated inequality. Bmax typically is between 300mT and 350mT for best optimization.

Bmax < 400
324 mT

d. Choose the desired safety configuration by selecting the “Chosen Insulation”. Typical systems that require a Class 2 output have “Single” Insulation on the Primary and “Reinforced” Insulation on the Secondary:

CHOSEN INSULATION	
Primary	Secondary
Single	Reinforced

e. Choose the desired wire gauge for each winding from the drop-down menus ("Awp" is primary, "Awpa" is primary auxiliary bias, etc…). Note that the secondary bias "Awps" is tapped from the main secondary winding "Aws" therefore "None" is selected. The "Insulated" winding area is a square equal to the max OD dimension squared. This is obviously a conservative measurement to ensure a good wind can be achieved. The "Bare" area is the nominal round copper area for loss calculations.

CHOSEN WIRE INFORMATION *(Insulated is Square, Bare is Circular)*				
Awp	Aws	Awpa	Awps	
22S	24R	30S	None	
0.456489 mm^2	0.546328 mm^2	0.076651 mm^2	0.000000 mm^2	*Insulated*
0.324339 mm^2	0.204715 mm^2	0.050671 mm^2	0.000000 mm^2	*Bare*

f. The "Fill Factor" should then be checked to ensure the transformer is manufacturable (<1 is imperative, but really the number should be <0.7 in many cases to provide headroom for margin tape and wrapper tape). This is by no means an exact calculation and the designer will need to experiment with this factor in real designs to determine what is realistically manufacturable for a given core and voltage rating. At the same time, the # of layers should be observed for each winding to understand the construction details of this design. The # of layers for the primary should be near to, but less than, an even integer value if possible. The # of layers of the secondary should be near to, but less than any integer value if possible. The primary aux # of layers doesn't matter too much in this design. In general, iterating wire size is inevitable.

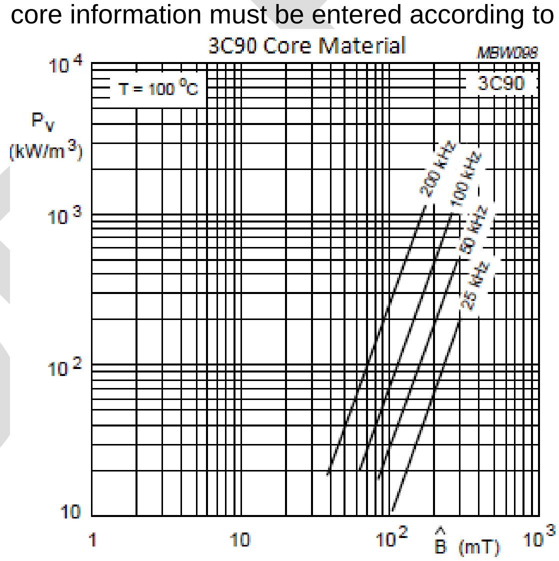
CALCULATED TRANSFORMER WIRE INFORMATION							
Primary Fill	Secondary Fill	Primary Aux. Fill	Sec. Aux. Fill	Fill Factor	# Primary layers	# Second. Layers	# P_aux layers
36.38 mm^2	21.77 mm^2	0.73 mm^2	0.00 mm^2	0.93	3.48	1.91	0.17

g. Finally, the losses will be calculated as follows:

CALCULATED LOSSES					
Bmax < 400	deltaB (B^)	Prim. Cu Loss	Sec. Cu Loss	Total Cu Loss	Core Loss
324 mT	162 mT	0.06 W	0.18 W	0.24 W	0.30 W

i. Copper loss is calculated in the primary as "Prim. Cu Loss" and secondary as "Sec. Cu Loss". Both are added together to get "Total Cu Loss". In general the designer wants to balance the losses between the two sides so during iteration of wire size, this factor should be monitored as well.

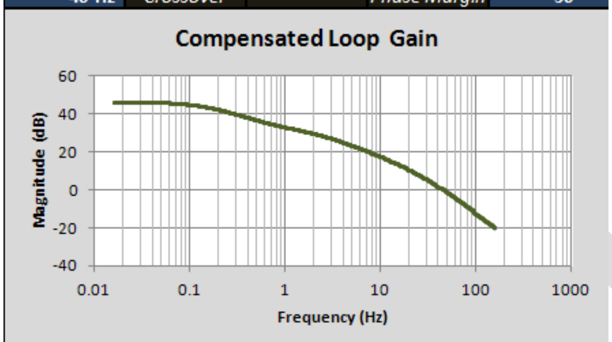
ii. Core loss is calculated according to the min. switching frequency and peak flux density "deltaB". To get the calculation correct the "Ploss_density" from the core information must be entered according to the chart below:

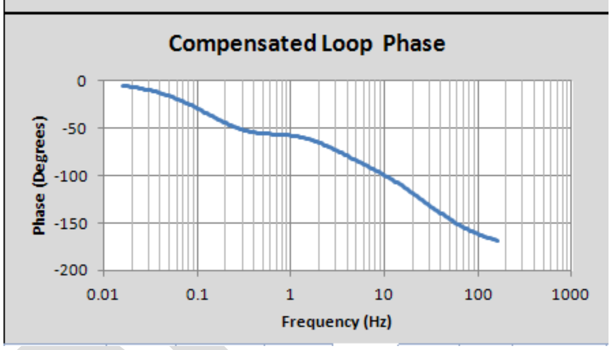


3. **Flyback**: There are no inputs on this worksheet. It is simply a component calculator with a schematic that auto-populates the values.

4. **PFC**: The inputs on this worksheet are fairly simple. The "Chosen MOSFET" and "Chosen Diode" are filled in to calculate the losses shown under "Power Calculations". If one of the red input cells turns yellow, it means that a calculated maximum operating point exceeds the max rating of the chosen device. The "Control Loop Components" are inputs to set the bandwidth and phase margin of the control loop. As a general rule of thumb, the "Ccomp" and "Csc" values can be left alone and only the "Rsc" value is iterated to give the desired phase margin and crossover frequency. For these type of dimming systems an aggressive PFC bandwidth (>15Hz) is usually desired for good transient performance but 70Hz is the maximum suggested bandwidth that can be obtained without saturating the error amplifier due to excessive 120Hz ripple on COMP. Note that PFC will decrease as bandwidth increases.

CONTROL LOOP COMPONENT CHOICES				
Ccomp	Csc	Rsc	Cz	Rz
1.0 µF	10.0 µF	20.0 kΩ	DNP µF	DNP kΩ
CONTROL LOOP CALCULATIONS				
fp1	fp2	fp3	fz1	Dcgain
2.03 Hz	0.15 Hz	31.85 Hz	0.80 Hz	46 dB
46 Hz	Crossover		Phase Margin	36 °





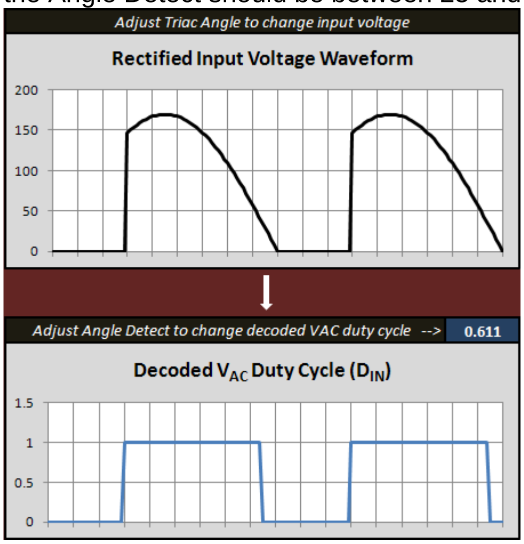
5. **Buck:** This is also a simple component calculator however the chosen device inputs are on the same worksheet. Again, the red input cells will turn yellow if a maximum rating is violated.

6. **EMI:** This worksheet uses the cumulative inputs and calculations of the power stage design to derive an appropriate differential mode (DM) filter for the input of the system. It includes some common-mode (CM) configurations also to start the designer at a reasonable design. In general, though, the CM filtering is also provided by controlling parasitics and edge rates which are not handled in this worksheet. In addition it provides a good starting place for the damping and inrush circuits necessary for phase dimmable systems. The designer WILL need to iterate this portion in the lab to

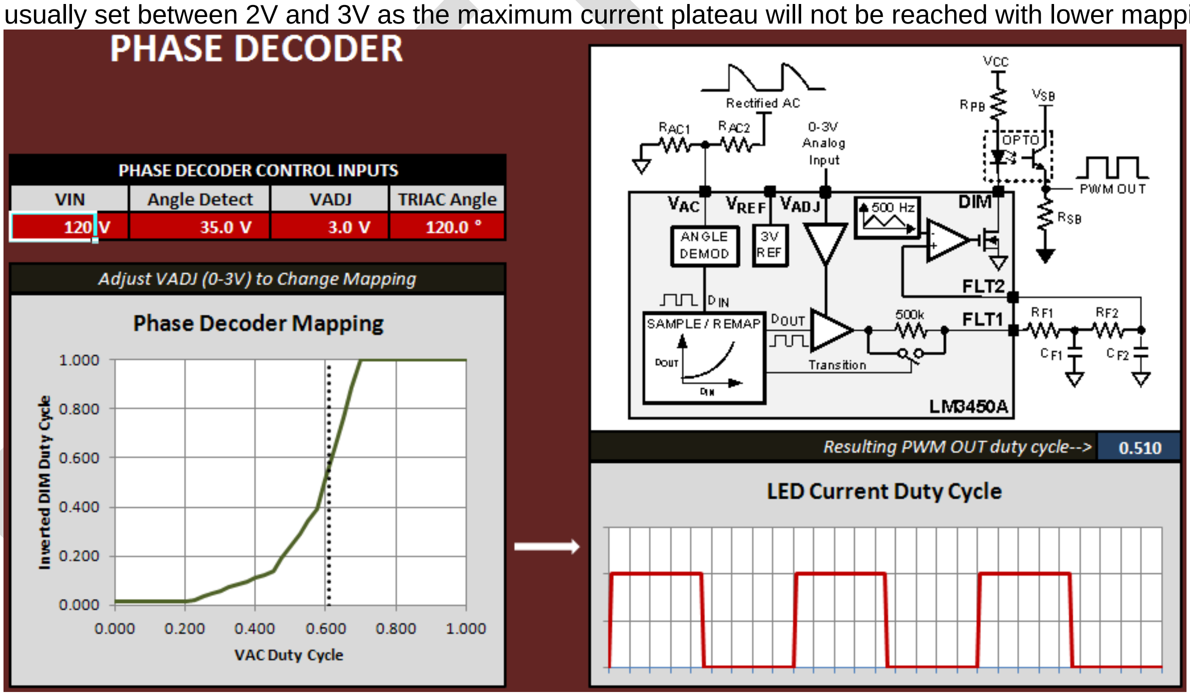
validate operation with a range of dimmers. Again, there are some inputs for the chosen filter components and bridge diodes which behave similar to the other component calculator worksheets.

7. **Dimming:** This worksheet is intended to help the designer understand the phase dimming decoder and dynamic hold circuit that is unique to the device. All plots (excluding the “Phase Decoder Mapping” which is simply a transfer function between the digital block input and digital block output) represent the time domain waveforms associated with the device.

Starting at the top, the user can set the “Phase Decoder Control Inputs” to see how different nominal input voltages (VIN), and TRIAC conduction angles will affect the rectified input voltage waveform. Then the “Decoded VAC Duty Cycle” can be further adjusted by changing the “Angle Detect” Input. In general, the Angle Detect should be between 25 and 50V for best detection:

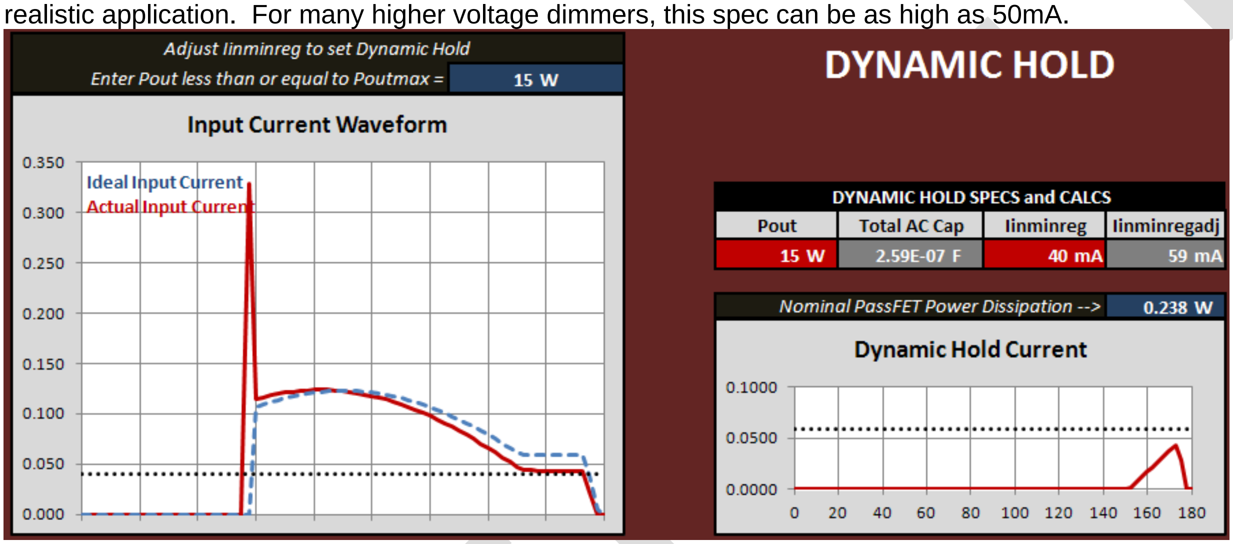


Then the user can change “VADJ” to adjust the mapping from the decoded VAC duty cycle to the DIM output and ultimately the inverted LED dimming duty cycle on the secondary. The VADJ voltage is usually set between 2V and 3V as the maximum current plateau will not be reached with lower mappings:



The lower section of the dimming worksheet shows the dynamic hold functionality. It is difficult for the designer to understand the dynamic hold without simulating closed loop functionality of the converter. The solver (that was enabled in the setup) provides and numerical solution for the closed loop operating point of the system. In this way, the worksheet can roughly calculate the resulting input current waveform in order to determine the added hold current as a function of time. This is critical to understand as it effects the steady-state PassFET power dissipation (shown in blue). If the power dissipation exceeds the specified power rating of the package, the cell will turn yellow. This dynamic hold simulation also allows the user to see the advantages and disadvantages of different mappings and operating points.

The output power for this simulation can be adjusted by the user and is valid as long as it is below the max output power from the overall spec (shown again on this workbook in blue). The designer can then also input the desired minimum regulated input current which should be specified by looking at the worst-case dimmer spec from the range of targeted dimmers. This should always be greater than 25mA for any realistic application. For many higher voltage dimmers, this spec can be as high as 50mA.



Note that the actual input current models the total AC capacitance derived from the EMI worksheet (first filter capacitor plus associated damping capacitance). The inrush current can be seen in the actual input current plot (albeit at low resolution on this plot….actual value will go even higher!). This capacitance is used to derive the actual necessary minimum regulated current (Iinminregadj) for a given desired Iinminreg set by the user. This Iinminregadj value is used to size the resistor from ISEN to GND.

FINAL THOUGHTS

This is a very intensive worksheet. It is meant to make a fairly complex design much quicker, however there is a learning curve and as in any AC-DC converter design. There will always be iterations necessary. After some time working with the spreadsheet, the designer should be able to quickly produce a good first rev design using the LM3450/A which should greatly reduce the design time and overall time to market.

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