

LLC Design for UCC29950

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Power Stage

ABSTRACT

First Harmonic Approximation (FHA) is the conventional approach used when analyzing the LLC converter topology. This approach requires a minimum of math to generate a reasonable approximation to the LLC power converter operating characteristic. On the other hand, FHA analysis is less than ideal when designing an LLC power converter to meet 'real world' specifications. One reason is that FHA is accurate when operating close to the resonant frequency, but becomes less accurate as the switching frequency moves away from resonance. Another failing is that FHA analysis results cannot be compared directly with observed waveforms from the physical LLC converter. For example, the FHA characteristic has load expressed in terms of LLC damping or 'Q-factor' while the power stage load is typically expressed in terms of current and voltage.

In an age of powerful computing, it is possible to generate the LLC operating characteristic without the aid of FHA. An LLC operating characteristic based upon this numerical approach has the advantage of accuracy across the whole range of switching frequencies. This operating characteristic can also be related directly to current and voltage waveforms and quantities measured in the physical LLC converter circuit.

The first part of this application note presents a summary of the analysis method used to generate the LLC operating characteristic. Subsequent sections show how the resulting LLC operating characteristic can be used to select the LLC power components needed to achieve a variety of common power supply specification requirements.

An objective of this document is to provide the designer with all the tools needed to select the LLC power components required to meet his/her specification requirement.

The design process outlined here is suitable only for LLC converters with diode rectifiers, or Synchronous Rectifiers (SR) that operate in diode equivalent mode. Use of other Synchronous Rectification methods effectively alter the LLC characteristic in a way that depends upon the particular driver timing employed for the SR switches.

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1 LLC Analysis Method

A typical LLC power converter schematic is presented in [Figure 1](#). The LLC power stage requires three reactive elements (L_r , L_m , and C_r) and a transformer to provide isolation. As shown in [Figure 1](#) it is common to employ the transformer parasitic components of leakage and magnetizing inductance to provide the two LLC inductive elements (L_r and L_m).

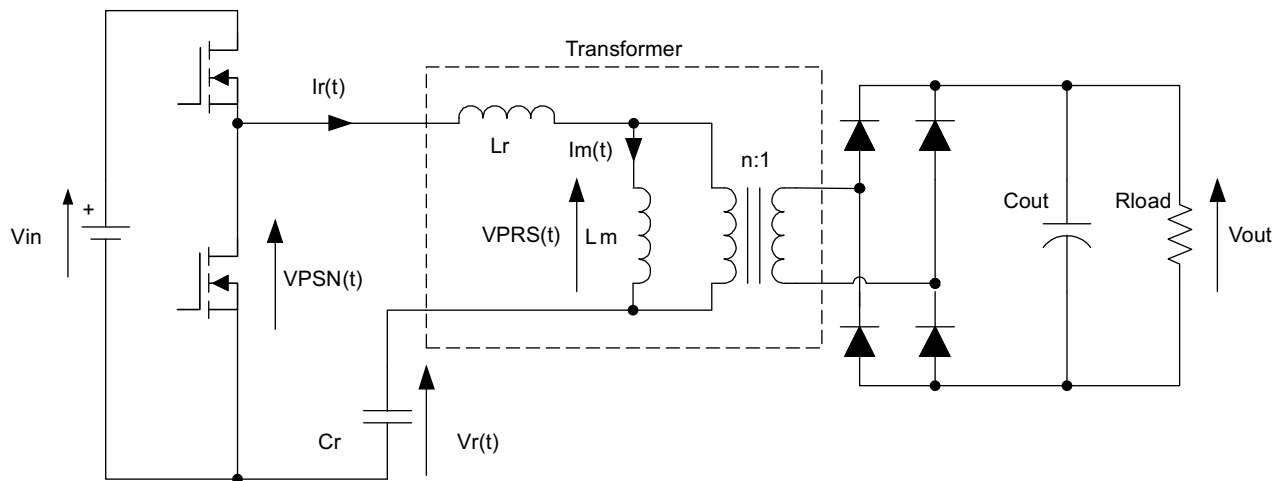


Figure 1. LLC Power Converter Schematic

The secondary side of the LLC power converter can be referred into the primary side to give the simplified equivalent circuit in [Figure 2](#). It is also convenient to normalize the LLC equivalent circuit, to an input voltage of 1, by making the following variable substitutions. Once this is done, we arrive at the normalized equivalent circuit in [Figure 3](#).

$$I_{rn}(\theta) = I_r(\theta) \times \frac{Z_n}{V_{in}}$$

$$I_{mn}(\theta) = I_m(\theta) \times \frac{Z_n}{V_{in}}$$

$$V_{rn}(\theta) = V_r(\theta) \times \frac{1}{V_{in}}$$

$$\theta = \omega \times t$$

$$\omega = \frac{1}{\sqrt{L_r \times C_r}}$$

$$Z_n = \sqrt{\frac{L_r}{C_r}}$$

$$x = \frac{n \times V_{out}}{V_{in}}$$

$$I_m = \frac{L_m}{L_r}$$

(1)

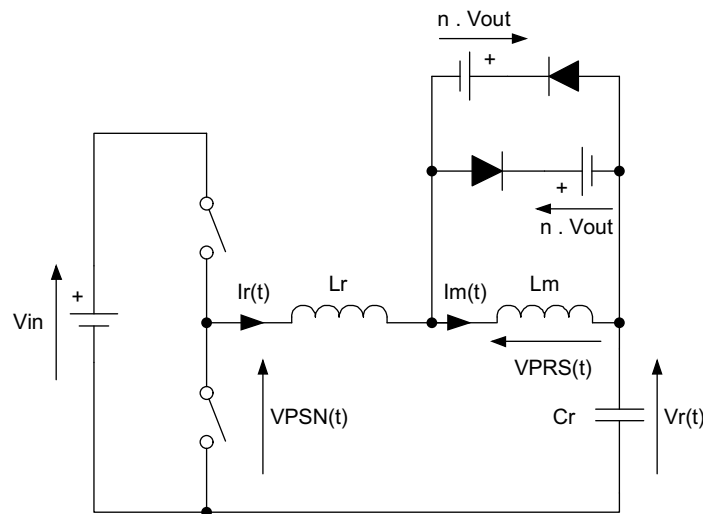


Figure 2. LLC Power Converter Simplified Equivalent Circuit

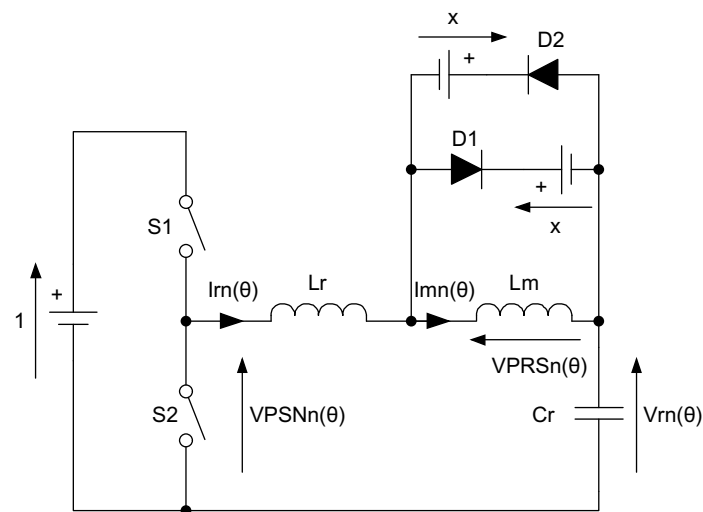


Figure 3. LLC Power Converter Normalized Simplified Equivalent Circuit

Analysis proceeds by breaking down each switching cycle into a series of intervals, based upon the states of the semiconductor devices that are conducting during the interval. There are four possible switch states that include conduction of an output rectifier diode. These are referred to as the S-States. There are two possible switch states that do not include conduction of an output rectifier diode. These are referred to as the P-States.

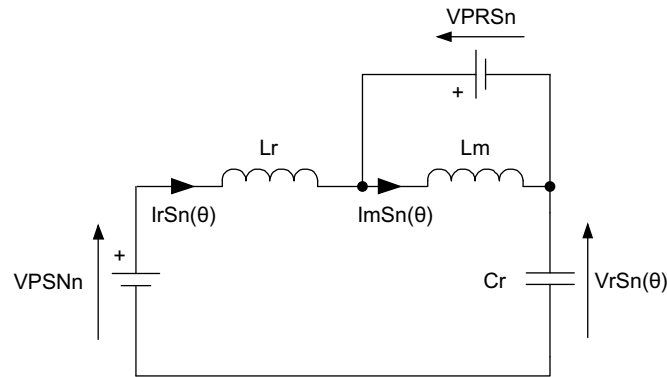


Figure 4. S-States Equivalent Circuit

The equivalent circuit during the S-states is presented in [Figure 4](#). The resonant current and voltage waveforms during one of these states can be expressed as follows:

$$I_{rSn}(\theta) = (V_{PSn} - V_{PRSn} - V_{rS0n}) \times \sin(\theta) + I_{rS0n} \times \cos(\theta) \quad (2)$$

$$I_{mSn}(\theta) = \frac{V_{PRSn} \times \theta}{I_m} + I_{mS0n} \quad (3)$$

$$V_{rSn}(\theta) = (V_{PSn} - V_{PRSn}) - (V_{PSn} - V_{PRSn} - V_{rS0n}) \times \cos(\theta) + I_{rS0n} \times \sin(\theta) \quad (4)$$

I_{rS0n} , I_{mS0n} , and V_{rA0n} are the initial values of resonant current, magnetising current, and resonant capacitor voltage at the start of the current S-State.

The variable V_{PSn} is set to 1 if the upper primary MOSFET (or body diode) is conducting during the current S-State. It is set to 0 if the lower primary MOSFET (or body diode) is conducting in the current S-State.

The variable V_{PRSn} is set to +x if the Primary Referred Secondary voltage is positive (as defined by the arrow in [Figure 4](#)) during the current S_State. It is set to -x if the V_{PRSn} voltage is negative. The following table gives the results for all four possible S-States.

$$\begin{pmatrix} \text{State_No} \\ V_{PSn} \\ V_{PRSn} \end{pmatrix} = \begin{pmatrix} S0 & S1 & S2 & S3 \\ 1 & 1 & 0 & 0 \\ -x & x & x & -x \end{pmatrix}$$

The equivalent circuit during the P-states is presented in [Figure 5](#). The resonant current and voltage waveforms during one of these states can be expressed as follows:

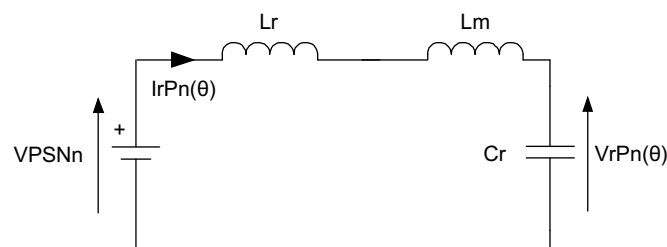


Figure 5. P-States Equivalent Circuit

$$\begin{aligned}
 I_{rPn}(\theta) &= \frac{VPSN_n - VrP0_n}{\sqrt{1+Im}} \times \sin\left(\frac{\theta}{\sqrt{1+Im}}\right) + IrP0_n \times \cos\left(\frac{\theta}{\sqrt{1+Im}}\right) \\
 VrBn(\theta) &= VPSN_n - (VPSN_n - VrP0_n) \times \cos\left(\frac{\theta}{\sqrt{1+Im}}\right) + IrP0_n \times \sqrt{1+Im} \times \sin\left(\frac{\theta}{\sqrt{1+Im}}\right)
 \end{aligned} \tag{5}$$

$$\begin{pmatrix} \text{State_No} \\ VPSN_n \\ VPRS_n \end{pmatrix} = \begin{pmatrix} P0 & P1 \\ 1 & 0 \\ na & na \end{pmatrix}$$

1.1 Steady-State Operating Modes

Over the normal region of interest, the LLC converter can operate in one of four different operating modes. An operating mode is defined as a particular sequence of states over the period of a switching cycle. The four operating modes of interest are listed below:

1. Above Resonance High Power (AH)
2. Above Resonance Low Power (AL)
3. Below Resonance High Power (BH)
4. Below Resonance Low Power (BL)

The sequence of states and corresponding resonant component waveforms for each mode/region are presented in [Section 1.1.1](#) through [Section 1.1.4](#).

1.1.1 Above Resonance High Power (AH)

In this region only the S-States occur. The sequence of states that defines this region is as follows:

$$\begin{pmatrix} \text{State_Seq} \\ \text{VPSNn} \\ \text{VPRSn} \end{pmatrix} = \begin{pmatrix} \text{S0} & \text{S1} & \text{S2} & \text{S3} \\ 1 & 1 & 0 & 0 \\ -x & x & x & -x \end{pmatrix}$$

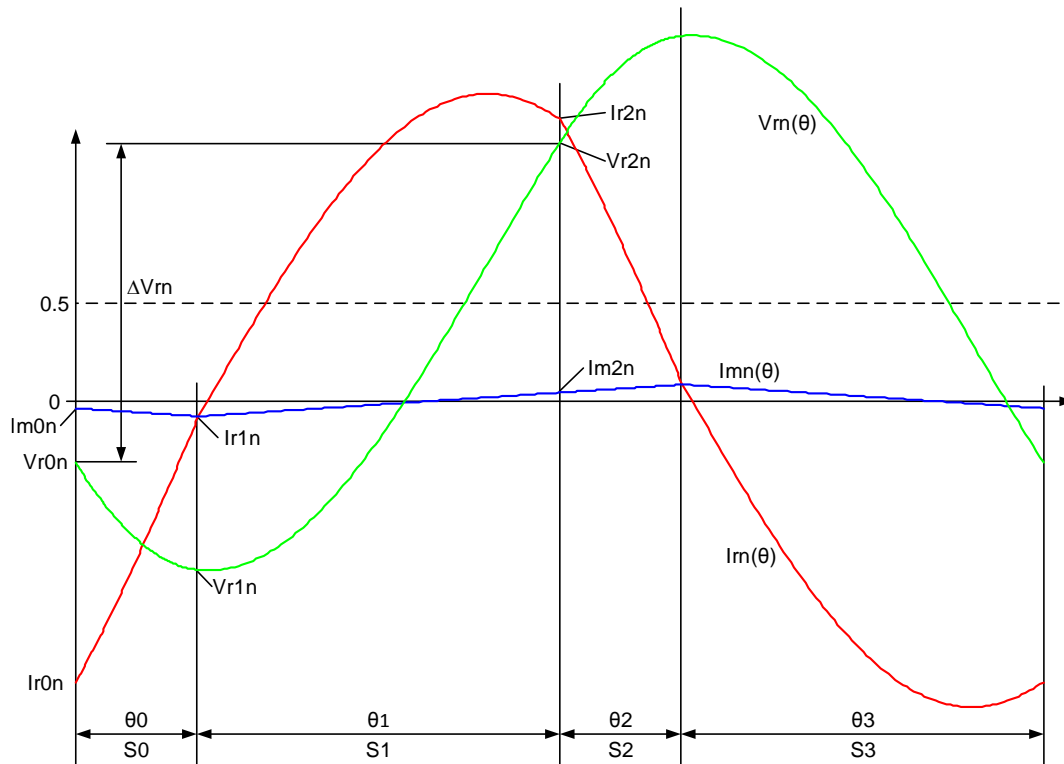


Figure 6. LLC Normalized Resonant Waveforms for AH Region ($x = 0.3$, $I_m = 5$, $\Delta V_{rn} = 1.642$)

1.1.2 Above Resonance, Low Power (AL)

In this region each half-cycle contains three states. The sequence of states that defines this region is as follows:

$$\begin{pmatrix} \text{State_Seq} \\ \text{VPSNn} \\ \text{VPRSn} \end{pmatrix} = \begin{pmatrix} \text{S0} & \text{P0} & \text{S1} & \text{S2} & \text{P1} & \text{S3} \\ 1 & 1 & 1 & 0 & 0 & 0 \\ -x & na & x & x & na & -x \end{pmatrix}$$

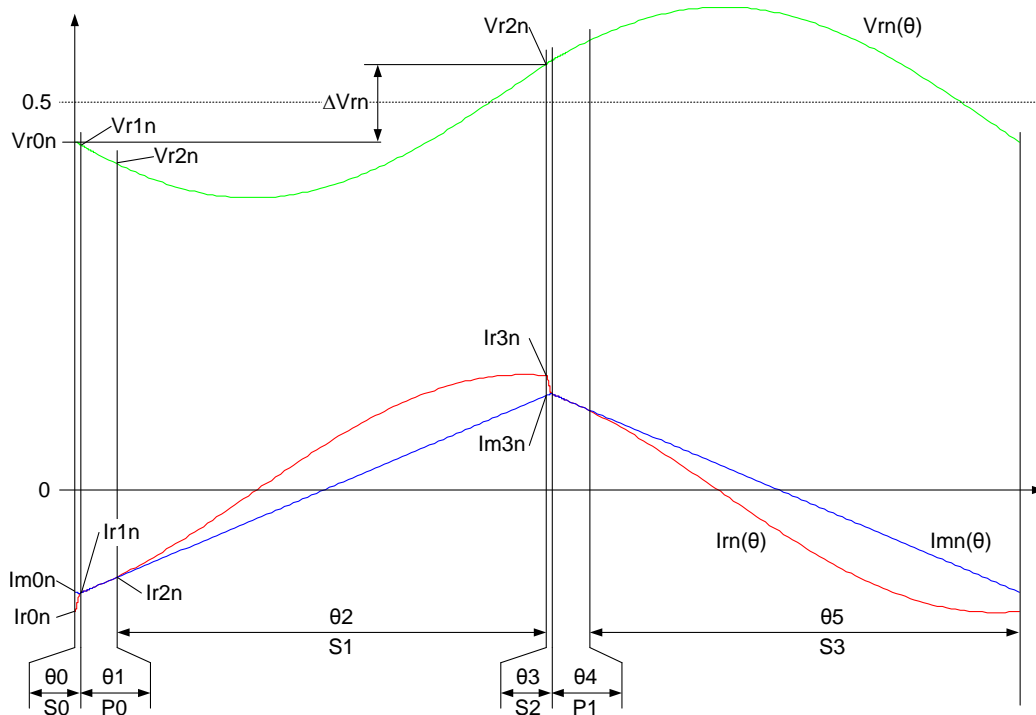


Figure 7. LLC Normalized Resonant Waveforms for AL Region ($x = 0.47$, $I_m = 5$, $\Delta V_{rn} = 0.1$)

1.1.3 Below Resonance High Power (BH)

In this region each half-cycle contains two states. The sequence of states defining this region is as follows:

$$\begin{pmatrix} \text{State_Seq} \\ \text{PSN_n} \\ \text{VPRS_n} \end{pmatrix} = \begin{pmatrix} \text{S1} & \text{P0} & \text{S3} & \text{P1} \\ 1 & 1 & 0 & 0 \\ x & na & -x & na \end{pmatrix}$$

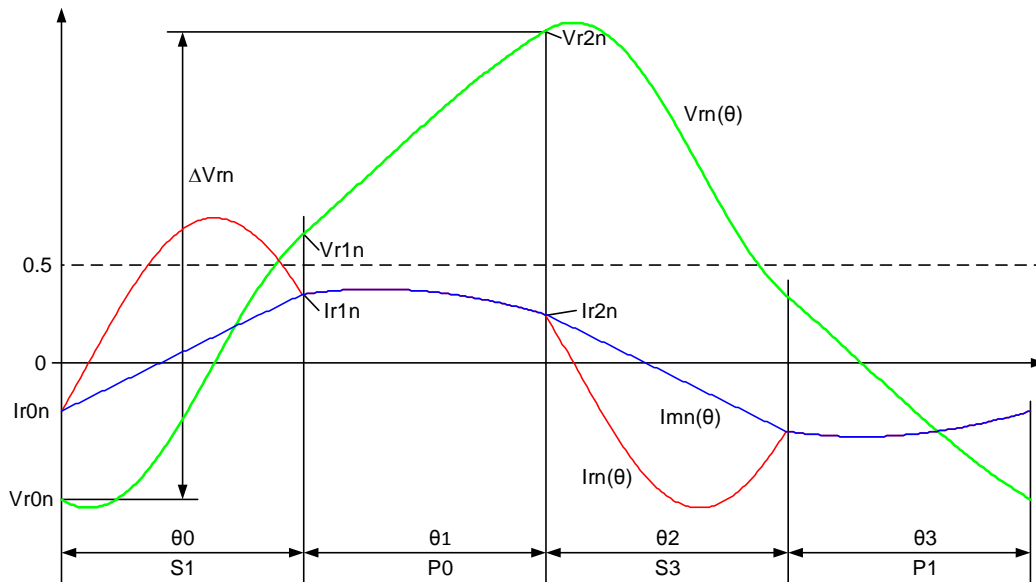


Figure 8. LLC Normalized Resonant Waveforms for BH Region ($x = 1$, $I_m = 5$, $\Delta V_{rn} = 2.4$)

1.1.4 Below Resonance Low Power (BL)

In this region each half-cycle contains three states. The sequence of states defining this region is as follows:

$$\begin{pmatrix} \text{State_Seq} \\ \text{PSN_n} \\ \text{PRS_n} \end{pmatrix} = \begin{pmatrix} \text{P0} & \text{S1} & \text{P0} & \text{P1} & \text{S3} & \text{P1} \\ 1 & 1 & 1 & 0 & 0 & 0 \\ \text{na} & \text{x} & \text{na} & \text{na} & \text{-x} & \text{na} \end{pmatrix}$$

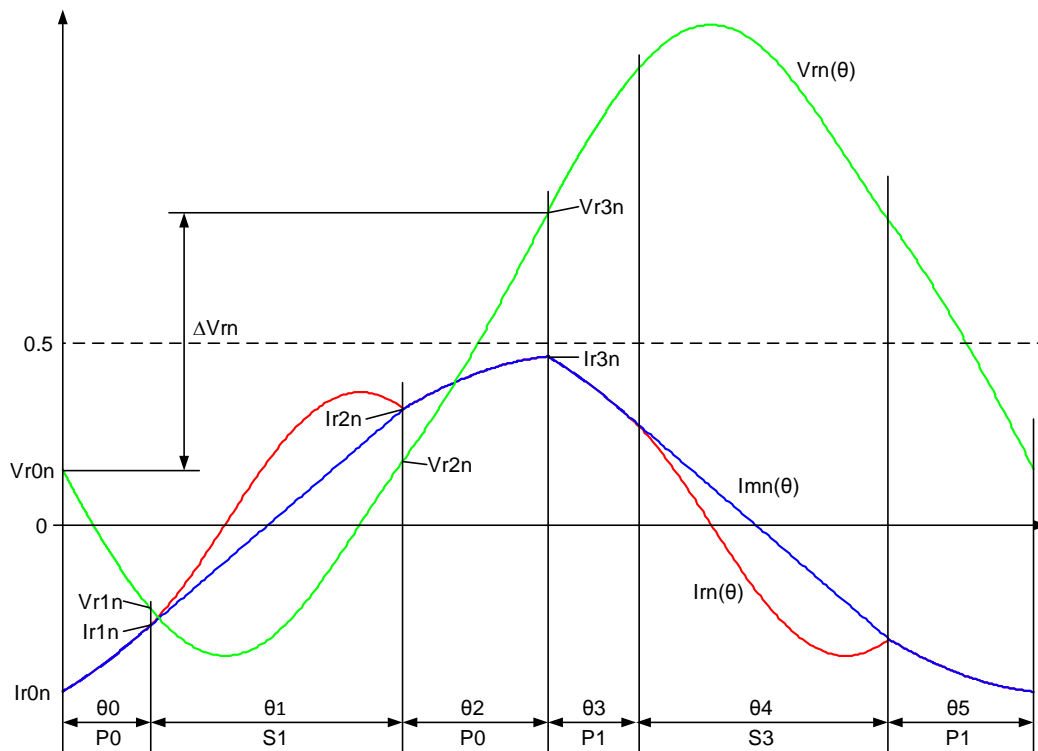


Figure 9. LLC Normalized Resonant Waveforms for BL Region ($x = 1$, $I_m = 5$, $\Delta V_{rn} = 0.7$)

1.2 Steady-State Operating Point

A steady-state operating point is calculated for a given voltage gain (x), inductor ratio (I_m), and normalized input cycle charge (ΔV_{rn}). The steady-state solution is achieved by equating the cycle energy drawn from the input capacitor to the cycle energy delivered to the output capacitor. For each operating mode, some of the state boundary reactive current/voltage levels are known and the remaining boundary values and state angular durations can be determined by numerical solution. This method can be repeated for a range of different x , I_m , and ΔV_{rn} to evaluate the complete LLC converter characteristic.

Solution of the steady-state operating point can be streamlined if we know in which operating mode our steady-state solution exists, or indeed if a useful steady-state solution exists before starting the numerical solution. This information can be obtained by pre-calculating the steady-state solution at the boundaries of each operating mode and at the boundaries of useful operation. Typically at the mode boundaries are additional constraints and these make the steady-state boundary solution relatively easy to compute. The next sections look in turn at how to obtain solutions for the mode boundaries and the boundaries of the useful operating regions.

1.2.1 ZCS/RR Boundary Condition

An important advantage of the LLC converter topology is its ability to operate the half-bridge MOSFETs in soft-switched or Zero Voltage Switched mode. The reduced switching energy that results allows LLC converters to operate efficiently at higher switching frequencies than alternative hard-switched power converter topologies. Not all regions of the LLC characteristic benefit from ZVS, and it is important that a practical LLC power converter is not allowed to stray into these non-ZVS regions.

As the name suggests the ZCS/RR Boundary Condition is actually two different boundary conditions. Both of these boundaries are closely associated with the loss of ZVS switching. For this reason, the boundary that occurs at lowest input power is taken as the effective boundary of the BH mode or region.

1.2.1.1 Resonant Reversal (RR) Boundary

Resonant Reversal occurs when an S0 State can occur before the end of the first BH half-cycle. The boundary condition occurs when the secondary winding voltage is just sufficient to forward bias the next pair of rectifier diodes at the end of the first BH half-cycle. This boundary condition may be expressed in normalized form as follows:

$$V_{r2n} = x \times \left(\frac{I_m + 1}{I_m} \right) + 1 = \frac{\Delta V_{rn} + 1}{2}$$

$$\Delta V_{rn} = 2 \times x \times \left(\frac{I_m + 1}{I_m} \right) + 1 \quad (6)$$

In other words, the resonant reversal boundary for a given value of x and I_m is obtained by setting the normalized input cycle charge (ΔV_{rn}) to the value returned by the expression in Equation 6. Note that ZVS operation is actually lost when the reverse resonant current amplitude is sufficient for it to cross the zero axis. In reality, this occurs slightly above the RR boundary.

In theory, it is possible to operate above the RR boundary when in the AH region. The reason being that since the S1 resonant current does not reach zero before the end of the half-cycle, it is not possible for it to reverse before the end of the half-cycle. Despite this, the RR boundary is used to constrain average input power. This ensures there is not a problem under transient conditions if the switching frequency is dropped through resonance.

1.2.1.2 Zero Current Switched (ZCS) Boundary

The Zero Current Switched (ZCS) boundary occurs when the resonant current falls to zero at the end of the first BH half-cycle. If the resonant current has fallen to zero, then ZVS operation cannot occur because there is no current to discharge the PSN node capacitance during dead time.

The condition for ZCS Boundary operation may be expressed as follows:

$$I_{r2n} = -I_{r0n} = 0 \quad (7)$$

Fixing the initial resonant inductor current as indicated in the previous equation, in addition to the other requirements for steady-state operation, allows the ZCS Boundary to be defined. This can be done for a range of x and I_m values and returns the normalized input cycle charge (ΔV_{rn}) that delivers steady-state operation at the ZCS boundary. Note that full ZVS operation is lost before the ZCS boundary is crossed.

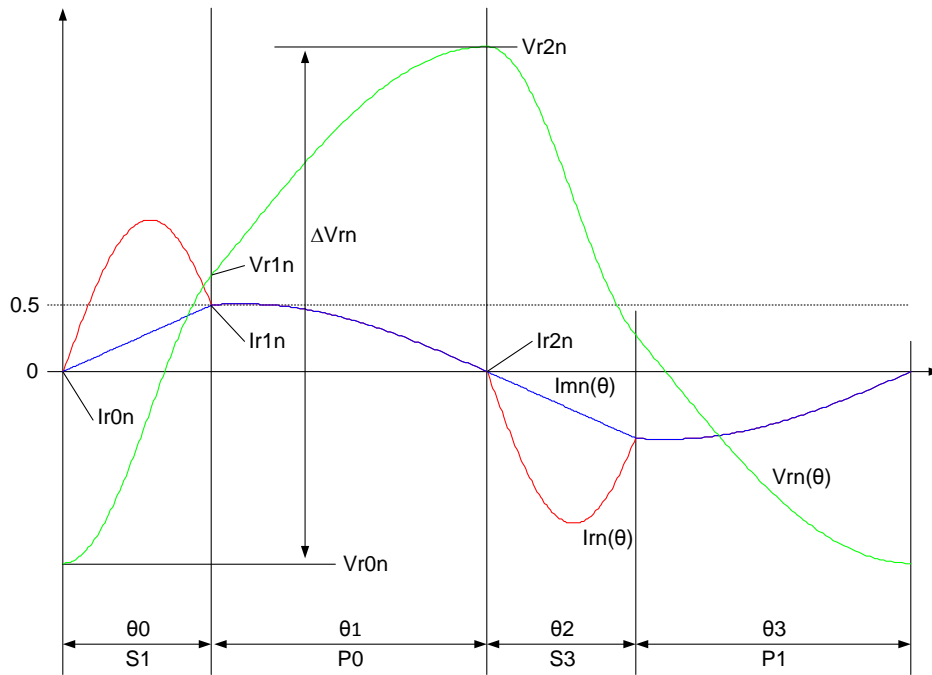


Figure 10. LLC Normalized Resonant Waveforms for ZCS Boundary Condition ($x = 1.3$, $I_m = 7$, $\Delta V_{rn} = 3.88$)

1.2.2 AH/BH Boundary Condition

The boundary between the AH and BH modes/regions occurs when the switching frequency is equal to the L_r/C_r resonant frequency. At this boundary the LLC resonant current and voltage waveforms are as illustrated in Figure 11. At this condition in the steady-state, the initial conditions for both A states are known and the angular duration of each half-cycle is also known.

$$I_{r0n} + x \times \frac{\theta_0}{I_m} = I_{r1n} = -I_{r0n}$$

$$\theta_0 = \pi$$

$$I_{r0n} = \frac{x \times \pi}{2 \times I_m}$$

$$V_{r0n} = \frac{1 - \Delta V_{rn}}{2}$$

(8)

Hence, it can be shown that for all load conditions: $x = 0.5$

The boundary condition between the AH and BH regions is therefore defined as the expression in Equation 8 for all values of I_m and ΔV_{rn} .

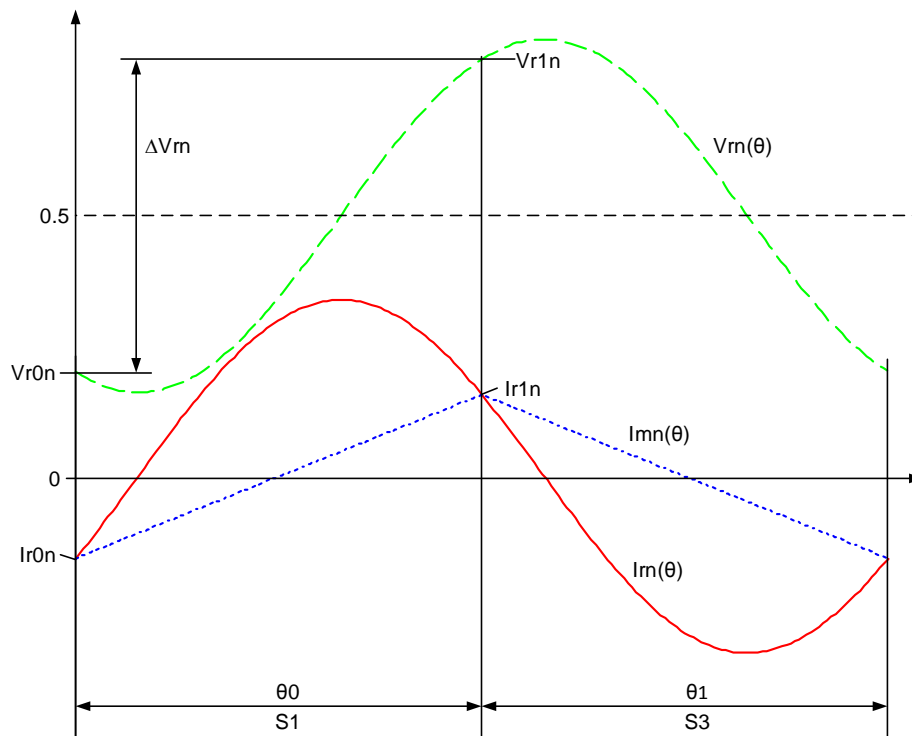


Figure 11. LLC Normalized Resonant Waveforms for AH/BH Boundary Condition ($x = 0.5$, $I_m = 5$, $\Delta V_{rn} = 0.6$)

1.2.3 BH/BL Boundary Condition

The boundary between the BH and BL modes occurs when the voltage at the start of the first half-cycle is just insufficient to forward bias the secondary rectifier diodes. For this reason, the switching cycle starts with a P0, rather than an S1 state. The condition at the boundary of operation can be determined as follows:

$$\begin{aligned}
 1 &= x \left(\frac{I_m + 1}{I_m} \right) + V_{r0n} \\
 V_{r0n} &= \frac{1 - \Delta V_{rn}}{2} \\
 \Delta V_{rn} &= 2 \times x \left(\frac{I_m + 1}{I_m} \right) - 1
 \end{aligned} \tag{9}$$

This expression determines the ΔV_{rn} value at the boundary condition for a given value of x and I_m .

1.2.4 AH/AL Boundary Condition

The boundary condition between the AH and AL modes occurs when there is just insufficient voltage to forward bias the secondary rectifier diodes at the start of the A1 state (as observed from the AH region). This condition may be expressed as follows:

$$V_{r1n} = 1 - x \left(\frac{I_m + 1}{I_m} \right) \tag{10}$$

Replacing the initial condition with this expression in the steady-state solution for the AH operating region provides us with a solution for the boundary condition.

1.2.5 Combined Boundary Solution

The graphic in Figure 12 shows the boundary values for ΔV_{rn} versus voltage gain for a range of I_m values. Based upon this data the operating mode of any given operating point ($I_m, x, \Delta V_{rn}$) can be predicted; therefore, the correct sequence of states for which to obtain a steady-state solution can be selected.

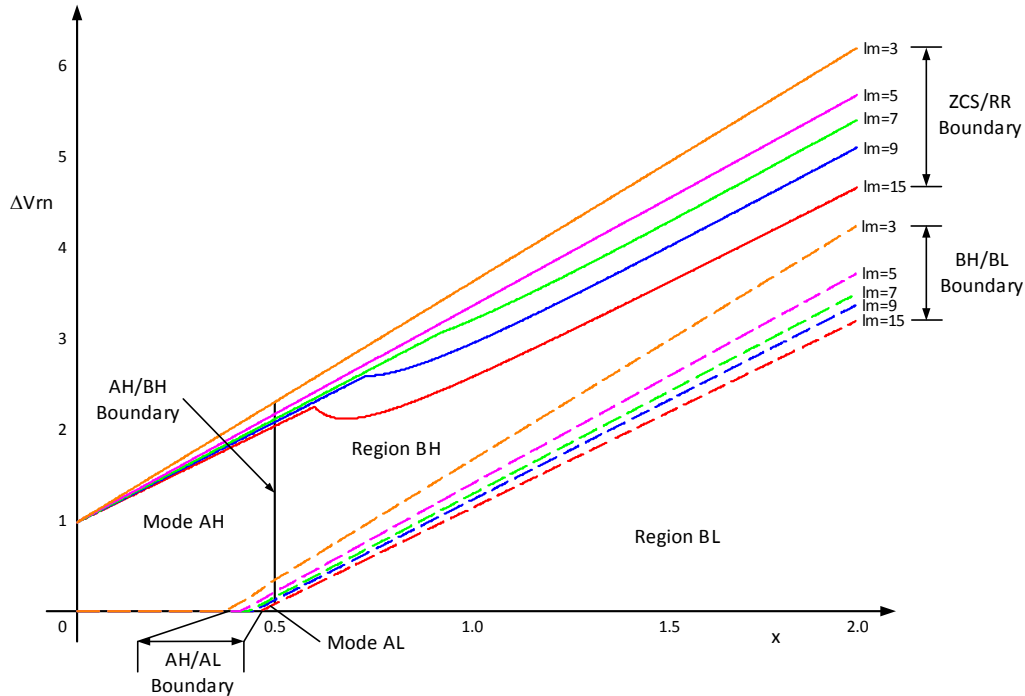


Figure 12. LLC Combined Boundary Solution ΔV_{rn} vs Voltage Gain (x) and Inductor Ratio (I_m)

1.2.6 Steady-State Operating Characteristic Normalized to Output Voltage

Based upon the complete Boundary solution, it is now possible to compute steady-state operating points over a range of inductor ratio (I_m), voltage gain (x), and normalized input charge (ΔV_{rn}) values. At each steady-state operating point, parameters of interest such as input power and switching frequency can be computed. Figure 13 presents the LLC input average current characteristic, normalized to output voltage, vs normalized period for an inductor ratio $I_m = 5$.

$$I_{inavno} = \frac{I_{inavn}}{x} = I_{inav} \times \frac{Z_n}{V_{in}} \times \frac{V_{in}}{n \times V_{out}} = I_{inav} \times \frac{Z_n}{n \times V_{out}} \quad (11)$$

The most common power supply requirement comes from the need to deliver constant output voltage in the face of varying load current and input voltage. At maximum load current, the operating trajectory of the LLC converter is represented in Figure 13 by the blue curve. As the input voltage changes, the LLC operating point moves left or right along this operating trajectory. This operating trajectory spans the two voltage gain curves that define the extremes of input voltage range.

Reduced power operating trajectories can be obtained by sliding this Blue curve down the Y-axis, while ensuring that it still spans the same two voltage gain curves.

The horizontal orange line in Figure 13 represents LLC operation with constant average input current. The overcurrent protection feature provided by the UCC29950 (OCP2) will ensure that steady-state LLC operation cannot stray above this orange line.

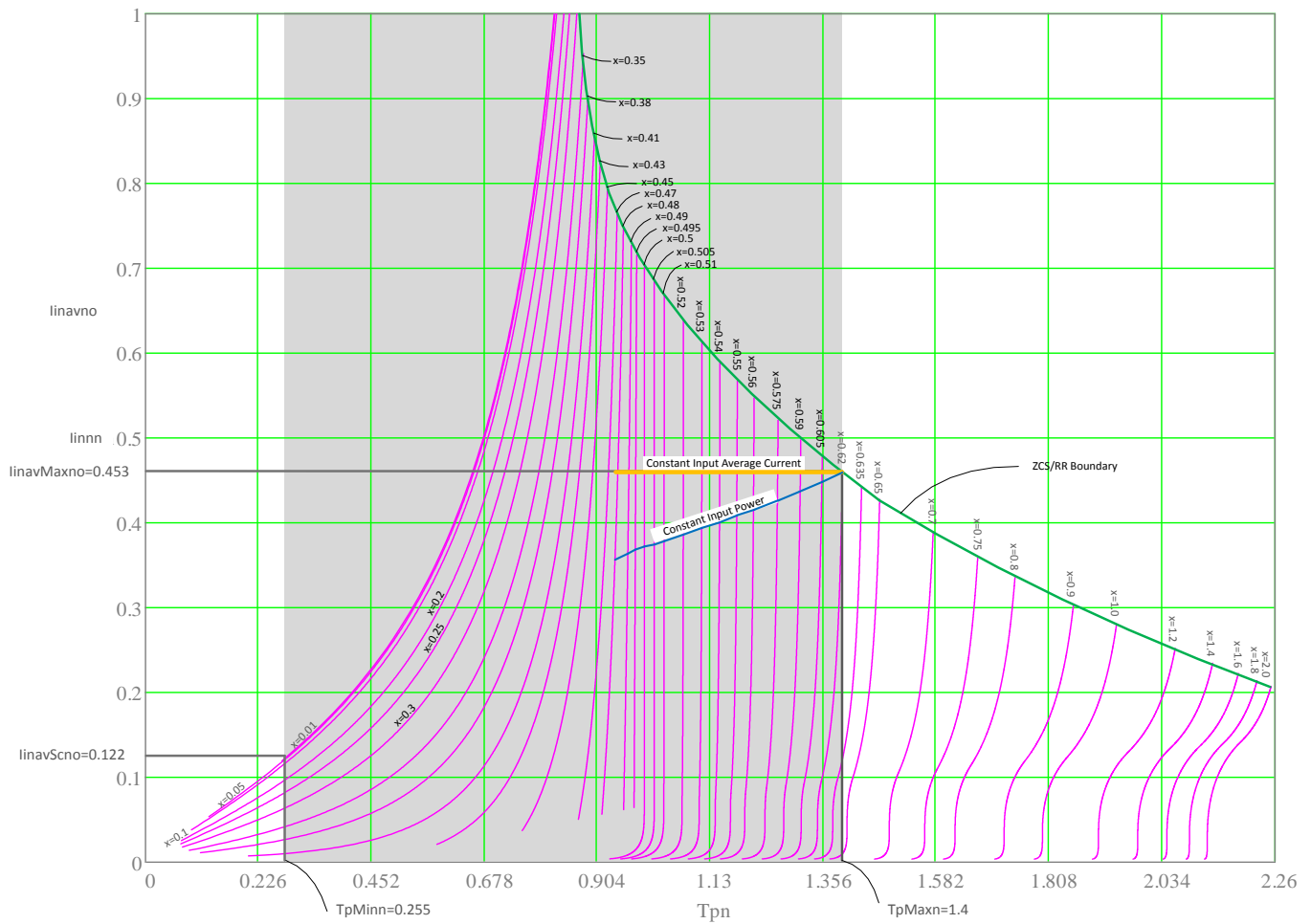


Figure 13. Steady-State Input Average Current (i_{inavno}) vs Switching Period (T_{pn}) for Range of Voltage Gain (x), Inductor Ratio $l_m = 5$

2 LLC Design

The previous section described how LLC operation can be broken down into different operating regions based upon the sequence of switch states. Numerically solving the system of equations that describe operation within each region and combining the results allows us to generate the complete steady-state normalized operating characteristic of the LLC converter. Once a steady-state operating point has been obtained, it is possible to calculate any other parameters of interest for this operating point, including the resonant current and voltage waveforms. The design process used here is to calculate a 'figure of merit' for all the possible LLC converter designs and to use this to help make the component selections that lead to the best possible performance in achieving the target specification.

[Section 2.1](#) details the calculation of Current Loss Factor. This provides a measure of relative resistive conduction loss between different possible LLC component selections. [Section 2.2](#) provides a top-level view of the design process. In this process, a series of informed decisions are taken to shrink the array of possible designs down to the final choice of components.

2.1 Current Loss Factor

The LLC converter design process consists of selecting the transformer turns ratio (n), the characteristic impedance (Z_n), the resonant frequency (ω_0), and the inductor ratio (l_m). There are a number of possible designs that meet the specification requirement, our job as designers is to select the design that offers best operating efficiency. For this we need a way of comparing the operating efficiency of a range of different designs.

The power lost in the primary and secondary circuits (PL_{Tot}) can be approximated as follows:

$$PL_{Tot} = PL_{Pri} + PL_{Sec} = I_{priRms}^2 \times R_{priEq} + I_{secRms}^2 \times R_{secEq} + I_{outavg} \times V_{fdEq} \quad (12)$$

$$PL_{Tot} = \frac{\left(I_{priRms} \times \frac{Z_n}{V_{in}} \right)^2 \times R_{priEq} + \left(I_{secRms} \times \frac{Z_n}{V_{in}} \right)^2 \times R_{secEq}}{\left(\frac{Z_n}{V_{in}} \right)^2} + I_{outavg} \times V_{fdEq} \quad (13)$$

$$PL_{Tot} = \frac{I_{priRmsn}^2 \times R_{priEq} + I_{secRmsn}^2 \times R_{secEq}}{l_{inavgn}^2} \times l_{inavg}^2 + I_{outavg} \times V_{fdEq} \quad (14)$$

R_{priEq} is the total effective resistance in the primary circuit. For a half-bridge, it includes the ON-state resistance of each arm of the bridge.

R_{secEq} is the total effective resistance in the secondary circuit.

V_{fdEq} is the total effective forward voltage drop of the output rectifier diodes. For a full-wave rectifier, this is twice the forward voltage drop of the rectifier diodes employed.

Consider the special case that V_{out} is equal to $V_{in}/2$ and we are delivering a constant power. In other words, the transformer turns ratio is only being adjusted to compensate for the LLC voltage gain (x) at our operating point. Also assume that the primary and secondary circuit resistance values are equal and are independent of transformer turns ratio. For this special case, modify the total loss expression as follows:

$$PL_{Tot} = \frac{I_{priRmsn}^2 + I_{secRmsn}^2}{l_{inavgn}^2} \times R_{priSecEq} \times l_{inavg}^2 + I_{outavg} \times V_{fdEq} \quad (15)$$

For our special case, all parameters in the loss expression are constant except the sum of squares of the rms over average current. This term is referred to as the Current Loss Factor (CLF) of the design, defined as follows:

$$CLF = \frac{I_{priRmsn}^2 + I_{secRmsn}^2}{l_{inavgn}^2} \quad (16)$$

At any given steady-state operating condition, the Primary and Secondary normalized RMS currents can be calculated as follows:

$$I_{priRmsn}^2 = \frac{1}{\sum_S \theta_{S+} + \sum_P \theta_{P+}} \times \left(\sum_S \int_0^{\theta_S} I_r S_n(\theta)^2 d\theta + \sum_P \int_0^{\theta_P} I_r P_n(\theta)^2 d\theta \right) \quad (17)$$

$$I_{secRmsn}^2 = \frac{n^2}{\sum_S \theta_{S+} + \sum_P \theta_{P+}} \times \left(\sum_S \int_0^{\theta_S} (I_r S_n(\theta) - I_m S_n(\theta))^2 d\theta \right) \quad (18)$$

S represents the number of S-States in a switching cycle of the current operating region.

P represents the number of P-States in a switching cycle of the current operating region.

The Current Loss Factor (CLF) has been evaluated for each steady-state operating point from [Figure 13](#) and the results are presented in [Figure 14](#). Each point on this characteristic represents an LLC design that is delivering the required specification in terms of V_{in} , V_{out} , and P_{out} . This characteristic allows comparison of the resistive power losses associated with each design.

The current loss factor characteristic of [Figure 14](#) provides a number of useful insights:

1. The most efficient operating point occurs when operating at resonance with a voltage gain of $x = 0.5$ (for a half-bridge design).
2. There is a gradual increase in resistive power loss as the operating point is moved down below resonance ($x > 0.5$).
3. Resistive power loss increases much more rapidly as the operating point is moved above resonance ($x < 0.5$). Resistive power losses become very severe once the voltage gain drops below $x = 0.35$. Designs that normally operate in this region should be avoided.
4. On any voltage gain curve, the resistive power loss is always a minimum at or close to the ZCS/RR Boundary. Resistive power loss increases rapidly as we move away from this ZCS/RR boundary. The most efficient design should therefore always operate as close as possible to the ZCS/RR boundary.

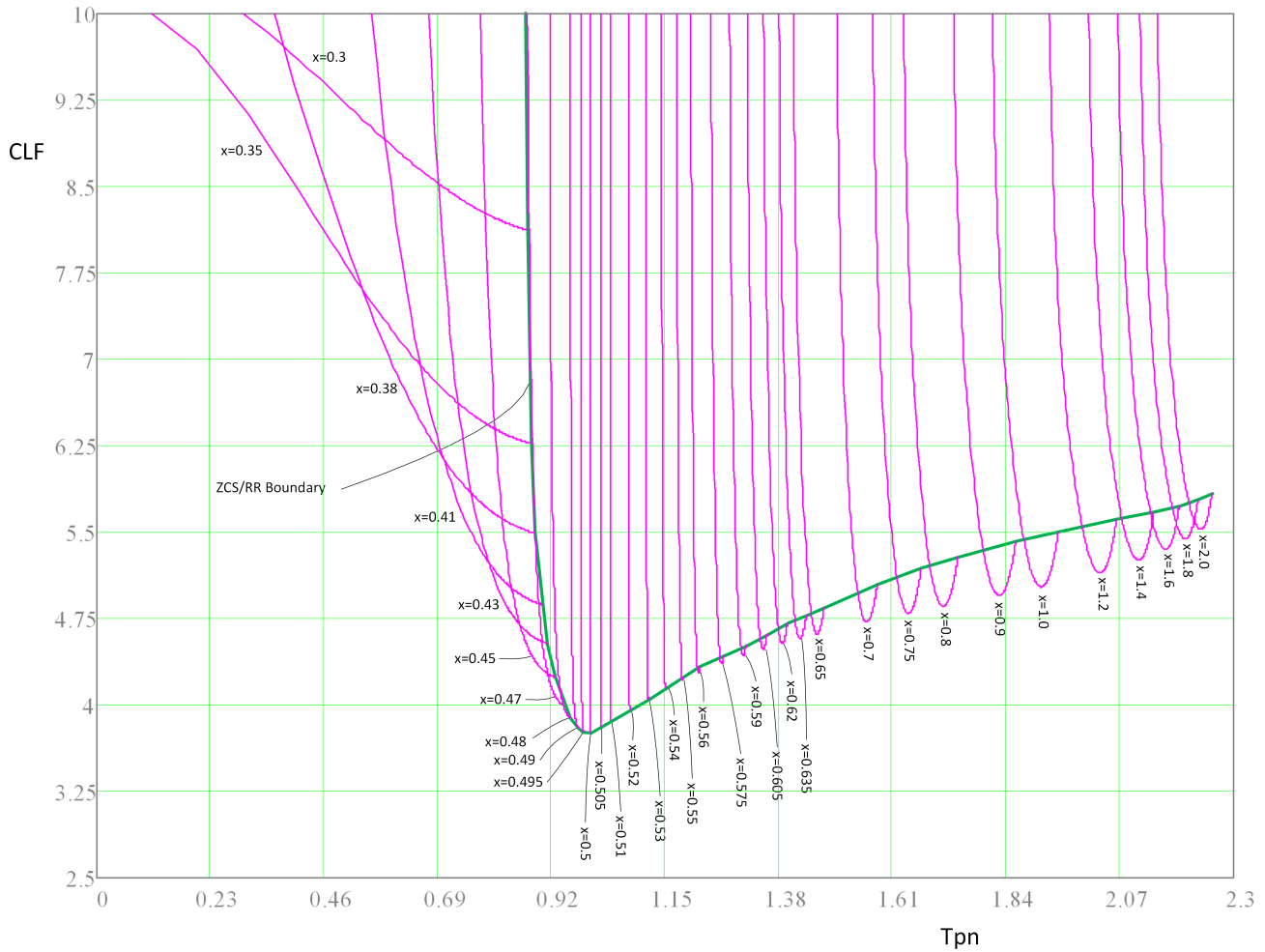


Figure 14. Current Loss Factor (CLF) vs Switching Period (Tpn) for Range of Voltage Gain (x), Inductor Ratio $l_m = 5$

2.2 LLC Design Approach

A typical LLC converter application delivers fixed output voltage while the input voltage and load current vary over some defined range. As designers, our primary interest is normally to maximize the LLC converter efficiency at maximum load power. This is because the thermal circuit must be sized to cope with the maximum power loss in the LLC converter.

The top-level design steps are outlined in the following list. Each of these design steps are examined in more detail in the following sub-sections:

1. Select the inductor ratio. This narrows the 'design space' to just one set of the LLC characteristic curves illustrated in [Appendix B](#).
2. Select the transformer turns ratio. This narrows the 'design space' to the area between two voltage gain curves on the selected LLC characteristic.
3. Select the linavno value that corresponds to maximum output power. This locates our maximum power regulation curve to a single curve on the selected LLC characteristic. Having selected the maximum power operating curve, the required LLC reactive components can be determined.

2.2.1 Inductor Ratio Selection

Many effects of adjusting the inductor ratio are expected:

1. When operating below resonance a bigger inductor ratio requires a lower switching frequency to achieve the same voltage gain. The bigger the inductor ratio used, the greater the range of switching frequencies required to achieve the same voltage gain range. Observe the change in axis scale required for normalized period across the characteristic curves of [Appendix B](#).
2. The secondary RMS/Average current also increases with increasing inductor ratio. This occurs because the secondary diode conduction interval becomes a smaller fraction of the switching cycle. For this reason, the resistive conduction power losses increase with inductor ratio when operating below resonance ($x > 0.5$).
3. When operating above resonance, dropping the inductor ratio causes an increase in the Current Loss Factor (CLF). [Figure 15](#) shows how the Current Loss Factor varies with LLC voltage gain and inductor ratio when operating on the ZCS/RR Boundary. This graphic illustrates that higher inductor ratios offer slightly lower conduction loss above resonance but higher conduction loss below resonance. Once the inductor ratio falls below $l_m = 5$, the increase in conduction loss around the resonant frequency becomes noticeable.
4. The dead-time required to discharge the switched node capacitance (CPSNe) at maximum switching frequency is directly related to inductor ratio. It is important that the time required to discharge the PSN at maximum switching frequency does not exceed the dead-time provided by UCC29950 or ZVS operation is lost. This calculation for PSN discharge time is included in [Section 2.2.1.1](#). For all designs this requirement should be checked and the inductor ratio selection adjusted, if necessary.

For most applications, an inductor ratio in the range of 3–7 works best with the UCC29950.

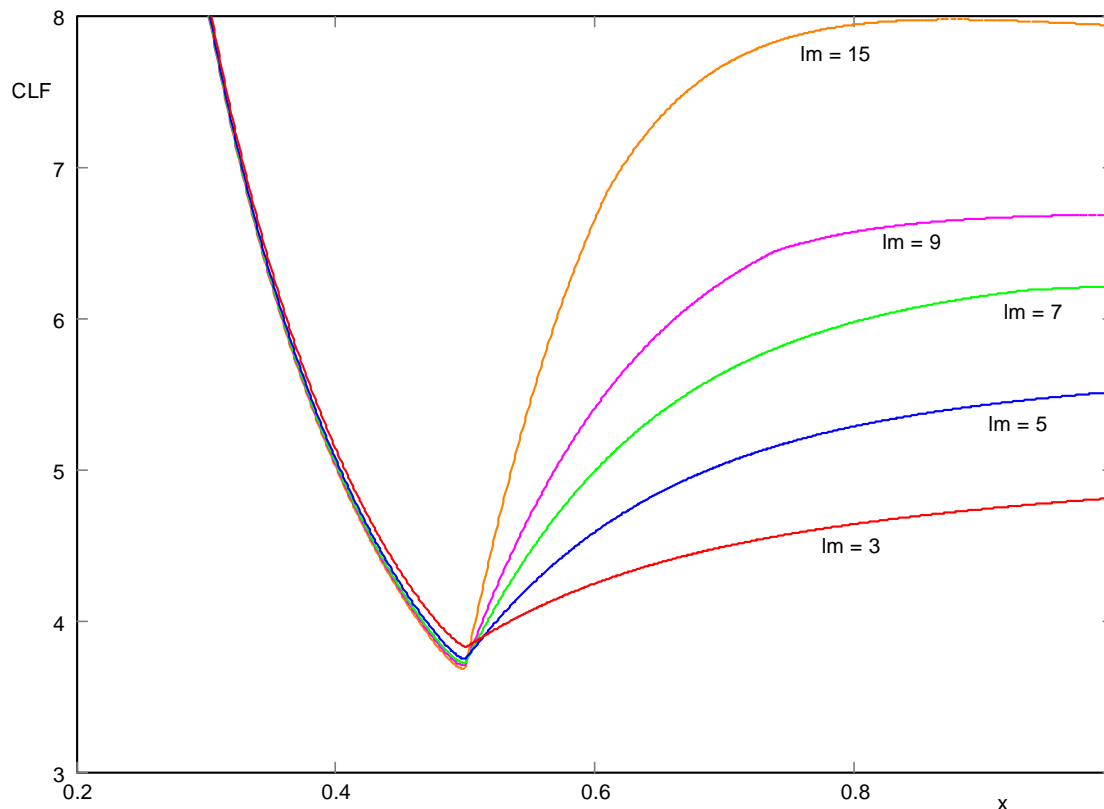


Figure 15. CLF vs x for Range of l_m at ZCS/RR Boundary Operation

2.2.1.1 Dead Time Required at Maximum Switching Frequency

The dead time at maximum switching frequency delivered by the UCC29950 LLC controller is fixed. This section shows how to check that this maximum frequency dead time is suitable for our LLC design. For this calculation, it is assumed that no load is being drawn from the output so the secondary rectifiers do not conduct for any portion of the switching cycle. With this assumption, our LLC converter can be represented by the equivalent circuit shown in [Figure 16](#).

With no current flowing into the secondary circuit, the resonant and magnetizing inductors are effectively connected in series. At the same time, they are being driven at a frequency that is well above the resonant frequency. The inductive impedance is much greater than the resonant capacitor impedance. The voltage on the resonant capacitor may therefore be approximated to a constant value of $V_{in}/2$ (0.5). In this case, the peak inductor current at the end of the positive half-cycle can be calculated as follows:

$$I_{rpkUIn} = \frac{T_p M_{inn}}{4 \times (1 + l_m)} \quad (19)$$

Since no power is being delivered to the load, the cycle charge drawn from the input must be close to zero. The resonant capacitor voltage during the dead-time must therefore be close to half the input voltage. During the dead-time, the LLC converter may be represented by the equivalent circuit shown in [Figure 17](#). C_{psne} is the total effective capacitance attached to the PSN node of the LLC half-bridge. It includes parallel combination of the effective drain-source capacitance of all the half-bridge switching MOSFETs. It also includes the parasitic capacitance across the primary winding of the transformer.

$$C_{psne} = 2 \times C_{dse} + C_{txpri} \quad (20)$$

Define a variable for the ratio of the resonant capacitor to the effective switched node capacitance as follows:

$$c_{psne} = \frac{C_r}{C_{psne}} \quad (21)$$

The normalized switched node voltage during the dead-time is described by the following equation:

$$V_{psnn}(\theta) = 0.5 + 0.5 \cos \left[\theta \times \sqrt{\frac{c_{psne}}{(1 + l_m)}} \right] - \sqrt{(1 + l_m) \times c_{psne}} \times I_{rpkUIn} \times \sin \left[\theta \times \sqrt{\frac{c_{psne}}{(1 + l_m)}} \right] \quad (22)$$

The dead-time can end as soon as the switched node voltage reaches zero. Hence, the following expression can be written for the required dead-time conduction angle at maximum switching frequency:

$$0 = 0.5 + 0.5 \cos \left[\theta_{fsmax} \times \sqrt{\frac{c_{psne}}{(1 + l_m)}} \right] - I_{rpkUIn} \times \sqrt{(1 + l_m) \times c_{psne}} \times \sin \left[\theta_{fsmax} \times \sqrt{\frac{c_{psne}}{(1 + l_m)}} \right] \quad (23)$$

Hence, the maximum dead-time required for full ZVS operation at maximum switching frequency can be determined:

$$T_{dfsmax} = \frac{\theta_{fsmax}}{\omega_0} = \sqrt{\frac{1 + l_m}{c_{psne}}} \times \left[\arccos \left[\frac{-0.5}{\sqrt{0.5^2 + (1 + l_m) \times c_{psne} \times (I_{rpkUIn})^2}} \right] - \arctan \left[\frac{I_{rpkUIn} \times \sqrt{(1 + l_m) \times c_{psne}}}{0.5} \right] \right] \quad (24)$$

It is important to use [Equation 24](#) to check that the dead-time provided by UCC29950 at maximum switching frequency is sufficient. The required dead-time can be decreased, if required, by reducing the inductor ratio used for the design, or increasing the capacitor ratio (c_{psne}) by reducing the effective switched-node capacitance of the primary half-bridge.

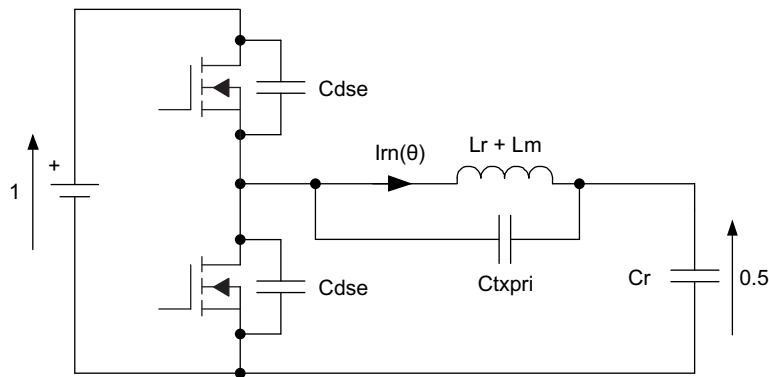


Figure 16. LLC Normalized Equivalent Circuit for Dead-Time at Zero Load Power

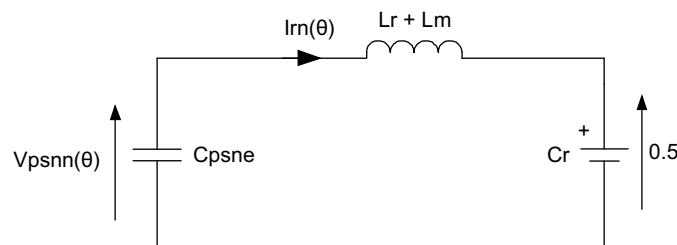


Figure 17. LLC Simplified Normalized Equivalent Circuit for Dead-Time at Zero Load Power

2.2.2 Turns Ratio Selection

LLC converter input to output ratio is the product of LLC voltage gain and turns ratio. Fixing the transformer turns ratio sets the range of LLC voltage gain over which the LLC converter must operate.

An LLC converter provides its lowest conduction loss when operating at resonance on the ZCS/RR boundary. This is clear from the Current Loss Factor curves of ([Appendix B](#)). Applications that have a fixed input and output voltage should be designed to operate at this point.

The LLC converter is normally required to be able to deliver fixed output voltage at maximum output power from a range of input voltage levels. This normal input voltage range (V_{inNMax} , V_{inNMin}) includes regulation tolerance of the PFC stage and twice line frequency ripple on the PFC output capacitor, for example. It is important that LLC power losses are minimized when working within this normal input voltage range.

The LLC converter is also expected to be able to deliver regulated output voltage, at maximum load power over an extended input voltage range. This extended input voltage range (V_{inEMax} , V_{inEMin}) allows the LLC converter to cope with transient and abnormal events such as line sags or surges, transient over/undershoot of the PFC output voltage, and hold-up requirements. Only transient operation is required over this extended input voltage range and therefore, LLC converter power loss in this region is not so important.

The transformer turns-ratio should be selected so that the normal input voltage range maps onto the LLC voltage gain range that offers minimum conduction loss. The LLC voltage gain range selected should lie on or very close to the resonant frequency. It may extend above or below resonance but should lie in the range $0.35 < x < 2$.

Having selected the gain range to cover the normal input voltage range, the transformer turns ratio required can be calculated as follows:

$$n = \frac{xN_{Min} \times V_{inNMax}}{V_{OutReg} + V_{fdEq}} \quad (25)$$

2.2.3 Calculating LLC Resonant Component Values

Maximum normalized input average current ($I_{inavMaxno}$) is chosen to be as close as possible to the intersection of the $xEMin$ curve with the ZCR/RR boundary. The characteristic impedance of the LLC resonant components are chosen such that the second level over-current limit (OCP2) level is mapped onto this $I_{inavMaxno}$ line. The resonant frequency of the LLC resonant components is chosen so that the UCC29950 minimum switching frequency ($f_{LLCFMIN}$) is mapped onto the T_{pn} axis at the intersection of the $xEMin$ curve and the ZCS/RR boundary. In this way, the UCC29950 minimum frequency limit and second-level overcurrent limit will ensure that the ZCS/RR boundary curve cannot be crossed.

The UCC29950 overcurrent limits are applied to the average current flowing into the LLC converter. As a consequence, the output power, and hence output current, that can be delivered increases with PFC output voltage. Normally, this does not present a problem because the PFC output voltage is regulated and therefore varies over a small range. It does mean; however, that the overcurrent limit level should be set to deliver the peak output power at the minimum bulk capacitor voltage. The LLC current sense resistor is selected to ensure that the second-level current limit (OCP2) does not allow ZCS/RR operation to persist if the output is overloaded.

$$I_{inOCP2} = \frac{1}{V_{inEMin}} \times \frac{P_{OutMax}}{\eta_{LLC}}$$

$$R_{CLS_LLC} = \frac{V_{CS_OCP2}}{I_{inOCP2}} \quad (26)$$

The coordinates of the intersection between the $xEMax$ curve and the ZCS/RR boundary curve (T_{pMaxn} , $I_{inavMaxno}$) are now used to compute LLC reactive component values:

$$Z_n = \frac{I_{inavMaxno} \times n \times (V_{OutReg} + V_{fdEq})}{I_{inOCP2}} \quad (27)$$

$$\omega_0 = 2 \times \pi \times T_{pMaxn} \times f_{LLCFMIN} \quad (28)$$

Hence we have the LLC converter resonant component values:

$$L_r = \frac{Z_n}{\omega_0}$$

$$C_r = \frac{1}{Z_n \times \omega_0}$$

$$L_m = I_m \times L_r \quad (29)$$

Design Example (Fixed Output Voltage Variable Input Voltage)

A.1 Design Example Introduction

For this design example, an LLC converter is designed that delivers a fixed regulated output voltage. The input voltage comes from the PFC pre-regulator stage. To cope with line surges, transient overload, and twice-line frequency ripple, the LLC converter must be able deliver regulated output over a range of input voltage levels. The target specification can be summarized as follows:

A.1.1 Input Data/Target Specification

Output Power Requirement: $P_{OutMax} = 512 \text{ W}$

Input Voltage Range

$$V_{in} = \begin{pmatrix} V_{inEMin} \\ V_{inNMin} \\ V_{inReg} \\ V_{inNMax} \\ V_{inEMax} \end{pmatrix} = \begin{pmatrix} 350 \\ 350.35 \\ 385 \\ 419.65 \\ 450 \end{pmatrix} \text{ V}$$

Switching Frequency Range. This is fixed within the UCC29950 controller device. These parameters are taken from the datasheet:

$$\begin{pmatrix} LLC_{FMIN} \\ LLC_{FMAX} \end{pmatrix} = \begin{pmatrix} 63.7 \text{ kHz} \\ 350 \text{ kHz} \end{pmatrix}$$

Output Voltage: $V_{outReg} = 208 \text{ V}$

Secondary Rectifier Diode Forward Voltage Drop: $V_{fdSec} = 1 \text{ V}$

A.1.2 Design Process

On the basis of the previous discussion, start by selecting to use an inductor ratio of $l_m = 5$. This allows us to choose the LLC steady-state linavno characteristic to employ for the design.

In this case, we aim to work just below resonance over the normal input voltage range (V_{inNMax} , V_{inNMin}). This ensures good efficiency while in normal regulation and ensures that we benefit from soft-switching of the output rectifier diodes. To do this, we must select a transformer turns ratio that is just above one.

$$n = \frac{42}{41} = 1.024$$

Based on the selected turns ratio we can work out both the normal and extended range of LLC voltage gain that is required:

$$\begin{pmatrix} xEMax \\ xNMax \\ x \\ xNMin \\ xEMin \end{pmatrix} = n \times \frac{VoutReg + 2 \times VfdSec}{Vin} = \begin{pmatrix} 0.615 \\ 0.614 \\ 0.559 \\ 0.513 \\ 0.478 \end{pmatrix}$$

To continue with the design process, select the closest voltage gain curves from Figure 18 that contain the required gain range calculated in the previous equation.

xEMin = 0.47
xEMax = 0.62

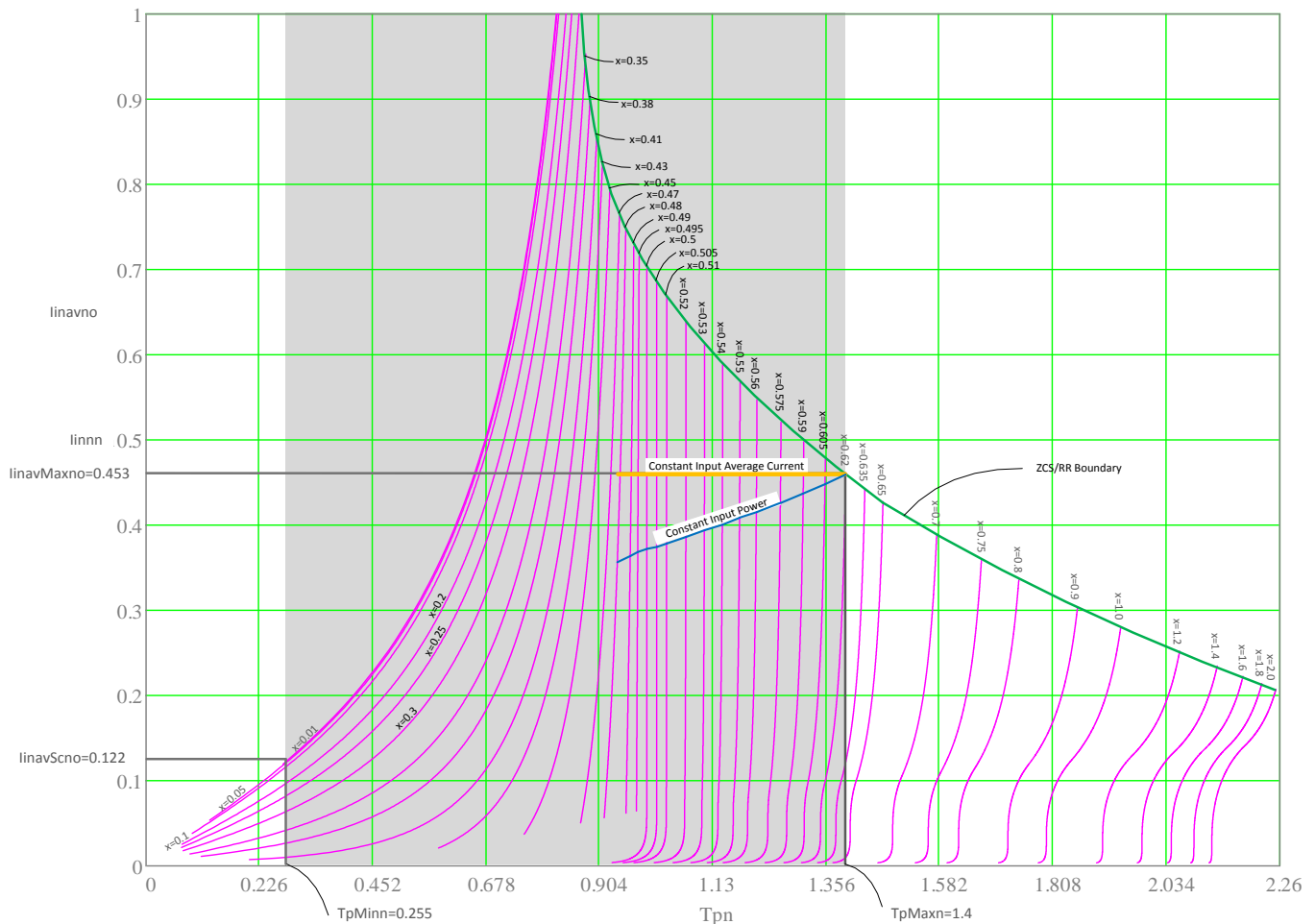


Figure 18. LLC Steady-State Normalized Operating Characteristic for Fixed Output Voltage $I_m = 5$

Clearly, there are a range of constant power curves running between these two gain curves that could be used to deliver the required input voltage regulation range. For a particular input power, the curve that is highest up the Y-axis delivers the highest characteristic impedance (Z_n) and hence the lowest total RMS current. To avoid excess switching power loss (and possibly damage to the primary MOSFETs) avoid having the peak power regulation curve cross the ZCS /RR Boundary. This forces us to place the peak power regulation curve no higher than the position of the blue curve indicated in Figure 18.

UCC29950 provides two mechanisms to ensure that the ZCS/RR boundary is not crossed by the LLC converter. Initially, the minimum switching frequency is limited to 63.7 kHz. Once the resonant period has been set, this prevents the LLC converter from operating to the right of the vertical T_{pMaxn} line. Secondly, an input overcurrent protection (OCP2) limit is designed to prevent the LLC converter from operating above the orange line. This prevents the design from straying over the ZCS/RR Boundary curve in the vertical direction.

Assume that the LLC converter efficiency at maximum output power is 90%. The average input current limit needed to ensure that we cannot exceed the peak power target at minimum input voltage is calculated as follows:

$$\eta_{LLC} = 90\%$$

$$I_{inOCP2} = \frac{1}{V_{inEMin}} \times \frac{P_{OutMax}}{\eta_{LLC}} = 1.625 \text{ A} \quad (30)$$

The OCP2 current limit threshold voltage can be obtained from the UCC29950 datasheet:

$$V_{CS_OCP2} = 0.6 \text{ V}$$

$$R_{CS_LLC} = \frac{V_{CS_OCP2}}{I_{inOCP2}} = 0.369 \ \Omega \quad (31)$$

The coordinates of the intersection between the $xEMax$ curve and the ZCS/RR boundary curve (T_{pMaxn} , $I_{inavMaxno}$) are used to compute LLC reactive component values:

$$I_{inavMaxno} = 0.453$$

$$T_{pMaxn} = 1.4$$

Based upon the parameters, the LLC controller resonant components may be determined as follows:

$$Z_n = \frac{I_{inavMaxno} \times n \times (V_{outReg} + 2 \times V_{fdSec})}{I_{inOCP2}} = 60 \ \Omega \quad (32)$$

$$\omega_0 = 2 \times \pi \times T_{pMaxn} \times LLC_{FMIN} = 8.9 \times 10^4 \text{ Hza} \quad (33)$$

Hence, we have the LLC converter resonant component values:

$$L_r = \frac{Z_n}{\omega_0} = 107 \ \mu\text{H}$$

$$C_r = \frac{1}{Z_n \times \omega_0} = 30 \ \text{nF}$$

$$L_m = I_m \times L_r = 535 \ \mu\text{H} \quad (34)$$

A.1.3 Short-Circuit Current Estimation

Having set the LLC converter resonant frequency, we have also set T_{pMin} .

$$T_{pMinn} = \frac{1}{LLC_{FMAX}} \times \frac{\omega_0}{2 \times \pi} = 0.255 \quad (35)$$

A short circuit applied to the LLC converter can be approximated as an output voltage of two forward voltage diode drops. Assume that the highest short-circuit current occurs at maximum input voltage. Assuming a full-wave bridge rectifier on the transformer secondary we get:

$$V_{outSc} = 2 \times V_{fdSec} = 2 \text{ V}$$

$$x_{Sc} = \frac{n \times V_{outSc}}{V_{inEMax}} = 0.005 \quad (36)$$

Applying a vertical line on [Figure 18](#) corresponding to T_{pMin} and looking for the intersection with the correct voltage gain curve (x_{Sc}) allows us to read off the normalized average input current value:

$$I_{inavScno} = 0.122$$

$$I_{outsc} = I_{inavScno} \frac{V_{inEMax}}{Z_n} \times n = 930 \text{ mA} \quad (37)$$

A.1.4 Maximum Dead-Time Estimation

The next step in the design process is to check that the dead-time at maximum switching frequency required by our LLC design matches the dead-time provided by the UCC29950 controller. The first step is to estimate the effective total capacitance associated with the PSN node. This can be approximated as the sum of the primary bridge MOSFETs drain to source capacitance and the parasitic capacitance across the transformer primary winding. This assumes that the resonant inductor is made up entirely of the transformer leakage inductance.

$$C_{dse} = 130 \text{ pF}$$

$$C_{pri} = 30 \text{ pF}$$

$$C_{psne} = 2 \times C_{dse} + C_{pri} = 290 \text{ pF}$$

The dead-time required by the LLC design for full ZVS operation at maximum switching frequency and zero load can be calculated as follows:

$$c_{psne} = \frac{C_r}{C_{psne}} = 101.755$$

$$T_{dfsmax} = \sqrt{L_r \times C_r} \times \sqrt{\frac{1 + I_m}{c_{psne}}} \times \left[\arccos \left[\frac{-0.5}{\sqrt{0.5^2 + \frac{c_{psne}}{(1 + I_m)} \times \left(\frac{T_{pMinn}}{4} \right)^2}} \right] - \arctan \left[\frac{T_{pMinn}}{2} \times \sqrt{\frac{c_{psne}}{(1 + I_m)}} \right] \right] = 0.943 \text{ } \mu\text{s} \quad (38)$$

The dead-time required is slightly greater than the value programmed into UCC29950, but it is sufficiently close that the no-load switching loss is acceptable. Keep in mind that the drivers for the LLC half-bridge are slightly asymmetric and this means that effective dead-time is slightly greater than the published datasheet parameter.

Normalized Steady-State LLC Design Curves

Figure 19 through Figure 23 illustrate the normalized steady-state LLC design curves.

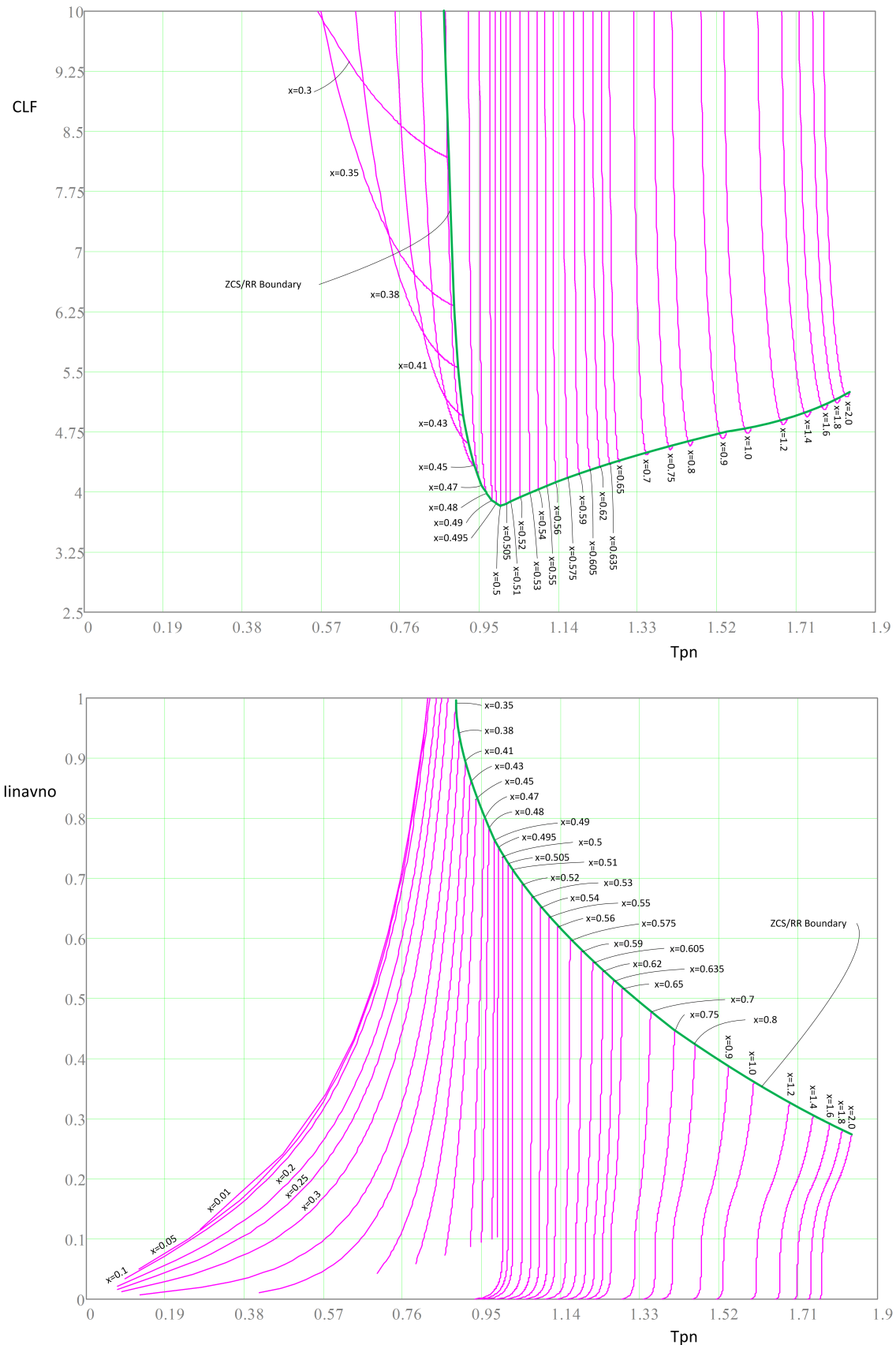


Figure 19. LLC Normalized Design Curves for Inductor Ratio $I_m = 3$

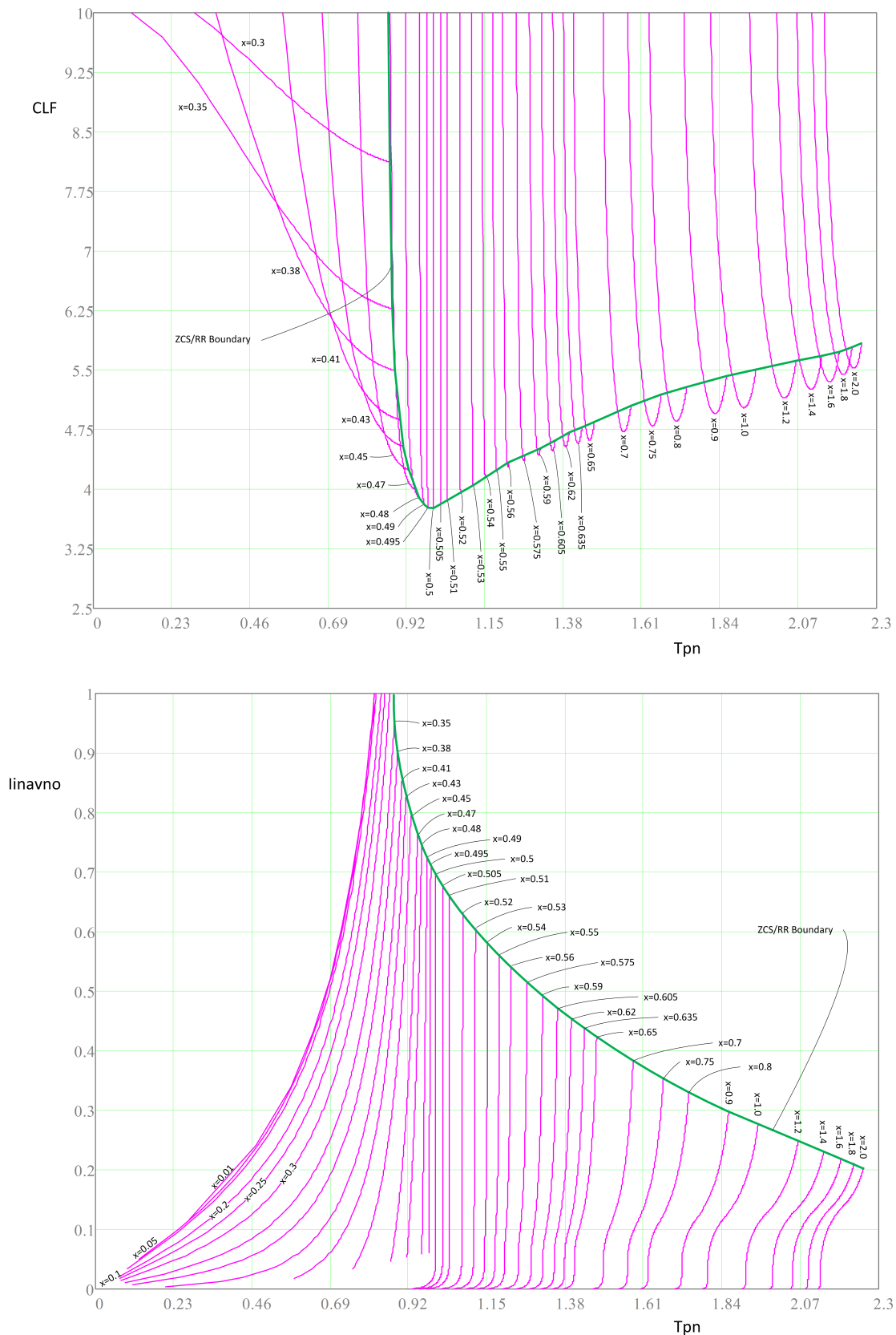


Figure 20. LLC Normalized Design Curves for Inductor Ratio $I_m = 5$

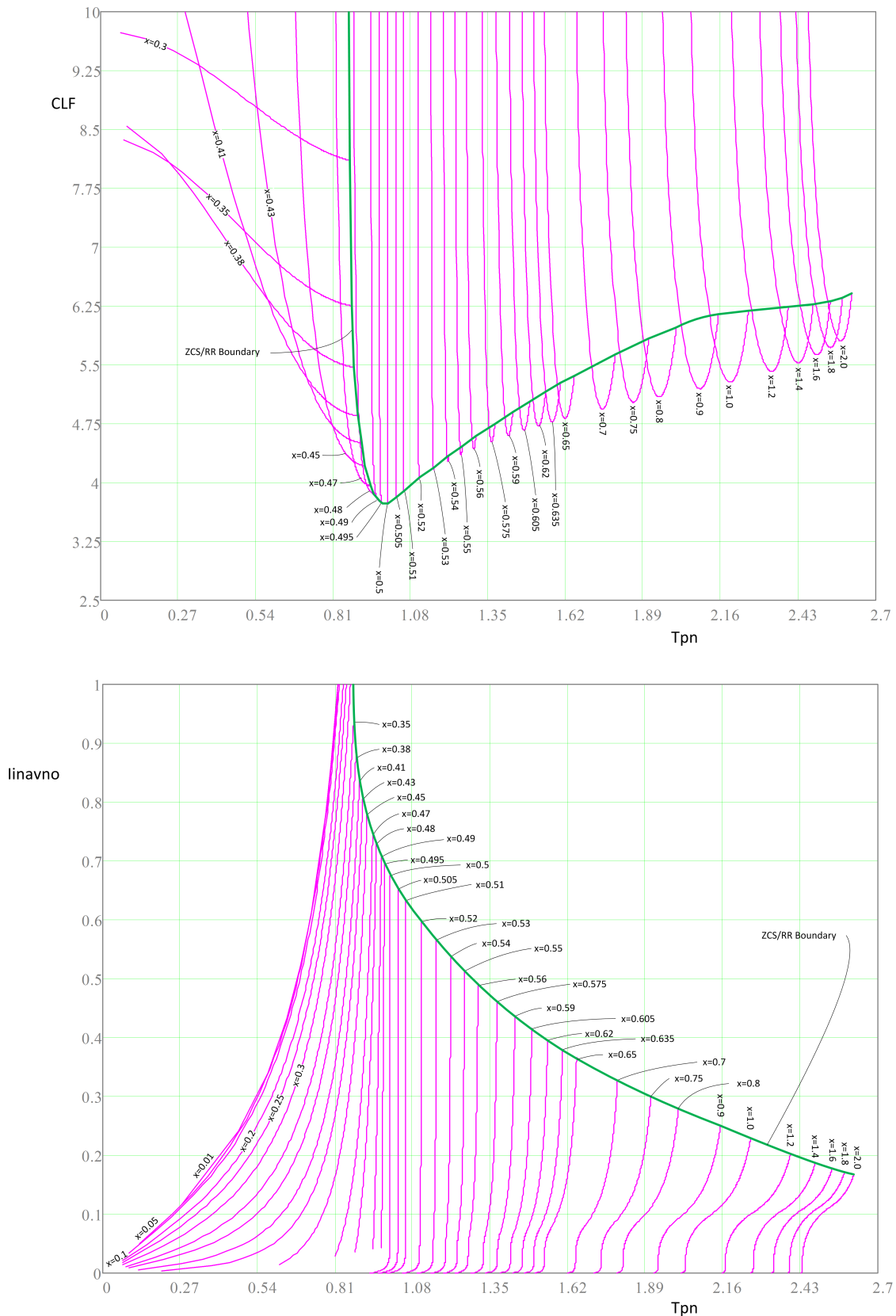


Figure 21. LLC Normalized Design Curves for Inductor Ratio $I_m = 7$

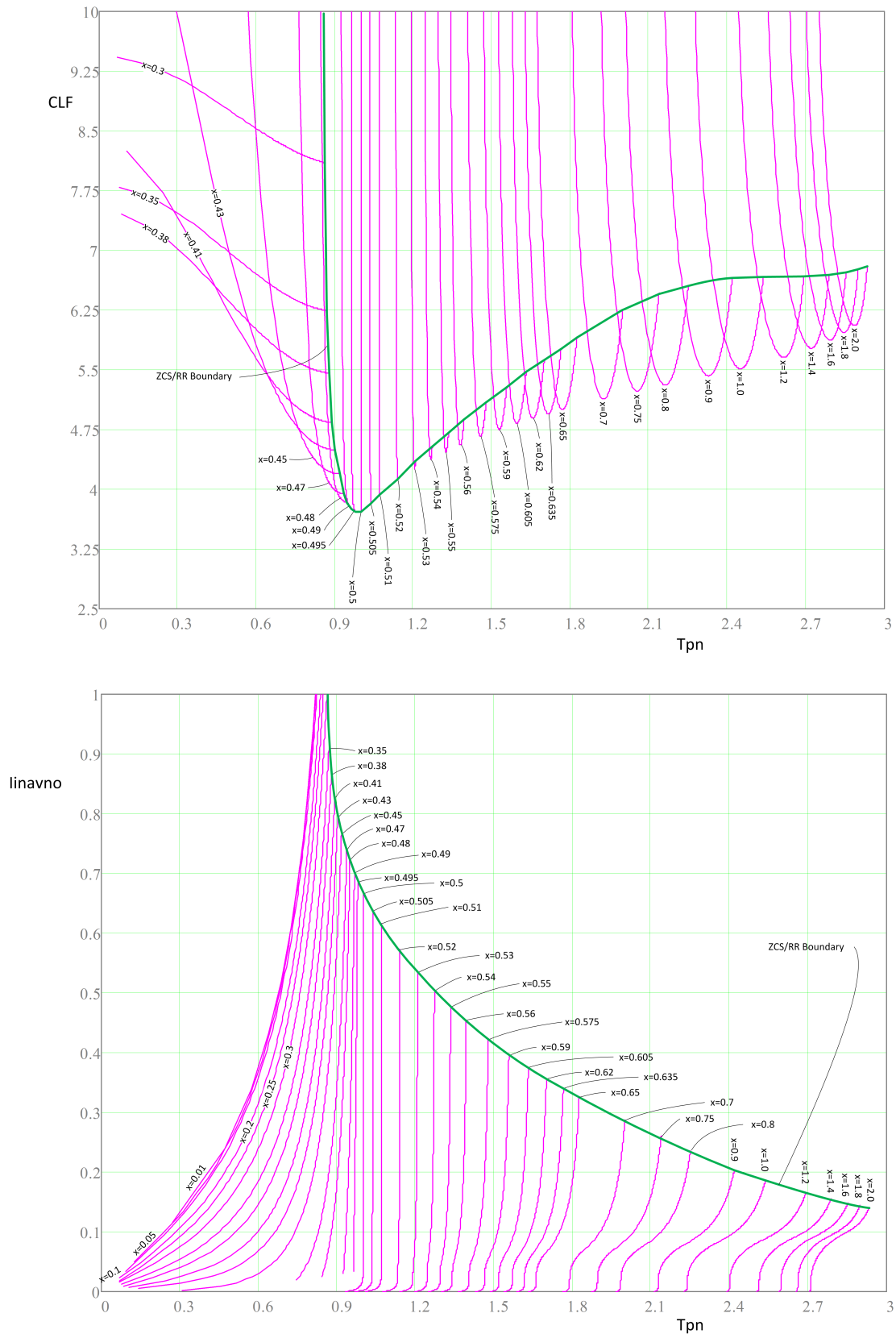


Figure 22. LLC Normalized Design Curves for Inductor Ratio $I_m = 9$

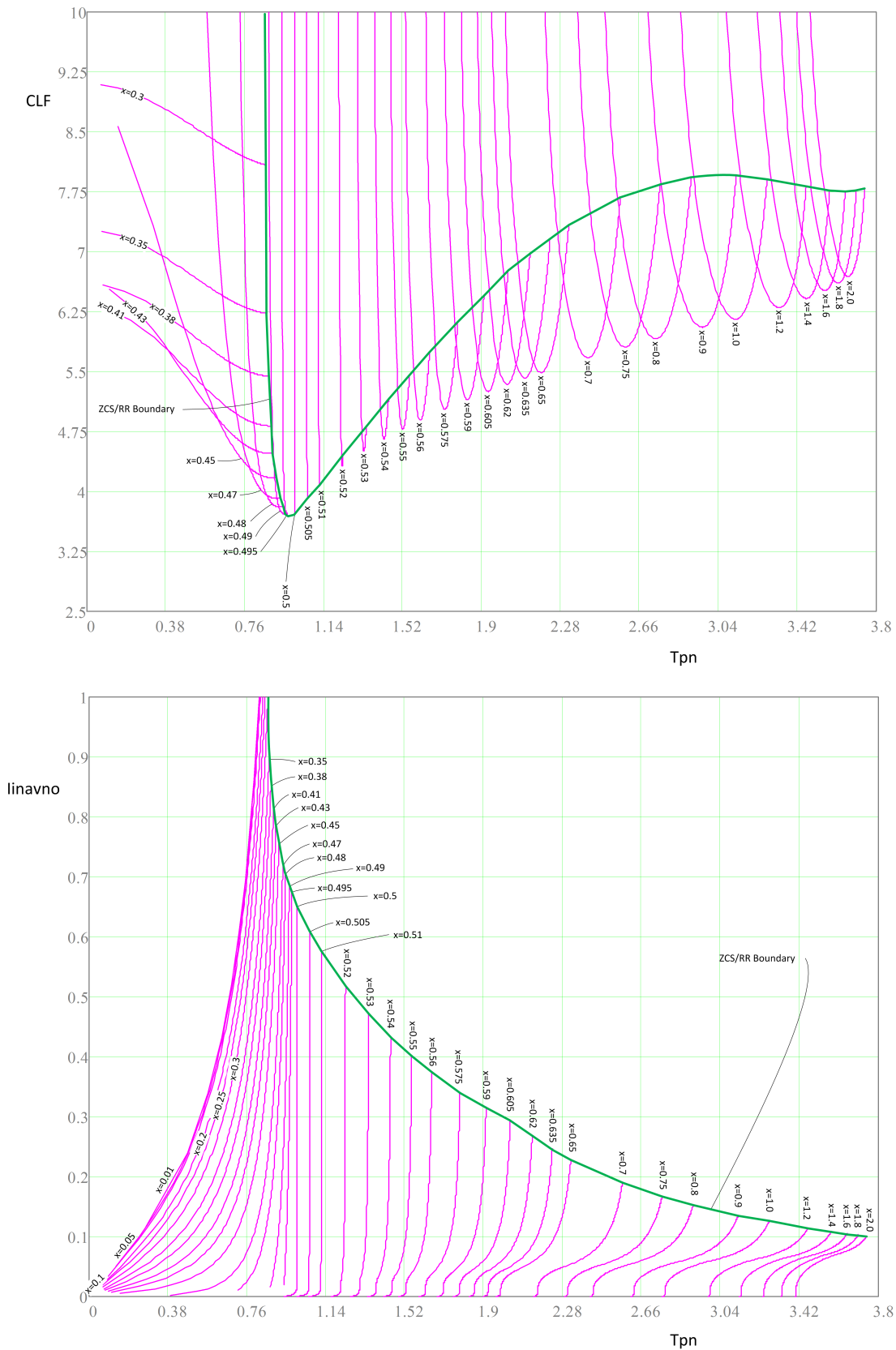


Figure 23. LLC Normalized Design Curves for Inductor Ratio $I_m = 15$

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