

# Easy Configuration of BQ76942, BQ76952 Battery Monitors



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## ABSTRACT

This application report contains a variety of information to assist the user in configuring the BQ769x2 family of battery monitors (which includes the BQ76942 and BQ76952). The document provides multiple examples of common configurations to help to user gain familiarity with the device settings.

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## 1 Introduction

The BQ769x2 family of battery monitors includes many configuration options to serve a wide range of applications. This document uses the BQ76942 Evaluation Module and [Battery Management Studio](#) to demonstrate several different configuration examples. These examples can also be applied to all devices in the BQ769x2 family. This document also includes an example .gg file which can be loaded onto an evaluation module using Battery Management Studio. The [BQ76942 Evaluation Module User's Guide](#) includes basic information on setting up the device, and this document should be used along with this guide.

## 2 Basic Configuration

After going through the Quick Start section of the [BQ76942 Evaluation Module User's Guide](#), refer to the following sections for the next steps on configuring the device. More detailed information for each feature is available in the device datasheet and TRM (Technical Reference Manual). Battery Management Studio also includes tool tips that give detailed descriptions of the different settings as the mouse pointer moves over different fields.

### 2.1 Regulator Settings

The BQ769x2 includes a 1.8-V regulator (REG18) and two LDOs (REG1 and REG2) with multiple voltage options. The REG18 supply is not configurable and is only used for internal circuitry, while REG1 and REG2 are configurable and can be used to power external circuitry. Multiple device features can reference REG1, so it is important for REG1 to be enabled for these features. The evaluation module also uses REG1 as a pull-up voltage for multiple pins, so it is recommended to enable the pre-regulator (REG0) and REG1.

The following example shows how to enable REG0, REG1, and REG2. REG1 and REG2 can be set to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V. The following example sets REG1 to 3.3 V and REG2 to 2.5 V. The options to configure REG1 and REG2 are also shown in [Figure 2-1](#).

Calibration	Name	Value	Unit
Settings	Configuration		
Power	Power Config	0102	Hex
System Data	REG12 Config	9d	Hex
Protections	REG0 Config	01	Hex
	HWD Regulator Options	00	Hex
	Comm Type	00	—
	I2C Address	00	—

REG0 Config								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	REG0_EH
Write to Data Memory								

REG12 Config								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	REG2V_2	REG2V_1	REG2V_0	REG2_EH	REG1V_2	REG1V_1	REG1V_0	REG1_EH
Write to Data Memory								

**REG1V\_2–REG1V\_0 (Bits 3–1)**

Selects voltage level for REG1 This setting should not be changed while REG1 is enabled.

Setting	Description
0–3	1.8 V
4	2.5 V
5	3 V
6	3.3 V
7	5 V

Figure 2-1. Enabling REG0, Enabling REG1 to 3.3 V and REG2 to 2.5 V

**2.2 Number of Cells**

The number of series cells for the application can be configured in the **Vcell Mode** register. The evaluation module includes a resistor divider to simulate cells for all cell inputs, so all cells can be enabled when using the evaluation module. To reduce the cell count, follow the instructions in the [BQ76942 Evaluation Module User's Guide](#) to update the hardware and update **VCell Mode** accordingly. In the following example, the cell count for BQ76942 is reduced to 8 cells to match the example in the Evaluation Module User's Guide.

Settings	DA Configuration	00	Hex
Power	Vcell Mode	033f	Hex
	CC3 Samples	80	Num
	Protection		

Vcell Mode								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	Cell 10 Mode	Cell 9 Mode
LSB	Cell 8 Mode	Cell 7 Mode	Cell 6 Mode	Cell 5 Mode	Cell 4 Mode	Cell 3 Mode	Cell 2 Mode	Cell 1 Mode
Write to Data Memory								

Figure 2-2. Configuring 8 Cells for BQ76942

## 2.3 Enabling Protections

Various device protections can be enabled through the **Enabled Protections A**, **Enabled Protections B**, and **Enabled Protections C** registers. In the default settings, only COV and SCD faults are enabled. In [Figure 2-3](#), all available protections are enabled. Additional registers can configure how the BQ76942 controls the CHG and DSG FETs in response to each protection being triggered. **CHG FET Protections A**, **CHG FET Protections B**, and **CHG FET Protections C** configure how the CHG FET should be controlled. **DSG FET Protection A**, **DSG FET Protection B**, and **DSG FET Protection C** configure how the DSG FET should be controlled.

When the CHG and DSG FETs are configured in series (these FETs are in series on the evaluation module), the **Body Diode Threshold** protection helps to prevent damage to the FETs. If the CHG FET is off and the device detects discharge current larger than this threshold, the CHG FET is turned on to protect the CHG FET body diode until the discharge current is removed. The reverse is true for the DSG FET when a charge current is detected above this threshold. This feature is not used if the FETs are configured in parallel. Configuration of FET control is covered more in [Section 2.8](#).

Secondary protections can react to more serious faults to take action to disable the pack. Configuration of Permanent Failures is very similar to the configuration of the primary protections. These can be configured through the Permanent Failure registers.

Calibration

Settings

Power

System Data

Protections

Permanent Fail

Security

Name	Value	Unit
▼ Protection		
Protection Configuration	0002	Hex
Enabled Protections A	1c	Hex
Enabled Protections B	17	Hex
Enabled Protections C	16	Hex
CHG FET Protections A	98	Hex
CHG FET Protections B	d5	Hex
CHG FET Protections C	56	Hex
DSG FET Protections A	e4	Hex
DSG FET Protections B	e6	Hex
DSG FET Protections C	e2	Hex
Body Diode Threshold	50	mA

  

**Enabled Protections A**

MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SCD	OCD2	OCD1	OCC	COV	CUV	RSVD_0	RSVD_0

Write to Data Memory

**Enabled Protections B**

MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	OTF	OTIIT	OTD	OTC	RSVD_0	UTIIT	UTD	UTC

Write to Data Memory

**Enabled Protections C**

MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	OCD3	SCDL	OCDL	COVL	RSVD	PTO	HWDF	RSVD_0

Write to Data Memory

**Figure 2-3. Enabling All Protections**

### 2.3.1 Voltage Protections

Voltage protections (over-voltage and under-voltage) can be enabled using **Enabled Protections A**. There are multiple parameters associated with each protection feature that can be adjusted based on the application. In the following example, the Threshold and Delay parameters for CUV (cell under-voltage) and COV (cell over-voltage) have been modified from the default values under the Protections settings. For example **CUV Threshold** can only be programmed in 50.6-mV increments and **CUV Delay** can only be programmed in 3.3-ms increments.

	Name	Value	Unit
<ul style="list-style-type: none"> <li>Calibration</li> <li>Settings</li> <li>Power</li> <li>System Data</li> <li style="border: 1px solid green; padding: 2px;">Protections</li> <li>Permanent Fail</li> </ul>	▼ CUV		
	Threshold	51	50.6mV
	Delay	33	3.3 ms
	Recovery Hysteresis	2	50.6mV
	▼ COV		
	Threshold	87	50.6mV
	Delay	33	3.3 ms
	Recovery Hysteresis	2	50.6mV

**Figure 2-4. Setting Voltage Protection Parameters**

### 2.3.2 Current Protections

Current protections (over-current and short-circuit detect) can be enabled under **Enabled Protections A** and **Enabled Protections C**. The parameters for each of these can be modified under the Protections settings. In the following example, several of the current protections parameters have been modified from the default values.

	Name	Value	Unit
<ul style="list-style-type: none"> <li>Calibration</li> <li>Settings</li> <li>Power</li> <li>System Data</li> <li style="border: 1px solid green; padding: 2px;">Protections</li> <li>Permanent Fail</li> <li>Security</li> </ul>	▼ OCC		
	Threshold	6	mV
	Delay	12	3.3 ms
	Recovery Threshold	-200	mA
	PACK-TOS Delta	2000	mV
	▼ OCD1		
	Threshold	10	mV
	Delay	6	3.3 ms
	▼ OCD2		
	Threshold	8	mV
	Delay	7	3.3 ms
	▼ SCD		
	Threshold	1	—
	Delay	15	µs
	Recovery Time	5	s
	▼ OCD3		
	Threshold	-5000	userA
Delay	2	s	
▼ OCD			
Recovery Threshold	200	mA	
▼ OCDL			

**Figure 2-5. Setting Current Protection Parameters**

### 2.3.3 Temperature Protections

Temperature protections can be enabled under **Enabled Protections B**. The parameters for each of these can be modified under the Protections settings. In the following example, the OTC (Over-temperature in charge) Threshold and OTD (Over-temperature in discharge) Threshold have been modified from the default values.

Protections	Recovery Threshold	200	mA
Permanent Fail	▼ OTC		
Security	Threshold	50	°C
	Delay	2	s
	Recovery	50	°C
	▼ OTD		
	Threshold	65	°C
	Delay	2	s
	Recovery	55	°C
	▼ OTF		
	Threshold	80	°C
	Delay	2	s
	Recovery	65	°C
	▼ OTINT		
	Threshold	85	°C
	Delay	2	s
	Recovery	80	°C
	▼ UTC		
	Threshold	0	°C
	Delay	2	s
	Recovery	5	°C
	▼ UTD		
	Threshold	0	°C
	Delay	2	s
	Recovery	5	°C
	▼ UTINT		
	Threshold	-20	°C
	Delay	2	s
	Recovery	-15	°C

**Figure 2-6. Setting Temperature Protection Parameters**

### 2.3.4 Other Protections

Pre-charge Timeout and Host Watchdog protections can be enabled under **Enabled Protections C**. In the following example, the HWD (Host Watchdog) fault delay and PTO (Precharge Timeout) delay have been modified from the default values.

▼ HWD			
Delay	65	s	
▼ Load Detect			
Active Time	0	s	
Retry Delay	50	s	
Timeout	1	hrs	
▼ PTO			
Charge Threshold	250	mA	
Delay	2000	s	
Reset	2	userAh	

**Figure 2-7. Setting PTO and HWD Parameters**

## 2.4 Thermistors

Several device pins have multiple functions. Some pins can be configured to interface with external thermistors in addition to the TSx pins. The following example shows TS1 configured for an external thermistor measuring a cell temperature, TS2 is unused, TS3 is configured for an external thermistor measuring FET temperature, and the HDQ pin is configured for an external thermistor where the temperature is reported but not used for protections. The thermistor pin settings are highly configurable, so refer to the data sheet if using a thermistor different from the default. (The default values are set to match the Semitec 103-AT and 204AP-2 thermistors.)

For detailed configuration options for thermistor pins, see the BQStudio tool tips or the device Technical Reference Manual.

Name	Value	Unit
TS1 Config	07	Hex
TS2 Config	00	Hex
TS3 Config	0f	Hex
HDQ Pin Config	0b	Hex

Figure 2-8. Enabling Additional Thermistors

## 2.5 General Purpose Outputs

Some device pins can be configured as GPOs (general purpose outputs). There are multiple options when setting the pins as GPOs. In the following example the CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins are configured to drive between 0 V and 3.3 V (voltage of REG1). The full list of commands to control each of the GPO pins is listed in the **General Purpose Digital Output Subcommands** table in the device data sheet. The description of each of the [OPT] register bits is described in the BQStudio tool tips as well as the **Multifunction Pin Options for ALT or GPO Pins** table in the device data sheet.

Name	Value	Unit
CFETOFF Pin Config	29	Hex
DFETOFF Pin Config	29	Hex
ALERT Pin Config	29	Hex
TS1 Config	07	Hex
TS2 Config	00	Hex
TS3 Config	0f	Hex
HDQ Pin Config	29	Hex
DCHG Pin Config	29	Hex
DDSG Pin Config	29	Hex

Figure 2-9. Enabling Multiple General Purpose Outputs

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PHL_FX01	PHL_FX10

Write to Data Memory

Figure 2-10. Setting CFETOFF as a GPO with Active-High Output Using REG1 High Drive Level

## 2.6 ADC Inputs

Multiple device pins can also be configured as general purpose ADC inputs. The following example demonstrates setting CFETOFF, DFETOFF, ALERT, TS1, TS2, TS3, HDQ, DCHG, and DDSG as general purpose ADC inputs. The BQStudio tool tips gives a detailed description for each of the [OPT] bits. When set as a general purpose ADC input, the [OPT] bits should always be set as shown in the following example (**OPT5, OPT3, OPT2** set to 1, **OPT4, OPT1, OPT0** set to 0).

Calibration*	Name	Value	Unit
Settings	CFETOFF Pin Config	b3	Hex
Power	DFETOFF Pin Config	b3	Hex
System Data	ALERT Pin Config	b3	Hex
Protections	TS1 Config	b3	Hex
Permanent Fail	TS2 Config	b3	Hex
	TS3 Config	b3	Hex
	HDQ Pin Config	b3	Hex
	DCHG Pin Config	b3	Hex
	DDSG Pin Config	b3	Hex

Figure 2-11. Enabling Multiple ADC Inputs

X HDO Pin Config								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FX01	PIN_FX10
Write to Data Memory								

Figure 2-12. Configuring the HDQ Pin as a General Purpose ADC Input

### 2.7 ALERT Pin

The ALERT pin can be configured to send an interrupt to the host to communicate when a fault is detected. The following example sets the ALERT pin as an active-high output referencing REG1 for the output voltage drive level. The PIN\_FXN bits configure the ALERT pin to function as an ALERT function.

Calibration*	Name	Value	Unit
Settings	ALERT Pin Config	2a	Hex
	TS1 Config	07	Hex

Figure 2-13. Configuring ALERT Pin Function

X ALERT Pin Config								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FX01	PIN_FX10
Write to Data Memory								

Figure 2-14. Setting ALERT with Active-High Output Using REG1 High Drive Level

There are many events that can be mapped to the ALERT pin to notify the host. The Default Alarm Mask register can be configured to control which events are mapped to the ALERT pin. The SF Alert Mask and PF Alert Mask registers can further control which safety alert and permanent fail alerts are mapped to the ALERT pin.

Settings*	Name	Value	Unit
Power*	Default Alarm Mask	f8fe	Hex
System Data	SF Alert Mask A	fc	Hex
Protections*	SF Alert Mask B	f7	Hex
Permanent Fail*	SF Alert Mask C	f6	Hex
	PF Alert Mask A	5f	Hex
	PF Alert Mask B	9f	Hex
	PF Alert Mask C	00	Hex
	PF Alert Mask D	00	Hex

Figure 2-15. Alarm Registers



X Default Alarm Mask								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	SSBC	SSA	PF	MSK_SFALERT	MSK_PFALERT	IIITSTART	IIITCOMP	RSVD_0
LSB	FULLSCAN	XCHG	XDSG	SHUTV	FUSE	CB	ADSCAH	WAKE

**Figure 2-16. Setting Events Mapped to ALERT Pin Using Default Alarm Mask Register**

## 2.8 FET Control Settings

There are multiple methods of FET control supported on the BQ769x2 devices. By default, the device will autonomously control the FETs based on fault conditions and recovery from these faults. The device can also be configured to allow the host to partially or fully control the FETs. This section describes some of the basic configurations.

Upon initial power-up of the device the FETs are disabled by default. Sending the **FET\_ENABLE** command will turn the FETs on. [Figure 2-17](#) shows the default settings for the **FET Options** register. In this configuration, the **FET\_CTRL\_EN** bit enables the device to enable the FETs. The **HOST\_FET\_EN** bit enables FET control commands from the host and also allows the host to use the CFETOFF and DFETOFF pins when those pins are configured to control the FETs. The **SFET** bit enables body diode protection for FETs configured in a series configuration like on the BQ76942 Evaluation Module.

X FET Options								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	RSVD_0	RSVD_0	FET_IHIT_OFF	PDSG_EN	FET_CTRL_EN	HOST_FET_EN	SLEEPCHG	SFET

Write to Data Memory

**Figure 2-17. FET Options Default Settings**

### 2.8.1 CFETOFF and DFETOFF

CFETOFF and DFETOFF can be set up to allow the host to disable the CHG and DSG FETs using these pins. The following example shows CFETOFF and DFETOFF configured as inputs to allow the host to disable the FETs using these pins.

Calibration		Name	Value	Unit
Settings		CFETOFF Pin Config	02	Hex
		DFETOFF Pin Config	02	Hex

**Figure 2-18. Configuring CFETOFF and DFETOFF for FET Control**

X CFETOFF Pin Config								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIH_FXH1	PIH_FXH0

Write to Data Memory

**Figure 2-19. CFETOFF Configuration Register**

### 2.8.2 DCHG and DDSG

The device can be configured to send a signal to the host processor or to external circuitry whenever fault conditions indicate the CHG and DSG FETs should be disabled through the DCHG and DDSG pins. In the following example, these pins are configured as active-high outputs with high drive level of REG1.

Calibration	Name	Value	Unit
Settings	DCHG Pin Config	2a	Hex
	DDSG Pin Config	2a	Hex

**Figure 2-20. Configuring DCHG and DDSG as Outputs to MCU**

X DCHG Pin Config								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FX01	PIN_FX10
<input type="button" value="Write to Data Memory"/>								

**Figure 2-21. DCHG Configuration Register**

### 3 GG File Example

Battery Management Studio allows the user to import and export images of all device register settings to text files with a .gg.csv extension. The following example configures the listed settings with the changes from the defaults highlighted in green. To use the following example, click on *Export -> Export Defaults* in the Data Memory screen of BQStudio with an EVM connected. The saved file can be edited with a text editor to make the highlighted changes and loaded onto the device using BQStudio by clicking *Import -> Import from a File*.

- Pre-regulator enabled, REG1 = 3.3 V, REG2 = 2.5 V
- CFETOFF and DFETOFF configured as inputs for FET Control
- DCHG and DDSG configured as active-high outputs to MCU
- ALERT configured as active-high output to MCU
- TS1 configured for cell temperature thermistor, TS3 configured for FET temperature thermistor, HDQ configured for temperature measurement without protections
- **VCell Mode** register set for 8 cells
- All protections enabled
- SOV and SUV permanent faults enabled
- **[FUSE]** bit set in **Default Alarm Mask** register
- **[SLEEPCHG]** bit set in FET Options register
- **[FET\_EN]** bit set in **Mfg Status Init** register

```
* Texas Instruments Data Flash File
* File created Thu Sep 17 15:10:54 2020
*
* Device Number 7694
* Firmware Version 0.36
* Build Number 39
* Order Number 0
*
* bqz Device Number 7692
* bqz Firmware Version 0.36
* bqz Build Number 39
*
* Field Order: Class name, Subclass name, Parameter name, Parameter Value, Display Units
"Calibration","Voltage","Cell 1 Gain","12120","-"
"Calibration","Voltage","Cell 2 Gain","12120","-"
"Calibration","Voltage","Cell 3 Gain","12120","-"
"Calibration","Voltage","Cell 4 Gain","12120","-"
"Calibration","Voltage","Cell 5 Gain","12119","-"
"Calibration","Voltage","Cell 6 Gain","12119","-"
"Calibration","Voltage","Cell 7 Gain","12119","-"
"Calibration","Voltage","Cell 8 Gain","12119","-"
"Calibration","Voltage","Cell 9 Gain","12122","-"
"Calibration","Voltage","Cell 10 Gain","12122","-"
"Calibration","Voltage","Pack Gain","34067","-"
"Calibration","Voltage","TOS Gain","33961","-"
"Calibration","Voltage","LD Gain","34268","-"
"Calibration","Voltage","ADC Gain","4039","-"
"Calibration","Current","CC Gain","1.000","mΩ"
"Calibration","Current","Capacity Gain","1.000","mΩ"
"Calibration","Vcell Offset","Vcell Offset","0","mV"
"Calibration","V Divider Offset","Vdiv Offset","0","userV"
"Calibration","Current Offset","Coulomb Counter Offset Samples","64","-"
"Calibration","Current Offset","Board Offset","0","-"
"Calibration","Temperature","Internal Temp Offset","0.0","°C"
"Calibration","Temperature","CFETOFF Temp Offset","0.0","°C"
"Calibration","Temperature","DFETOFF Temp Offset","0.0","°C"
"Calibration","Temperature","ALERT Temp Offset","0.0","°C"
"Calibration","Temperature","TS1 Temp Offset","0.0","°C"
"Calibration","Temperature","TS2 Temp Offset","0.0","°C"
"Calibration","Temperature","TS3 Temp Offset","0.0","°C"
"Calibration","Temperature","HDQ Temp Offset","0.0","°C"
"Calibration","Temperature","DCHG Temp Offset","0.0","°C"
"Calibration","Temperature","DDSG Temp Offset","0.0","°C"
"Calibration","Internal Temp Model","Int Gain","25390","-"
"Calibration","Internal Temp Model","Int base offset","3032","-"
"Calibration","Internal Temp Model","Int Maximum AD","16383","-"
```

```

"Calibration","Internal Temp Model","Int Maximum Temp","6379","0.1K"
"Calibration","18K Temperature Model","Coeff a1","-15524","-"
"Calibration","18K Temperature Model","Coeff a2","26423","-"
"Calibration","18K Temperature Model","Coeff a3","-22664","-"
"Calibration","18K Temperature Model","Coeff a4","28834","-"
"Calibration","18K Temperature Model","Coeff a5","672","-"
"Calibration","18K Temperature Model","Coeff b1","-371","-"
"Calibration","18K Temperature Model","Coeff b2","708","-"
"Calibration","18K Temperature Model","Coeff b3","-3498","-"
"Calibration","18K Temperature Model","Coeff b4","5051","-"
"Calibration","18K Temperature Model","Adc0","11703","-"
"Calibration","180K Temperature Model","Coeff a1","-17513","-"
"Calibration","180K Temperature Model","Coeff a2","25759","-"
"Calibration","180K Temperature Model","Coeff a3","-23593","-"
"Calibration","180K Temperature Model","Coeff a4","32175","-"
"Calibration","180K Temperature Model","Coeff a5","2090","-"
"Calibration","180K Temperature Model","Coeff b1","-2055","-"
"Calibration","180K Temperature Model","Coeff b2","2955","-"
"Calibration","180K Temperature Model","Coeff b3","-3427","-"
"Calibration","180K Temperature Model","Coeff b4","4385","-"
"Calibration","180K Temperature Model","Adc0","17246","-"
"Calibration","Custom Temperature Model","Coeff a1","0","-"
"Calibration","Custom Temperature Model","Coeff a2","0","-"
"Calibration","Custom Temperature Model","Coeff a3","0","-"
"Calibration","Custom Temperature Model","Coeff a4","0","-"
"Calibration","Custom Temperature Model","Coeff a5","0","-"
"Calibration","Custom Temperature Model","Coeff b1","0","-"
"Calibration","Custom Temperature Model","Coeff b2","0","-"
"Calibration","Custom Temperature Model","Coeff b3","0","-"
"Calibration","Custom Temperature Model","Coeff b4","0","-"
"Calibration","Custom Temperature Model","Rc0","0","-"
"Calibration","Custom Temperature Model","Adc0","0","-"
"Calibration","Current Deadband","Coulomb Counter Deadband","9","234nV"
"Calibration","CUV","CUV Threshold Override","ffff","Hex"
"Calibration","COV","COV Threshold Override","ffff","Hex"
"Settings","Fuse","Min Blow Fuse Voltage","5000","mV"
"Settings","Fuse","Fuse Blow Timeout","30","s"
"Settings","Configuration","Power Config","2982","Hex"
"Settings","Configuration","REG12 Config","9d","Hex"
"Settings","Configuration","REG0 Config","01","Hex"
"Settings","Configuration","HWD Regulator Options","00","Hex"
"Settings","Configuration","Comm Type","00","-"
"Settings","Configuration","I2C Address","00","-"
"Settings","Configuration","SPI Configuration","20","-"
"Settings","Configuration","Comm Idle Time","0","s"
"Settings","Configuration","CFETOFF Pin Config","02","Hex"
"Settings","Configuration","DFETOFF Pin Config","02","Hex"
"Settings","Configuration","ALERT Pin Config","2a","Hex"
"Settings","Configuration","TS1 Config","07","Hex"
"Settings","Configuration","TS2 Config","00","Hex"
"Settings","Configuration","TS3 Config","0f","Hex"
"Settings","Configuration","HDQ Pin Config","0b","Hex"
"Settings","Configuration","DCHG Pin Config","2a","Hex"
"Settings","Configuration","DDSG Pin Config","2a","Hex"
"Settings","Configuration","DA Configuration","05","Hex"
"Settings","Configuration","Vcell Mode","033f","Hex"
"Settings","Configuration","CC3 Samples","80","Num"
"Settings","Protection","Protection Configuration","0002","Hex"
"Settings","Protection","Enabled Protections A","fc","Hex"
"Settings","Protection","Enabled Protections B","f7","Hex"
"Settings","Protection","Enabled Protections C","f6","Hex"
"Settings","Protection","CHG FET Protections A","98","Hex"
"Settings","Protection","CHG FET Protections B","d5","Hex"
"Settings","Protection","CHG FET Protections C","56","Hex"
"Settings","Protection","DSG FET Protections A","e4","Hex"
"Settings","Protection","DSG FET Protections B","e6","Hex"
"Settings","Protection","DSG FET Protections C","e2","Hex"
"Settings","Protection","Body Diode Threshold","50","mA"
"Settings","Alarm","Default Alarm Mask","f808","Hex"
"Settings","Alarm","SF Alert Mask A","fc","Hex"
"Settings","Alarm","SF Alert Mask B","f7","Hex"
"Settings","Alarm","SF Alert Mask C","f4","Hex"
"Settings","Alarm","PF Alert Mask A","5f","Hex"
"Settings","Alarm","PF Alert Mask B","9f","Hex"
"Settings","Alarm","PF Alert Mask C","00","Hex"
"Settings","Alarm","PF Alert Mask D","00","Hex"
"Settings","Permanent Failure","Enabled PF A","03","Hex"

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"Settings","Permanent Failure","Enabled PF B","00","Hex"
"Settings","Permanent Failure","Enabled PF C","07","Hex"
"Settings","Permanent Failure","Enabled PF D","00","Hex"
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"Settings","FET","Chg Pump Control","01","Hex"
"Settings","FET","Precharge Start Voltage","0","mV"
"Settings","FET","Precharge Stop Voltage","0","mV"
"Settings","FET","Predischarge Timeout","5","10ms"
"Settings","FET","Predischarge Stop Delta","500","mV"
"Settings","Current Thresholds","Dsg Current Threshold","100","userA"
"Settings","Current Thresholds","Chg Current Threshold","50","userA"
"Settings","Cell Open-Wire","Check Time","5","s"
"Settings","Interconnect Resistances","Cell 1 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 2 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 3 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 4 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 5 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 6 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 7 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 8 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 9 Interconnect","0","mΩ"
"Settings","Interconnect Resistances","Cell 10 Interconnect","0","mΩ"
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"Settings","Cell Balancing Config","Balancing Configuration","00","Hex"
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"Settings","Cell Balancing Config","Max Cell Temp","60","°C"
"Settings","Cell Balancing Config","Max Internal Temp","70","°C"
"Settings","Cell Balancing Config","Cell Balance Interval","20","s"
"Settings","Cell Balancing Config","Cell Balance Max Cells","1","Num"
"Settings","Cell Balancing Config","Cell Balance Min Cell V (Charge)","3900","mV"
"Settings","Cell Balancing Config","Cell Balance Min Delta (Charge)","40","mV"
"Settings","Cell Balancing Config","Cell Balance Stop Delta (Charge)","20","mV"
"Settings","Cell Balancing Config","Cell Balance Min Cell V (Relax)","3900","mV"
"Settings","Cell Balancing Config","Cell Balance Min Delta (Relax)","40","mV"
"Settings","Cell Balancing Config","Cell Balance Stop Delta (Relax)","20","mV"
"Power","Shutdown","Shutdown Cell Voltage","0","mV"
"Power","Shutdown","Shutdown Stack Voltage","6000","mV"
"Power","Shutdown","Low V Shutdown Delay","1","s"
"Power","Shutdown","Shutdown Temperature","85","°C"
"Power","Shutdown","Shutdown Temperature Delay","5","s"
"Power","Shutdown","FET Off Delay","0","0.25s"
"Power","Shutdown","Shutdown Command Delay","0","0.25s"
"Power","Shutdown","Auto Shutdown Time","0","min"
"Power","Shutdown","RAM Fail Shutdown Time","5","s"
"Power","Sleep","Sleep Current","20","mA"
"Power","Sleep","Voltage Time","5","s"
"Power","Sleep","Wake Comparator Current","500","mA"
"Power","Sleep","Sleep Hysteresis Time","10","s"
"Power","Sleep","Sleep Charger Voltage Threshold","20000","mV"
"Power","Sleep","Sleep Charger PACK-TOS Delta","2000","mV"
"System Data","Integrity","Config RAM Signature","0000","Hex"
"Protections","CUV","Threshold","50","50.6mV"
"Protections","CUV","Delay","74","3.3 ms"
"Protections","CUV","Recovery Hysteresis","2","50.6mV"
"Protections","COV","Threshold","86","50.6mV"
"Protections","COV","Delay","74","3.3 ms"
"Protections","COV","Recovery Hysteresis","2","50.6mV"
"Protections","COVL","Latch Limit","0","-"
"Protections","COVL","Counter Dec Delay","10","s"
"Protections","COVL","Recovery Time","15","s"
"Protections","OCC","Threshold","4","mV"
"Protections","OCC","Delay","4","3.3 ms"
"Protections","OCC","Recovery Threshold","-200","mA"
"Protections","OCC","PACK-TOS Delta","2000","mV"
"Protections","OCD1","Threshold","8","mV"
"Protections","OCD1","Delay","1","3.3 ms"
"Protections","OCD2","Threshold","6","mV"
"Protections","OCD2","Delay","7","3.3 ms"
"Protections","SCD","Threshold","0","-"
"Protections","SCD","Delay","15","µs"
"Protections","SCD","Recovery Time","5","s"
"Protections","OCD3","Threshold","-4000","userA"
"Protections","OCD3","Delay","2","s"
"Protections","OCD","Recovery Threshold","200","mA"
"Protections","OCDL","Latch Limit","0","-"
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"Protections", "OCDL", "Recovery Threshold", "200", "mA"
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"Protections", "Load Detect", "Retry Delay", "50", "s"
"Protections", "Load Detect", "Timeout", "1", "hrs"
"Protections", "PTO", "Charge Threshold", "250", "mA"
"Protections", "PTO", "Delay", "1800", "s"
"Protections", "PTO", "Reset", "2", "userAh"
"Permanent Fail", "CUDEP", "Threshold", "1500", "mV"
"Permanent Fail", "CUDEP", "Delay", "2", "s"
"Permanent Fail", "SUV", "Threshold", "2200", "mV"
"Permanent Fail", "SUV", "Delay", "5", "s"
"Permanent Fail", "SOV", "Threshold", "4500", "mV"
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"Permanent Fail", "TOS", "Threshold", "500", "mV"
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"Permanent Fail", "VIMR", "Check Voltage", "3500", "mV"
"Permanent Fail", "VIMR", "Max Relax Current", "10", "mA"
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"Permanent Fail", "VIMR", "Relax Min Duration", "100", "s"
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"Permanent Fail", "DFETF", "OFF Threshold", "-20", "mA"
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"Permanent Fail", "2LVL", "Delay", "5", "s"
"Permanent Fail", "LFOF", "Delay", "5", "s"
"Permanent Fail", "HWMX", "Delay", "5", "s"
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"Security", "Keys", "Unseal Key Step 1", "0414", "Hex"
"Security", "Keys", "Unseal Key Step 2", "3672", "Hex"
"Security", "Keys", "Full Access Key Step 1", "ffff", "Hex"
"Security", "Keys", "Full Access Key Step 2", "ffff", "Hex"

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## 4 References

- [BQ76942 Evaluation Module User's Guide](#)
- [BQ76952 Evaluation Module User's Guide](#)

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