Application Note

How to Co-Layout Three Common SOT-563 Package Pinouts

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ABSTRACT

Buck converter applications commonly require co-layout between devices with different pinouts due to the design flexibility this provides. This application note focuses on how to co-layout among three types of SOT-563 packages. First, the pinout of TPS56x252/7, TPS56x242/7, and TPS56x203/6 are compared. Next, the schematic design is introduced. Finally, this application design is verified based on experiments.

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Trademarks

1 Introduction

The TPS56x252/7, TPS56x242/7 and TPS56x203/6 are all single output, adaptive on-time, D-CAP3™ control mode, synchronous buck converter that require very low external component count in SOT-563 packages. However, each device's pinout is slightly different. This application note mainly discusses how to do co-layout among TPS56x252/7, TPS56x242/7, and TPS56x203/6.

2 Comparison of Pinout

Figure 2-1 shows TPS56x203/6 pinout with SOT-563 package. TPS56x203/6 pinout is quite common in the industry. Figure 2-2 shows TPS56x242/7 pinout with SOT-563 package which has been optimized. It integrates BST capacitor and add AGND for pin 4. Figure 2-3 shows TPS56x252/7 pinout with SOT-563 package. It integrates BST capacitor and add PG for pin 4. As shown in Table 2-1, these three device families have the same pin functionality aside from pin 4. With compatible external circuitry, co-layout can be achieved for the three packages.

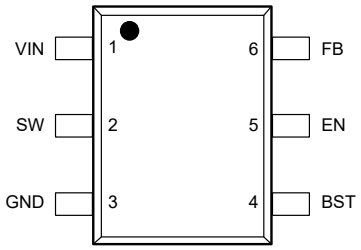

Figure 2-1. TPS56x203/6 Pinout

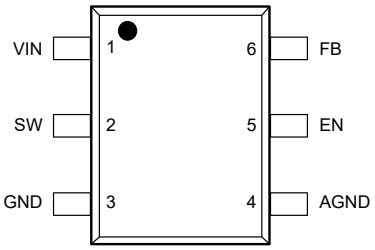

Figure 2-2. TPS56x242/7 Pinout

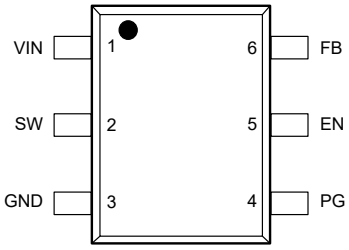

Figure 2-3. TPS56x252/7 Pinout

Table 2-1. Pin Functions

Pin		Description
No.	Name	
1	VIN	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
2	SW	Switch node pin. Connect the output inductor to this pin.
3	GND	GND pin source terminal of the low-side power NFET as well as the ground terminal for controller circuit.
4	PG	Open-drain power-good indicator.
	AGND	Ground of the internal analog circuitry. Connect AGND to the GND plane.
	BST	Supply input for the high-side NFET gate driver circuit. Connect 0.1-uF capacitor between BST and SW pins.
5	EN	Enable input control. Driving EN high enables the converter.
6	FB	Converter feedback input. Connect to the output voltage with a feedback resistor divider.

3 Schematic Diagram

3.1 How to Co-layout Among Three Types of SOT-563

Since pin 4 definitions are different for TPS56x252/7, TPS56x242/7, and TPS56x203/6, the compatible schematic is designed to achieve co-lay. Figure 3-1 shows the co-lay schematic. There are several differences for the BOM, also note that TPS56x203/6 allows EN pin to connect to Vin by only one pullup resistor. Table 3-1 shows solder information for different part. Table 3-2 shows comparison of EN pin configuration.

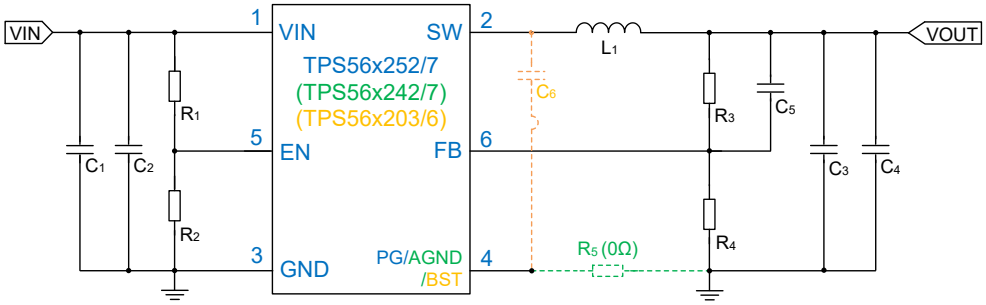

Figure 3-1. Co-layout Schematic Among Three Types of SOT-563

Table 3-1. Solder Information for Different Part

Part Number	Description
TPS56x252/7	1. If PG function is not needed, PG can be floating or connected with GND. PG tied to GND can get better thermal performance. 2. C_6 needs to be floating. R_5 can be soldered or floating. 3. EN pin max voltage is 6V, need two voltage divider resistors.
TPS56x242/7	1. R_5 needs to be soldered to connect AGND to GND. 2. C_6 needs to be floating. 3. EN pin max voltage is 6V, need two voltage divider resistors.
TPS56x203/6	1. C_6 needs to be tied to SW. 2. R_5 needs to be floating. 3. EN pin max voltage is 6V, allow two voltage resistors or one 100k pullup resistor.

Table 3-2. Comparison of EN Pin Configuration

Part Number	TPS56325x/TPS56425x	TPS562242	TPS56x203/6	TPS56x242/7
EN Default Status	Low	High	Low	Low
EN ABS Voltage	6V	6V	6V	6V
If Have A Zener Diode in Internal EN Pin	No	No	Yes	No
Support only 100k top resistor directly to Vin	No	No	Yes	No

3.2 How to Co-Layout Between TPS56x252/7 and TPS56x242/7

Figure 3-2 shows the co-lay schematic for TPS56x252/7 and TPS56x242/7. If PG function of TPS56x252/7 is not used, PG of TPS56x252/7 can be directly connected with GND and TPS56x252/7 and TPS56x242/7 are exactly pin to pin.

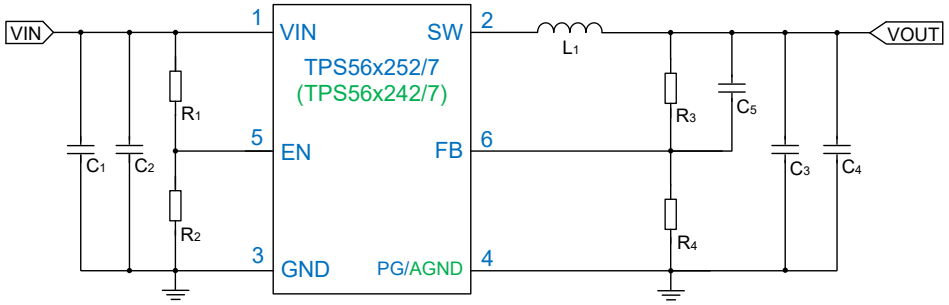

Figure 3-2. Co-Layout Schematic for TPS56x252/7 and TPS56x242/7

3.3 How to Co-layout Between TPS56x252/7 and TPS56x203/6

Figure 3-3 shows the co-lay schematic for TPS56x252/7 and TPS56x203/6. Table 3-3 shows solder information for TPS56x252/7 and TPS56x202/7.

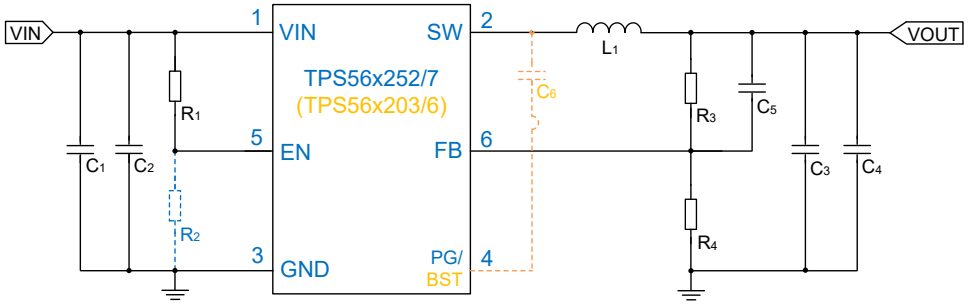

Figure 3-3. Co-layout Schematic for TPS56x252/7 and TPS56x203/6

Table 3-3. Solder Information for TPS56x252/7 and TPS56x203/6

Part Number	Description
TPS56x252/7	1. If PG function is not needed, PG can be floating or connected with GND. 2. C_6 needs to be floating. 3. EN pin max voltage is 6V, need two voltage divider resistors.
TPS56x203/6	1. C_6 needs to be tied to SW. 2. EN pin max voltage is 6V, allow two voltage resistors or one 100k pullup resistor.

3.4 How to Co-Layout Between TPS56x242/7 and TPS56x203/6

Figure 3-4 shows the co-lay schematic for TPS56x242/7 and TPS56x203/6. Table 3-4 shows solder information for TPS56x242/7 and TPS56x203/6.

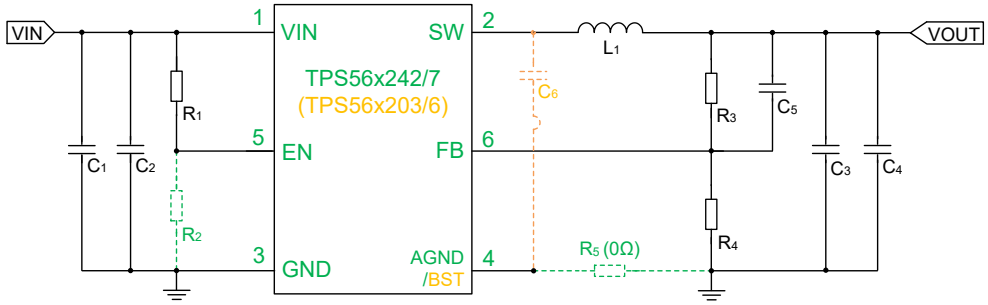

Figure 3-4. Co-Layout Schematic for TPS56x242/7 and TPS56x203/6

Table 3-4. Solder Information for TPS56x242/7 and TPS56x203/6

Part Number	Description
TPS56x242/7	1. R_5 needs to be soldered to connect AGND to GND. 2. C_6 needs to be floating. 3. EN pin max voltage is 6V, need two voltage divider resistors.
TPS56x203/6	1. C_6 needs to be tied to SW. 2. R_5 needs to be floating. 3. EN pin max voltage is 6V, allow two voltage resistors or one 100k pullup resistor.

4 Experimental Results

Figure 4-1, Figure 4-2, and Figure 4-3 are tested at 12V input voltage, 1.05V output voltage. All three devices work stably in steady state operation.

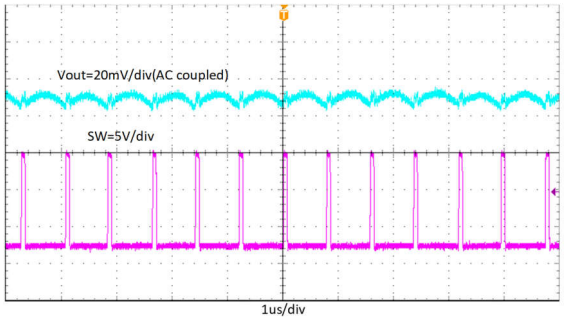

Figure 4-1. TPS564242 12V Input to 1.05V Output at 4A

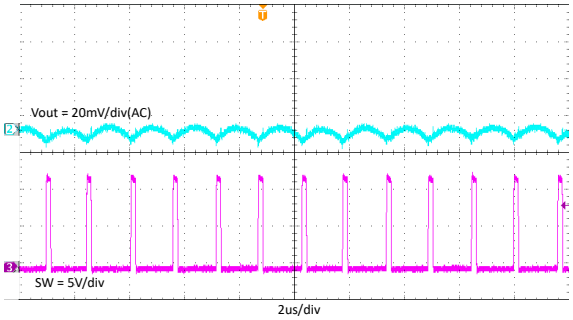

Figure 4-2. TPS563203 12V Input to 1.05V Output at 3A

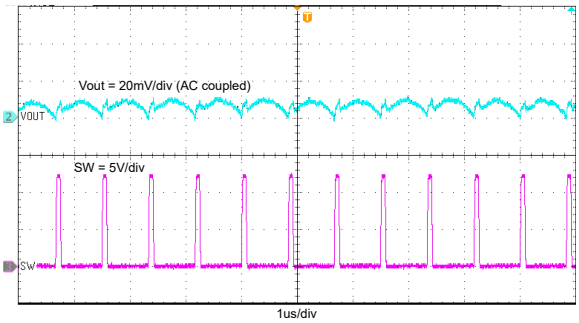

Figure 4-3. TPS563252 12V Input to 1.05V Output at 3A

5 Summary

This application note introduces how to co-layout among TPS56x252/7, TPS56x242/7, and TPS56x203/6 with SOT-563 package, which helps simplify the power design. Pinout is also compared and compatible schematic recommendations are given. Finally, the experiment verification results of the co-layout design proves all three devices can work stably in steady state operation.

6 References

- Texas Instruments, *TPS56325x 3-V to 16-V Input, 3-A Synchronous Buck Converters in SOT-563 Package* data sheet.
- Texas Instruments, *TPS56524x 3-V to 16-V Input Voltage, 5-A Synchronous Buck Converter in SOT-563 Package* data sheet.
- Texas Instruments, *TPS56424x 3-V to 16-V Input Voltage, 4-A Synchronous Buck Converter in SOT-563 Package* data sheet.
- Texas Instruments, *TPS56320x 4.2-V to 17-V Input, 3-A Synchronous Buck Converter in SOT563* data sheet.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2023) to Revision A (January 2024)	Page
• Replaced TPS56x202/7 with TPS56x203/6	1

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