Application Note

Layout Guide for Buck-Boost Charger BQ257XX Series

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ABSTRACT

This application note describes the optimized layout guide for the BQ257XX family of buck-boost charger solutions. BQ257XX family includes BQ2570X, BQ2571X, BQ2572X, BQ2573X. These products are synchronous NVDC buck-boost battery charge controller, offering a low component counts, high efficiency solution for space constrained, 1s~4s battery charging applications. In order for the chargers to perform optimally, certain layout rules should be followed. The rule of utilizing a good layout is to minimize the PCB trace inductance in the high di/dt current paths, to limit capacitive coupling from high dv/dt nodes onto other traces, and to ensure proper GND connections. By following the rules, designer will be able to achieve the best charger operation including low EMI, high accuracy, high efficiency, low temperature operation.

Table of Contents

List of Figures

Trademarks

1 Introduction

Buck-boost charger has 5 switches and one inductor. The proper layout design is the key to achieve the stable operation, good thermal and low EMI performance. But there are many layout challenges for circuit designers. A poor layout can result in low efficiency, reduced charging capability, reduced measurement accuracy, or even unstable operation due to noise interference. To overcome the challenges, TI BQ257XX EVM is a good starting point for a custom layout. There can be alternative methods however, this layout is proven and most likely provides the best operation of the device due to the optimization of PCB trace inductance and the suggested grounding method. Figure 1-1 shows the BQ25710 EVM circuit as an example for the layout guide in this application note.

1.1 BQ25710 EVM Circuit

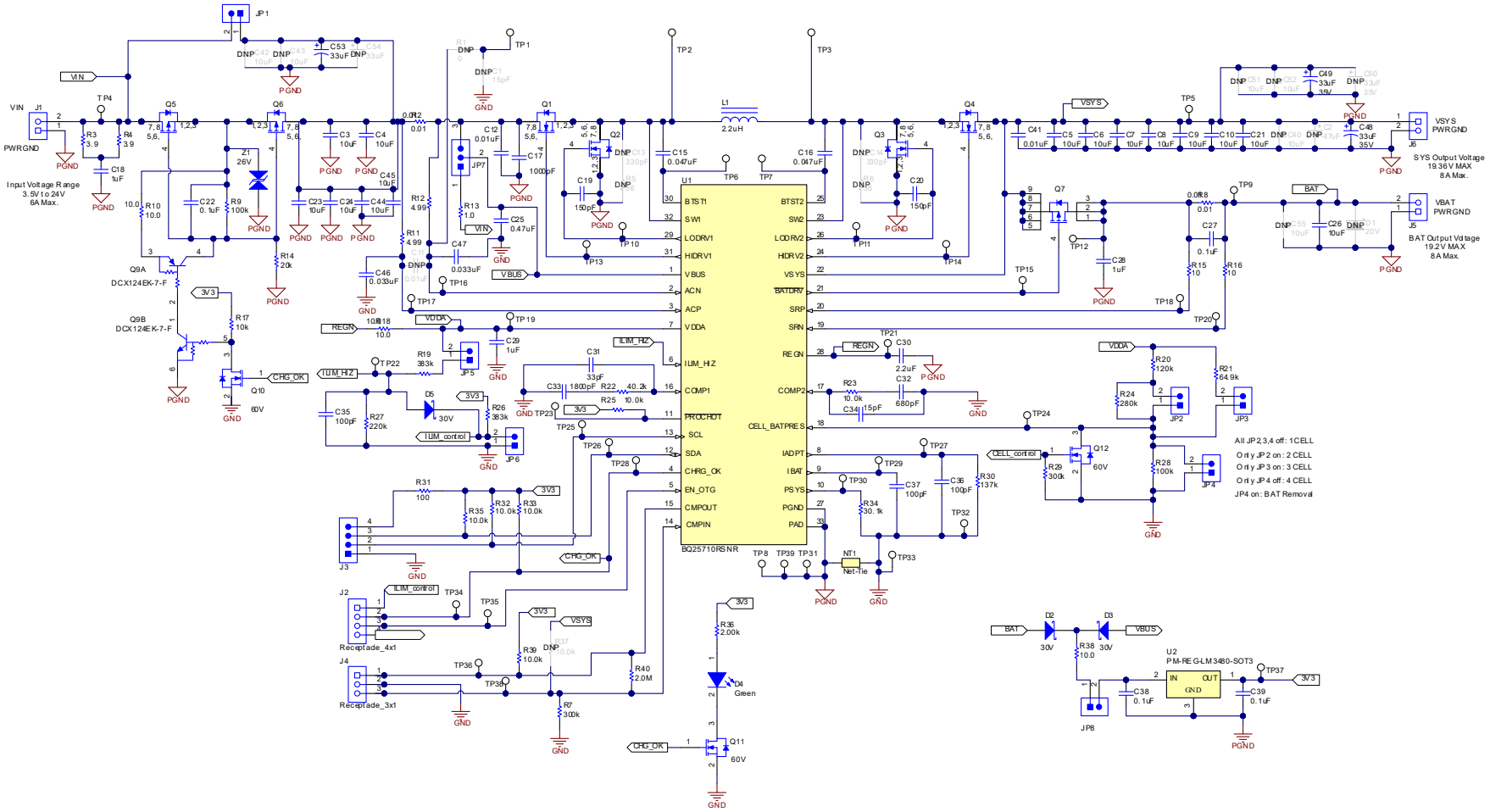

Figure 1-1. BQ25710 EVM Circuit

2 Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout guide based on priority for proper layout.

2.1 PCB Stack-Up (4 Layers)

For proper layout design, multi-layer PCB is suggested. The BQ257XX EVM uses a 4-layer PCB as shown in Figure 2-1. The top layer contains power traces and most signal lines. Any remaining area on top layer must be filled with ground and be connected to bottom and internal grounds by strong via connection through all layers. The internal layer 2 is ground only and layer 3 contains signal lines and ground. The bottom layer is used for additional non-critical signals and ground.

As shown in Figure 2-2, put ground near power components layer (Top layer) since that can be an effective shield to reduce inductive and capacitive coupling noise. If the ground layer is the next layer following the power stage layer, the ground layer copper gets the lowest thermal resistance, smallest high-frequency loop area and shield most of the rest circuit from the high-noise power stage. Also, if all high-current loop components are put on the same layer, the magnetic field lines are vertical to the board. So, the ground copper layer can provide the best shielding performance between the power stage circuit and other small signal circuits on the board.

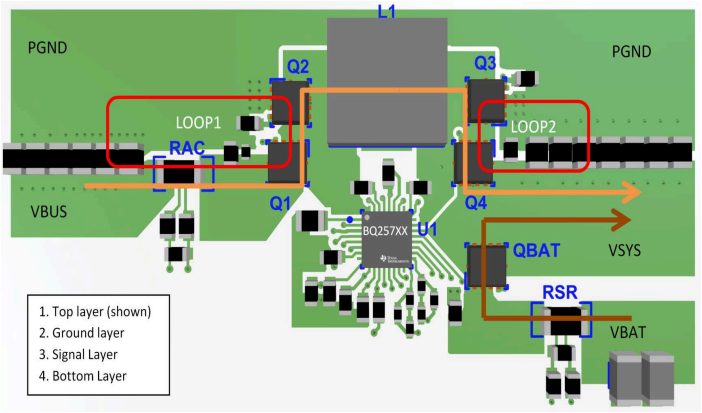

Figure 2-1. Layout Example for PCB Stack-Up and Top Side Components Placement

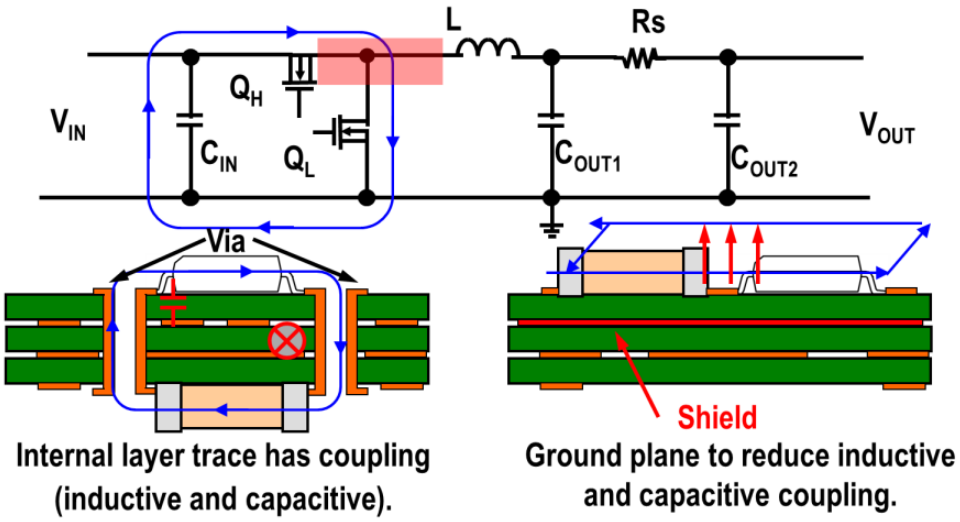

Figure 2-2. Power Stage Component Placement and Ground Layer

2.2 Identifying Critical Circuit Paths

The key to a successful layout is understanding the circuit by identifying these critical components:

- High di/dt paths
- High dv/dt nodes
- Sensitive traces

Figure 2-3 shows the high di/dt paths in the BQ25710 application diagram. The most dominant high di/dt loops are the input switching current loop and output switching current loop. The input loop consists of an input capacitor and MOSFETs (Q1 and Q2), The output loop consists of an output capacitor and MOSFETs (Q3 and Q4), along with return paths.

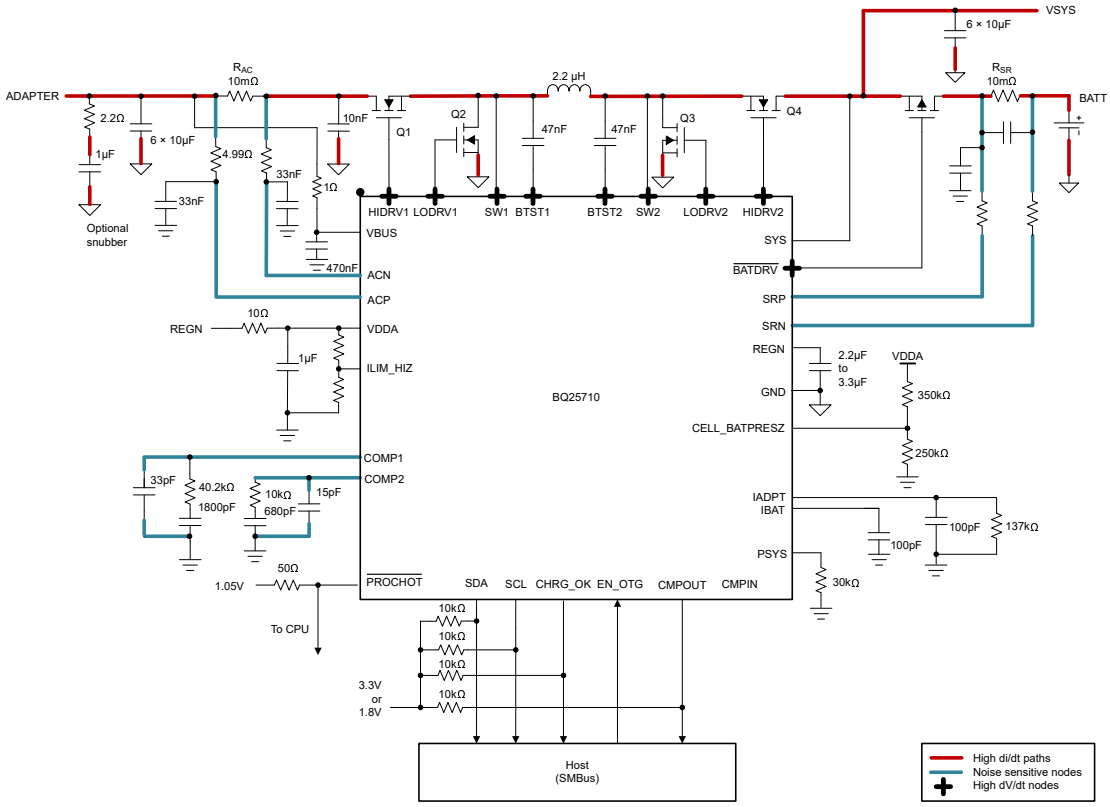

Figure 2-3. BQ25710 Application Diagram Identifying High di/dt Loops, High dv/dt Nodes and Sensitive Traces

The high dv/dt nodes are those with fast voltage transitions. These nodes are the switch nodes (SW1 and SW2), the bootstrap nodes (BTST1 and BTST2), and the gate-drive traces (HIDRV1, LODRV1, HIDRV2 and LODRV2). The areas of the switching nodes need to be as large as possible yet as small as possible for electrical noise reasons. If the SW1 and SW2 are poured with too big area copper planes, the high dv/dt noisy signal can couple into other traces nearby through capacitive coupling, which can cause EMI issues.

The current-sense traces from R_{AC}, R_{SR} to the IC pins (ACP, ACN, SRP and SRN) and the compensation components (COMP1 and COMP2) form the noise-sensitive traces. For good layout performance, optimize the surface areas of high dv/dt nodes, and keep the noise-sensitive traces away from the noisy (high di/dt and dv/dt) portions of the circuit and minimize the loop areas.

2.3 Input and Output Loop Placements Considering Noise, Efficiency, and Thermal Performance

Once the critical parts of layout are identified, the next task is to minimize any sources of noise and unwanted parasitic. The input-switching current loop and output-switching current loop are the dominant high current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance. Therefore, it's highly recommended to put the power components on same layer. Also Allow enough copper area for thermal dissipation. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat. Figure 2-4 shows the power components placement on top layer as a good example with BQ25710 EVM matching with the schematic shown in Figure 1-1.

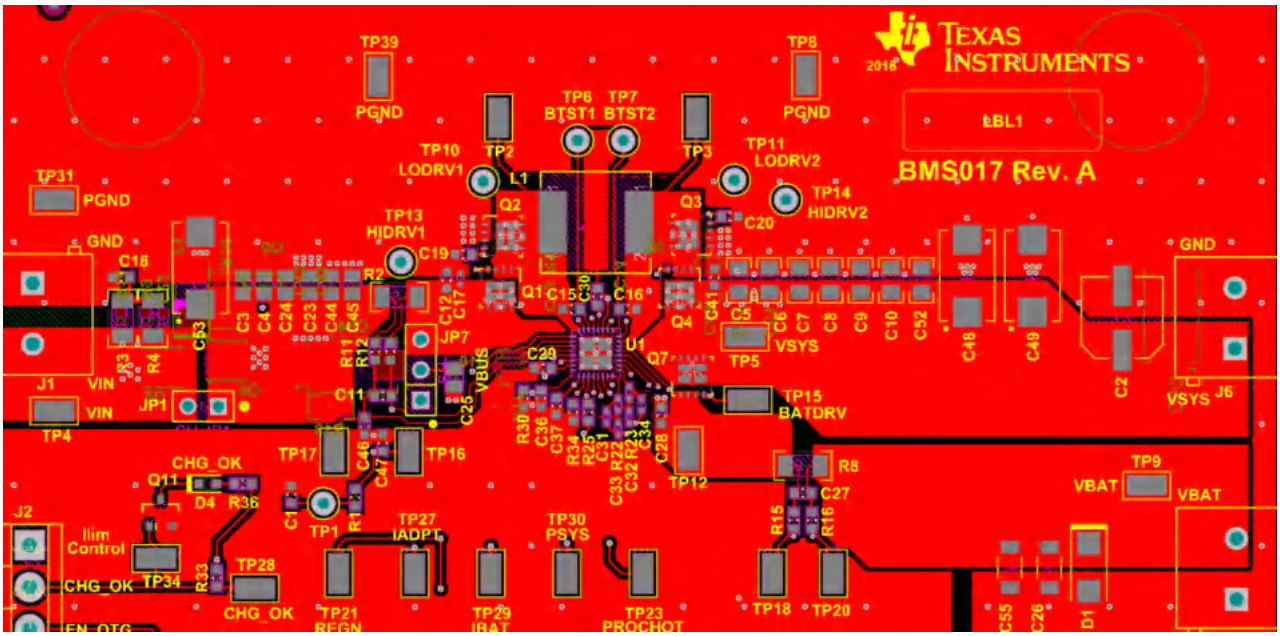

Figure 2-4. Power Components Placement on Top Layer

VBUS capacitors, R_{AC}, Q1 and Q2 form a small loop1. VSYS capacitors, Q3 and Q4 form a small loop 2. As shown in Figure 2-1, the most important loop areas to minimize on loop 1 and loop 2 are the path from the input capacitors through the buck high-side and low-side MOSFETs, and back to the ground connection of the input capacitor and the path from the output capacitors through the boost high-side and low-side MOSFETs, and back to the ground connection of the output capacitor. Connect the negative terminal of the capacitor close to the source of the low-side MOSFETs (at ground). Similarly, connect the positive terminal of the capacitor or capacitors close to the drain of the high-side MOSFETs of both loops. Especially 10nF + 1nF (0402 size) decoupling capacitors must be placed after R_{AC} as close as possible to FETs for decoupling switching loop high frequency noise.

Connect the power components with large copper to reduce the parasitic resistance. Since the current path from VBUS to VSYS and VBAT to VSYS has low impedance, pay attention to via resistance if not on the same layer. The number of vias can be estimated as 1 to 2A/via for a 10mil via with 1oz copper thickness. If high density design is required, you can move part of CBUS or CSYS to the other side of PCB. Lastly, we recommend to place QBAT and R_{SR} near the battery terminal since the device detects the battery voltage through SRN pin near battery terminal.

2.4 Kelvin Sensing Circuit for Current Sense to Achieve High Accuracy

Use Kelvin-sensing connections for R_{AC} and R_{SR} current sense resistors. Figure 2-5 shows an example of Kelvin-sensing technique for R_{SR} resistor. Put enough copper on high current path going through sensing resistor since the thin trace can cause an unexpected voltage drop on the board. Also keep in mind that non-kelvin connection can cause the different voltage across SRP and SRN compared to the voltage across sensing resistor. So, connect the current sense traces to the center of the pads and run current sense traces as differential pairs. To avoid noise getting picked up, put signal lines far away from noisy paths into inner layers.

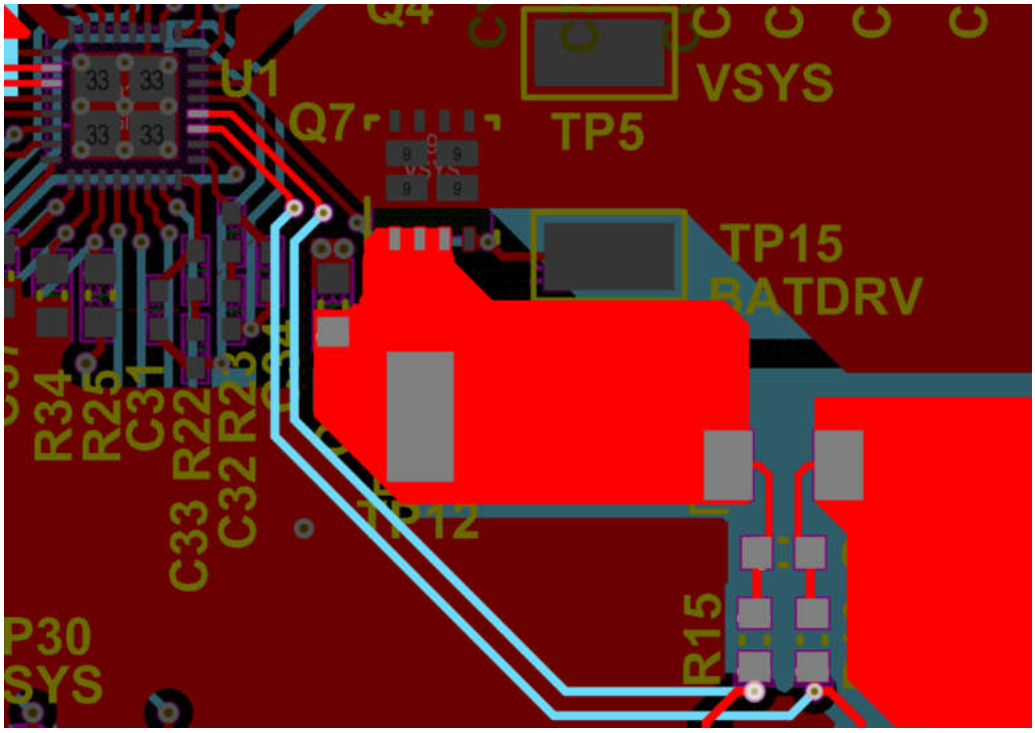

Figure 2-5. Kelvin Sensing Connections for R_{SR} Resistor

2.5 Small Capacitors Placements Considering Noise

Place REGN capacitor(C30), VBUS capacitor(C25), VDDA capacitor(C29) close to IC as shown in Figure 2-6. Use AGND for VBUS, VDDA capacitors and use PGND for REGN capacitor since REGN pin out is for power stage gate drive. Since REGN capacitor provides a low impedance path for the driver circuits in BQ25710, put REGN capacitor close to the IC to maintain the lowest impedance source for the fast di/dt required for IC's FET drivers.

Place high-side FET bootstrap circuit capacitors close to IC and on the same layer of PCB. As shown in Figure 2-7, capacitors on SW1/2 nodes are recommended to use wide copper polygon to connect to power stage and capacitors on BTST1/2 nodes are recommended to use at least 8mil trace to connected to BTST1/2 pins to reduce line parasitic inductance. Another R/C for signal pins must be placed close to the IC far away from high frequency noise. Add ground vias close to R/C to connect the ground of signal to ground plane.

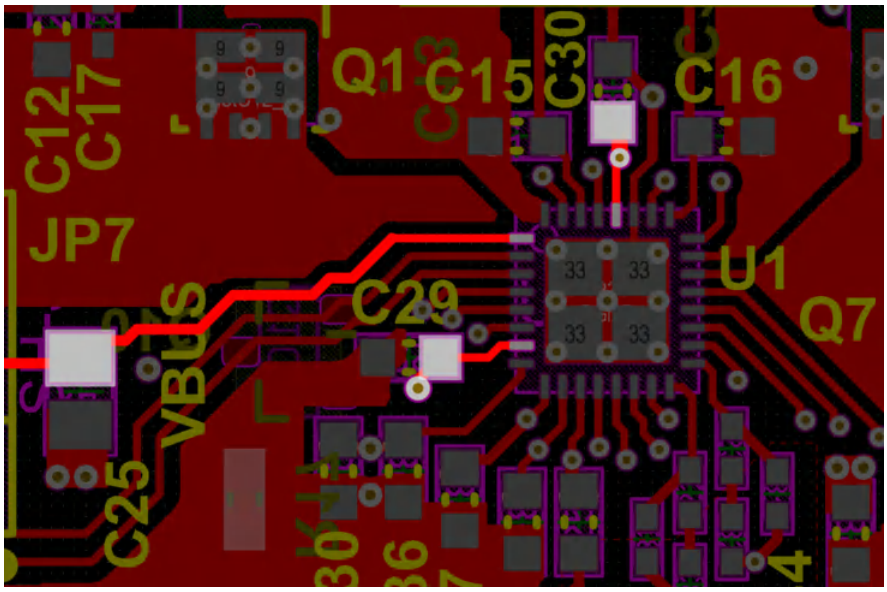

Figure 2-6. Capacitors Placement for VBUS, VDDA, REGN

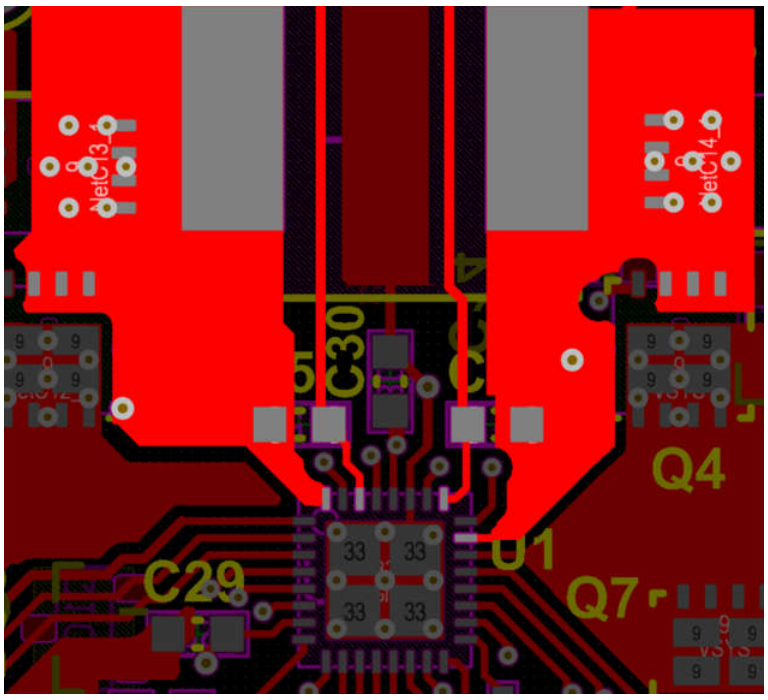

Figure 2-7. Capacitors for BTST1/2 pins

2.6 Separating AGND and PGND

Separate PGND and AGND first to avoid small signal ground coupling high current (high di/dt) ground noise. In power supply layout, separating the signal system is important, such as the feedback path which is susceptible to noise and the switching nodes that switch large current.

- AGND: a quiet ground reference for control signals (analog ground)
- PGND: a noisy ground reference for power signals (power ground)

AGND is used for all sensing, compensation, and control network ground for example: ACP/ACN/COMP1/COMP2/CMPIN/CMPOUT/IADPT/IBAT/PSYS. PGND is used as return path for power stage related large current signals.

Though the DC ground potential is the same, measure must be taken to separate these AGND and PGND planes to make sure noise arising from digital or high-power signals is not conducted between them to interfere with analog signals. As shown in Figure 1-1, we recommend to have two ground signs in the schematic already as difficulties arise when visualizing sensitive and noisy potentials on the layout if the same GND sign is used on the schematic. Therefore, we recommend starting with split GND in the schematic level and connect them with a net tie (NT1).

Figure 2-8 shows the connection between PGND and AGND with a net tie in PCB layout highlighting top layer (Red) and layer3 (Blue). AGND is used for control signals and must be closer to the IC and own a polygon. Connect all AGND to a dedicated low-impedance copper lane to make sure AGND and PGND are on the same potential and ultimately must be connected together at one point near the IC as shown in Figure 2-8 (like exposed power pad underneath the IC).

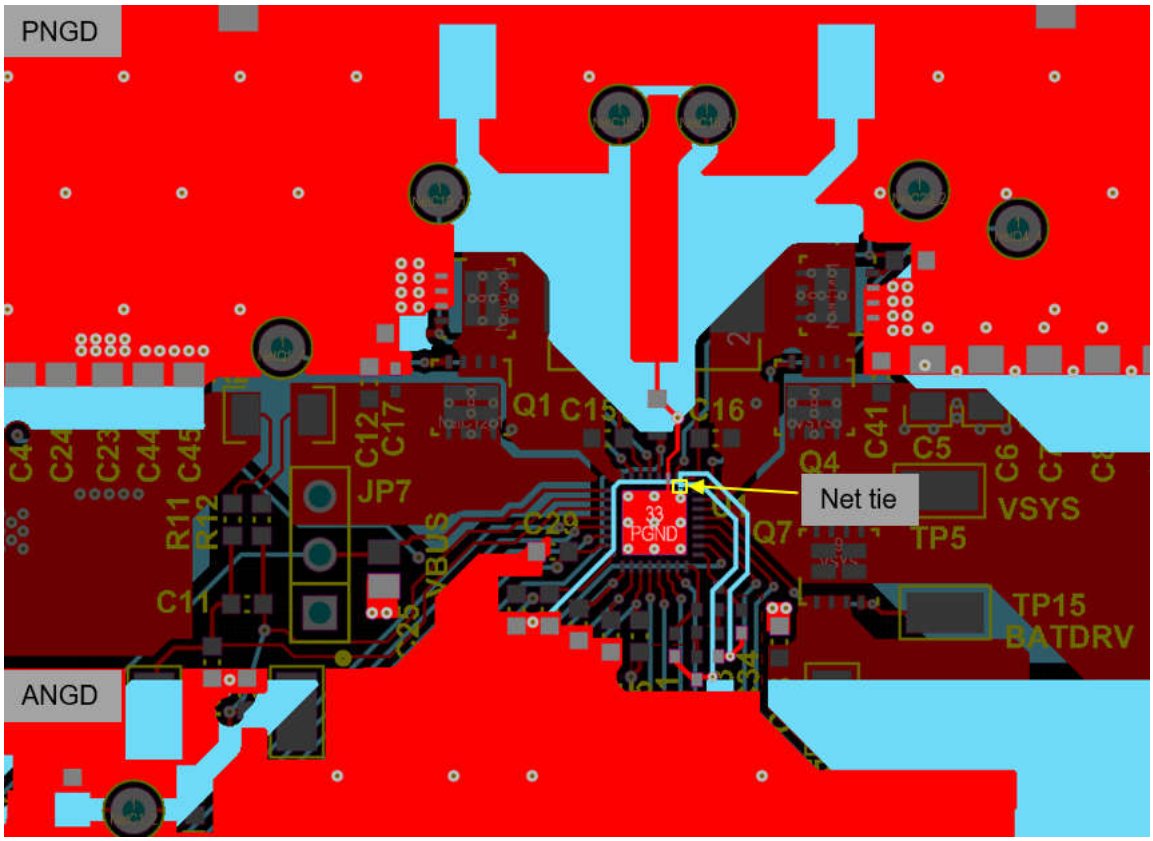

Figure 2-8. Separating AGND and PGND With Net-Tie

3 References

- Texas Instruments, *BQ25710 SMBus Narrow VDC Buck-Boost Battery Charge Controller With System Power Monitor and Processor Hot Monitor* data sheet.
- Texas Instruments, *bq2571x Evaluation Module* user's guide.
- Texas Instruments, *Layout Optimization of 4-Switch Buck-Boost Converters* application note.

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