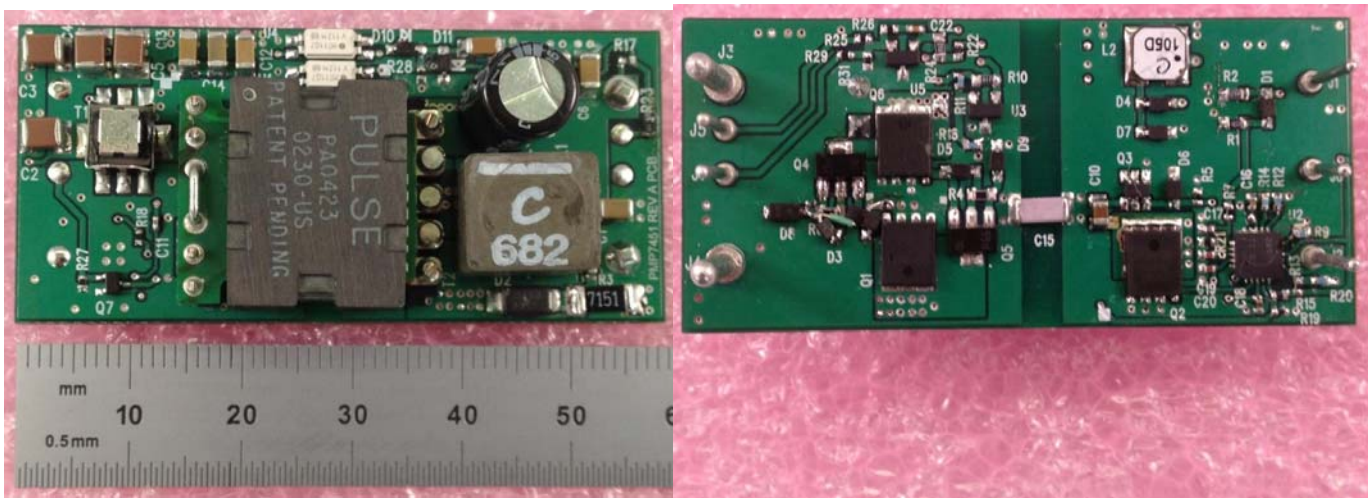
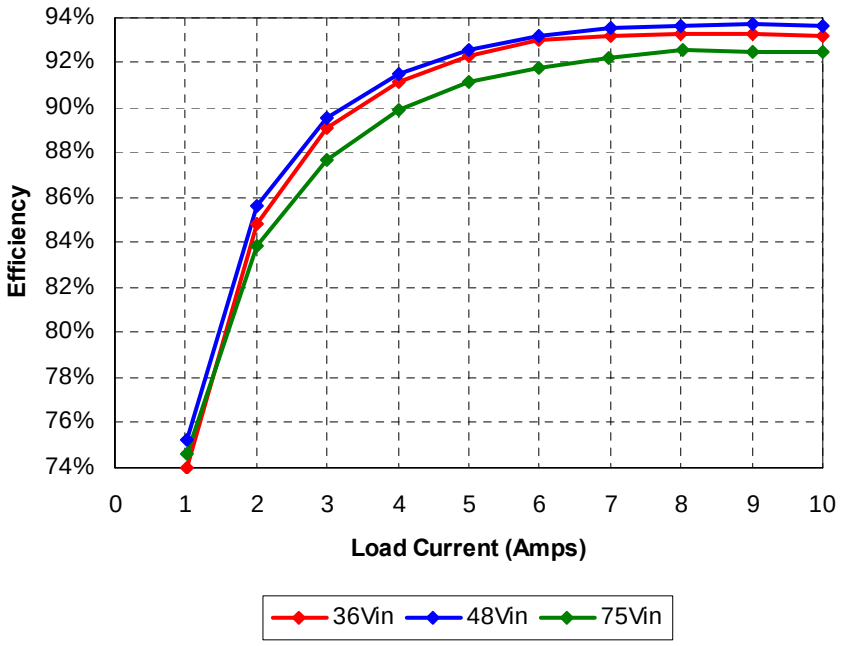
PMP7451 Rev B Test Results

1 Photo

The photographs below show the top and bottom views of the PMP7451 Rev B demo board. The circuit is built on a PMP7451 Rev A PWB.



2 Efficiency



PMP7451 Rev B Test Results

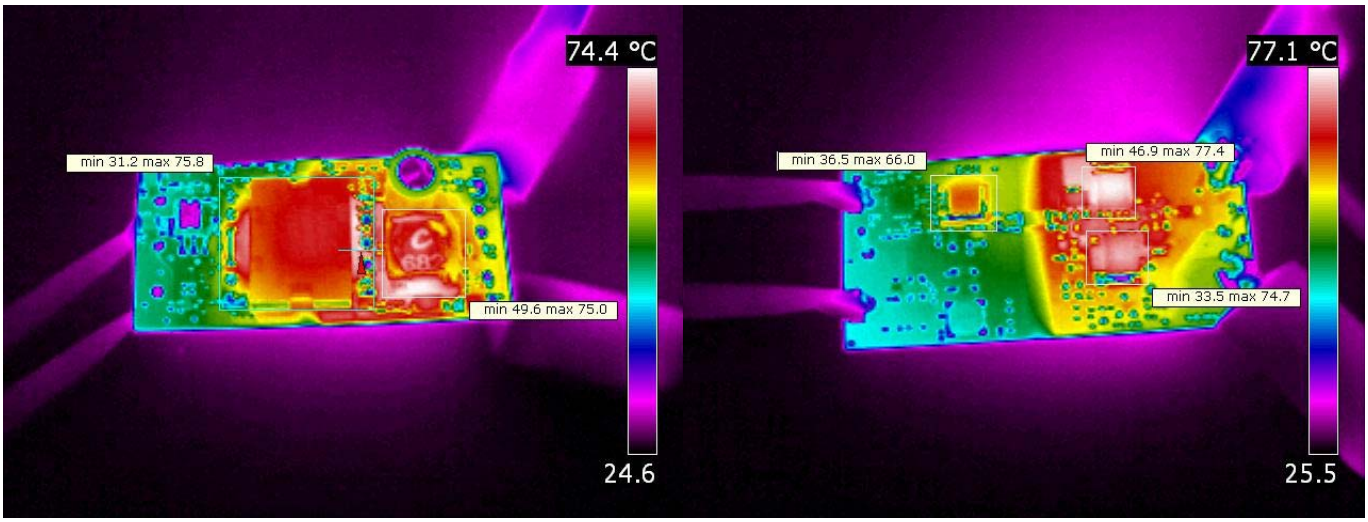
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.02	36.0	0.123	0.00	4.428	0.0%
1.009	12.04	36.0	0.456	12.15	4.268	74.0%
2.000	12.04	36.0	0.788	24.08	4.288	84.9%
2.987	12.04	36.0	1.121	35.96	4.393	89.1%
4.003	12.05	36.0	1.470	48.24	4.684	91.1%
4.998	12.05	36.0	1.812	60.23	5.006	92.3%
5.998	12.06	36.0	2.161	72.34	5.460	93.0%
7.01	12.06	36.0	2.519	84.54	6.143	93.2%
8.00	12.06	36.0	2.873	96.48	6.948	93.3%
9.01	12.07	36.0	3.237	108.75	7.781	93.3%
10.00	12.07	36.0	3.599	120.70	8.864	93.2%

Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.09	48.0	0.084	0.00	4.032	0.0%
1.007	12.09	48.0	0.337	12.17	4.001	75.3%
2.003	12.09	48.0	0.589	24.22	4.056	85.7%
2.996	12.08	48.0	0.842	36.19	4.224	89.5%
4.007	12.08	48.0	1.102	48.40	4.491	91.5%
5.002	12.08	48.0	1.360	60.42	4.856	92.6%
6.001	12.08	48.0	1.620	72.49	5.268	93.2%
7.00	12.08	48.0	1.883	84.56	5.824	93.6%
8.00	12.08	48.0	2.150	96.64	6.560	93.6%
9.01	12.08	48.0	2.420	108.84	7.319	93.7%
10.00	12.08	48.0	2.688	120.80	8.224	93.6%

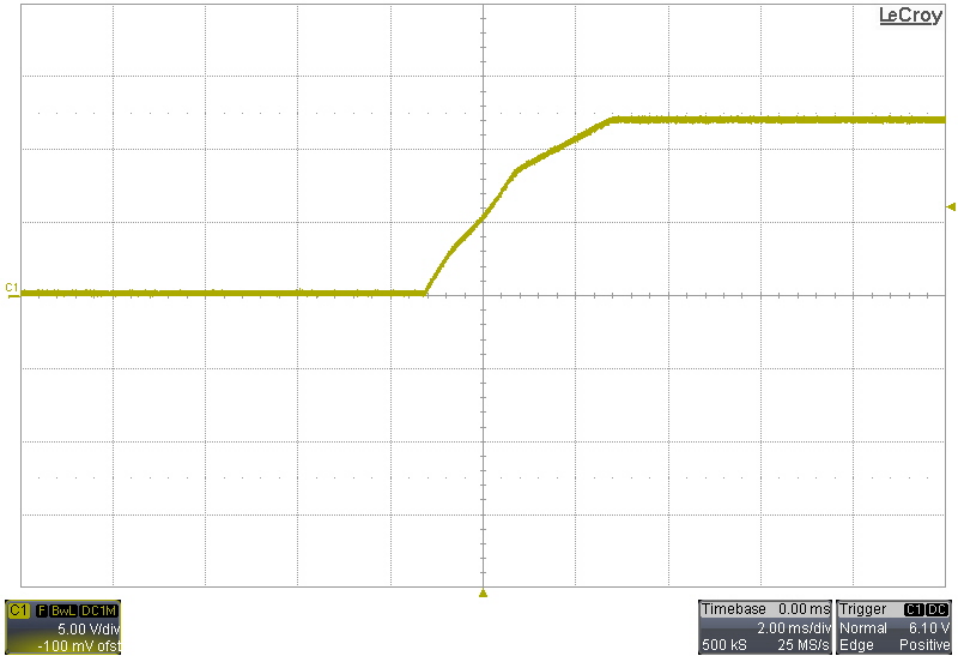
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.10	75.0	0.055	0.00	4.125	0.0%
1.005	12.09	75.0	0.217	12.15	4.125	74.7%
1.992	12.09	75.0	0.383	24.08	4.642	83.8%
2.992	12.09	75.0	0.550	36.17	5.077	87.7%
4.010	12.09	75.0	0.719	48.48	5.444	89.9%
5.008	12.09	75.0	0.886	60.55	5.903	91.1%
5.992	12.09	75.0	1.052	72.44	6.457	91.8%
6.98	12.09	75.0	1.220	84.39	7.112	92.2%
8.01	12.09	75.0	1.395	96.84	7.784	92.6%
9.01	12.09	75.0	1.571	108.93	8.894	92.5%
10.00	12.09	75.0	1.743	120.90	9.825	92.5%

3 Thermal Images

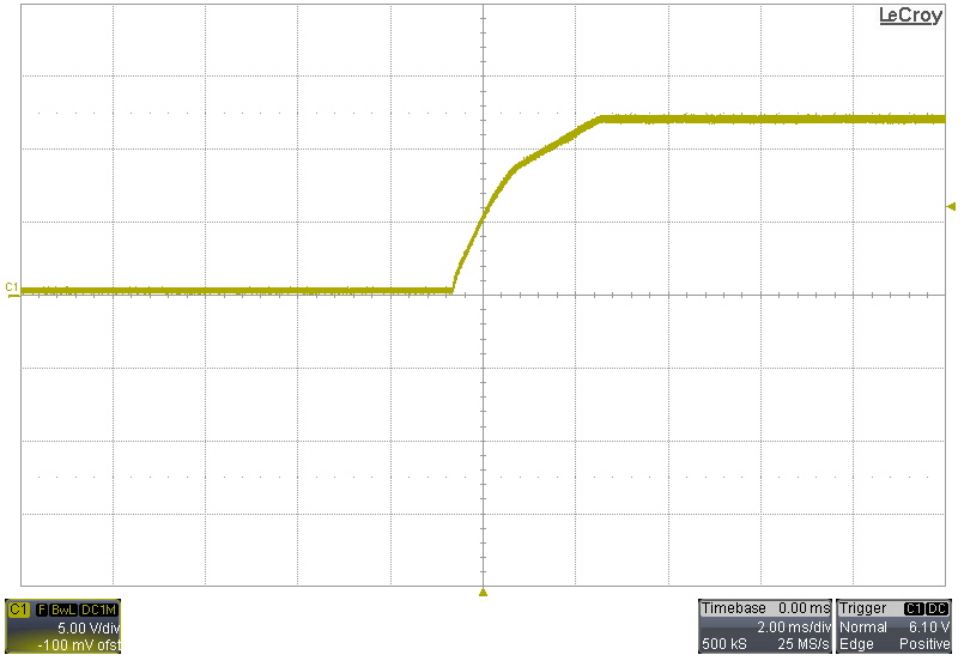
The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 25C with 100LFM of forced air flow. The input was 48VDC, and the output was loaded with 10A.



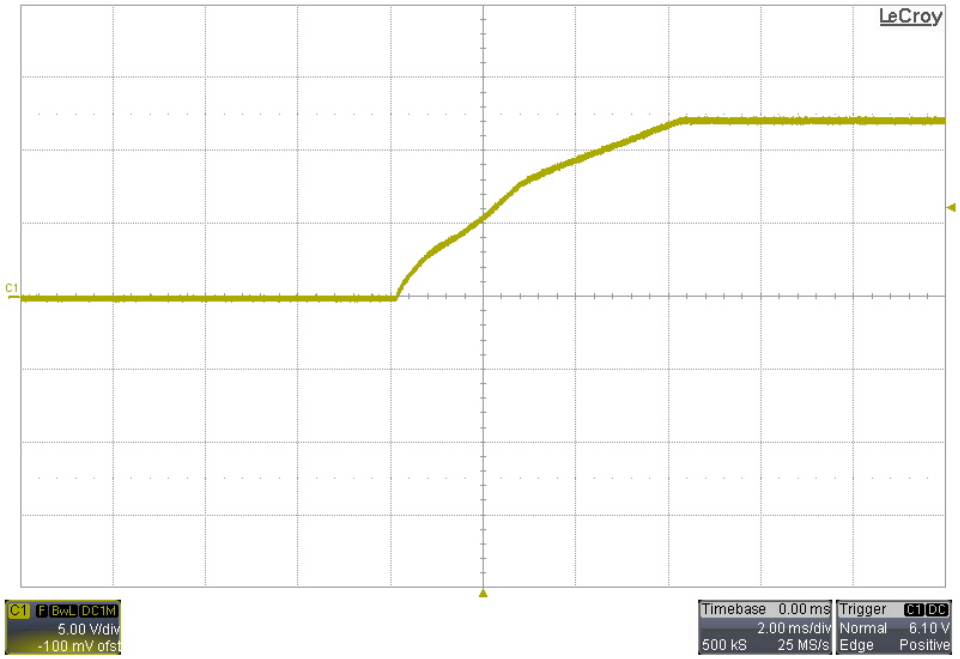
4 Startup – 36V Input, No Load



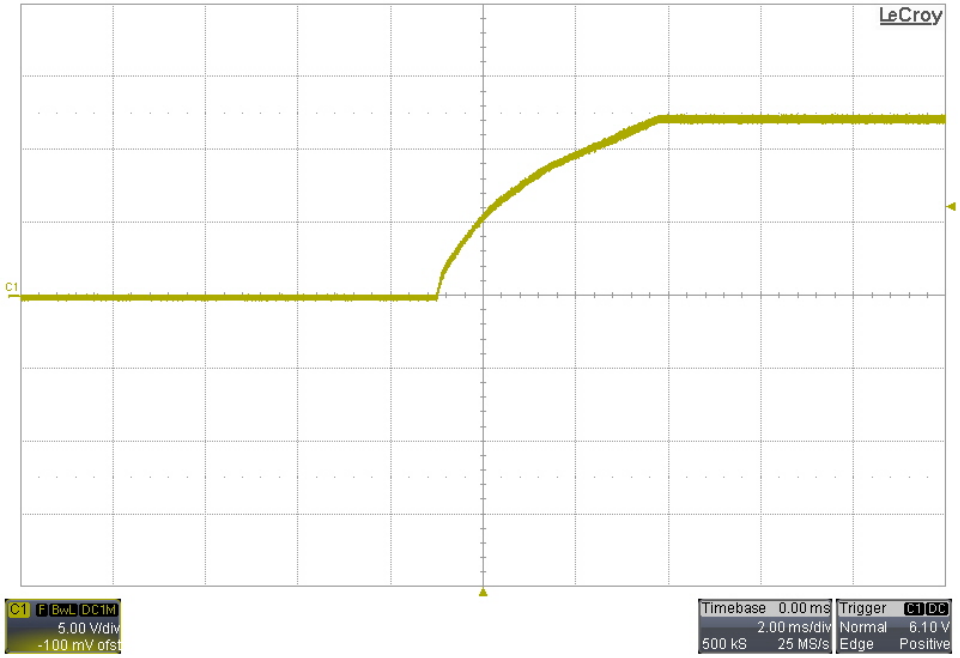
5 Startup – 75V Input, No Load



6 Startup – 36V Input, 2Ω Load



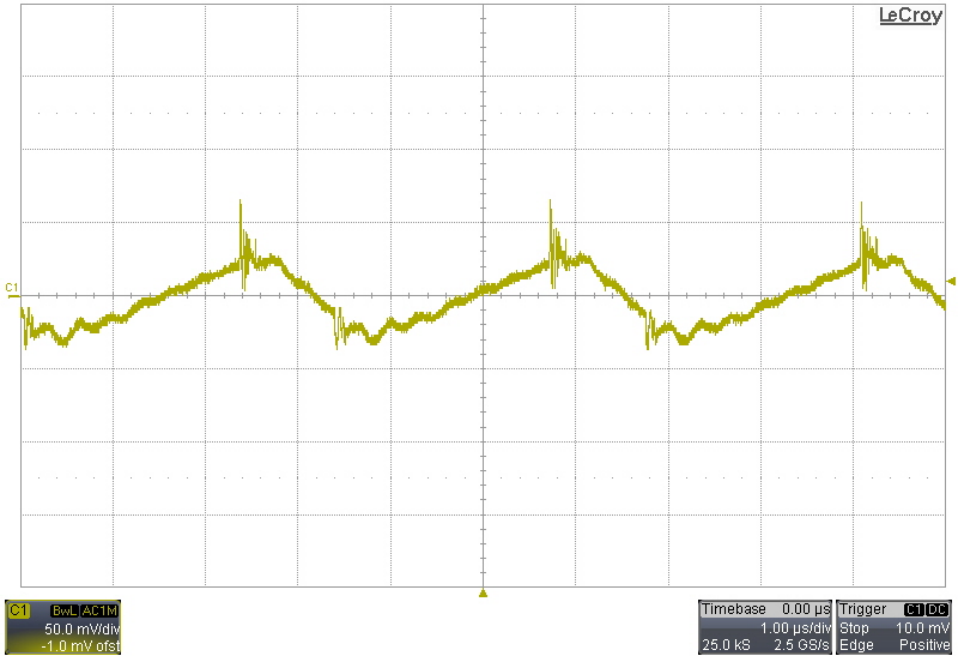
7 Startup – 75V Input, 2Ω Load



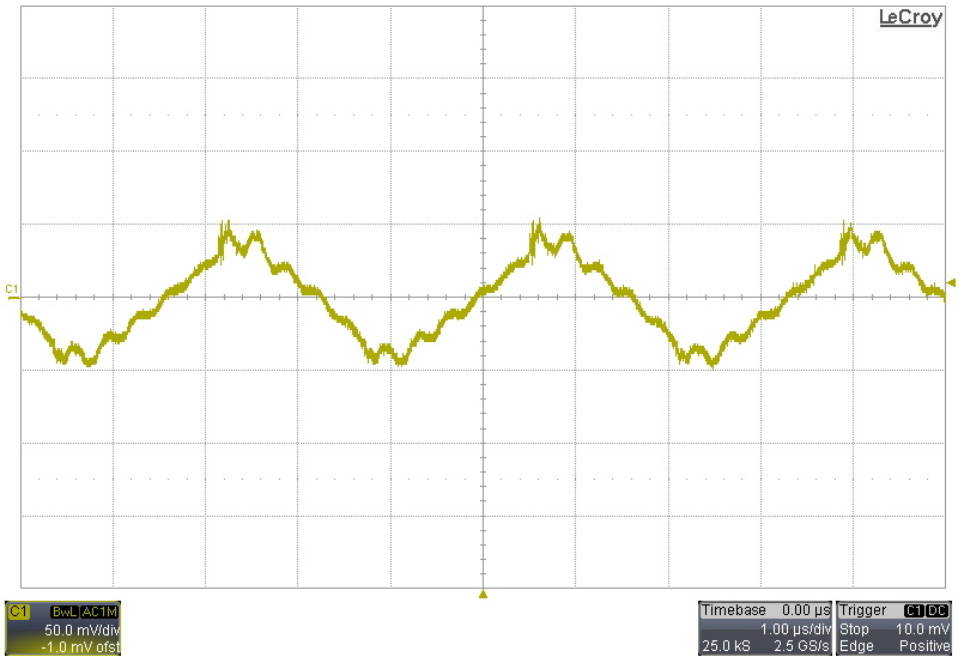
8 Output Ripple Voltage

The output ripple voltage is shown in the plots below. The output was loaded with 10A.

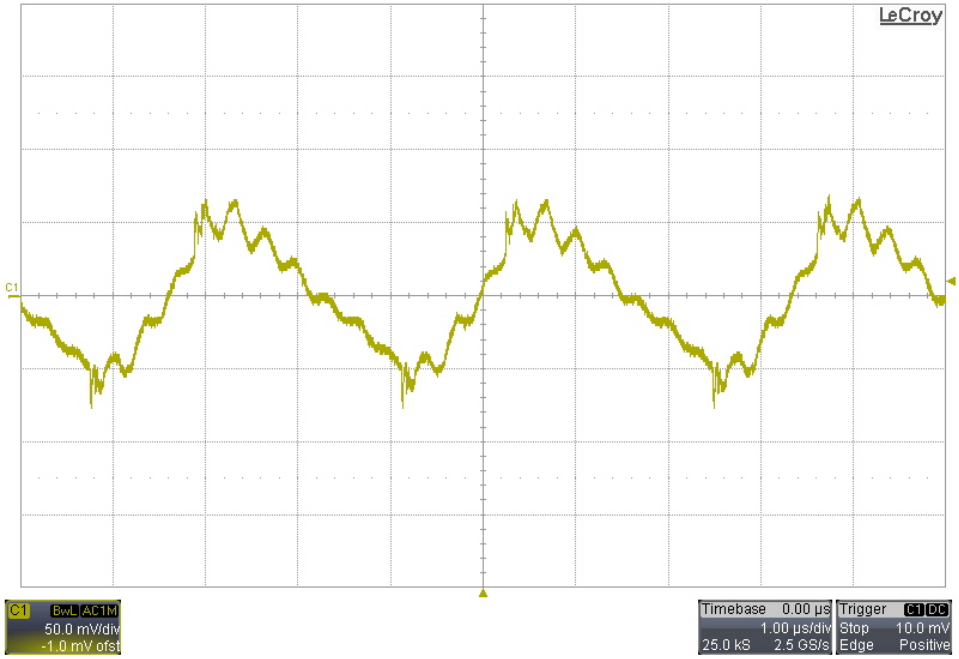
8.1 36V Input



8.2 48V Input



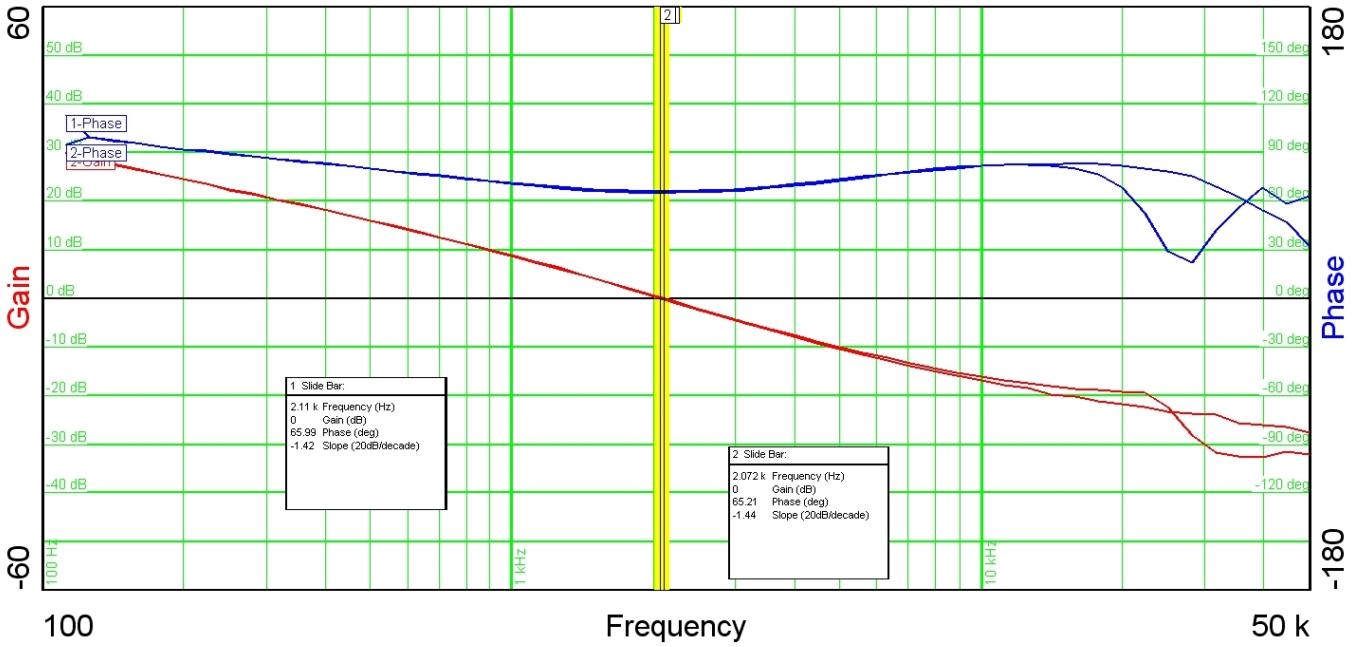
8.3 75V Input



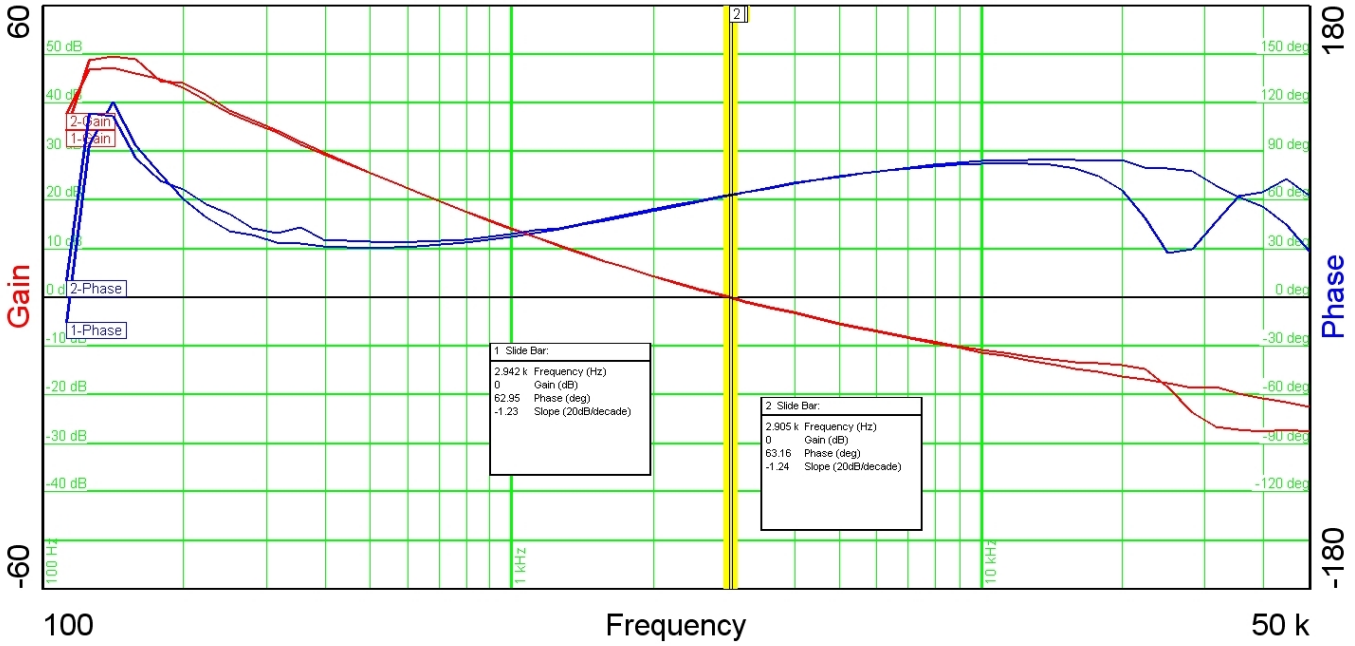
9 Frequency Response

The frequency response of the feedback loop is shown below. For the gain/phase plot #1, the input was set to 36V. For the gain/phase plot #2, the input was set to 75V. The output was loaded with 10A.

9.1 Measured Across R23



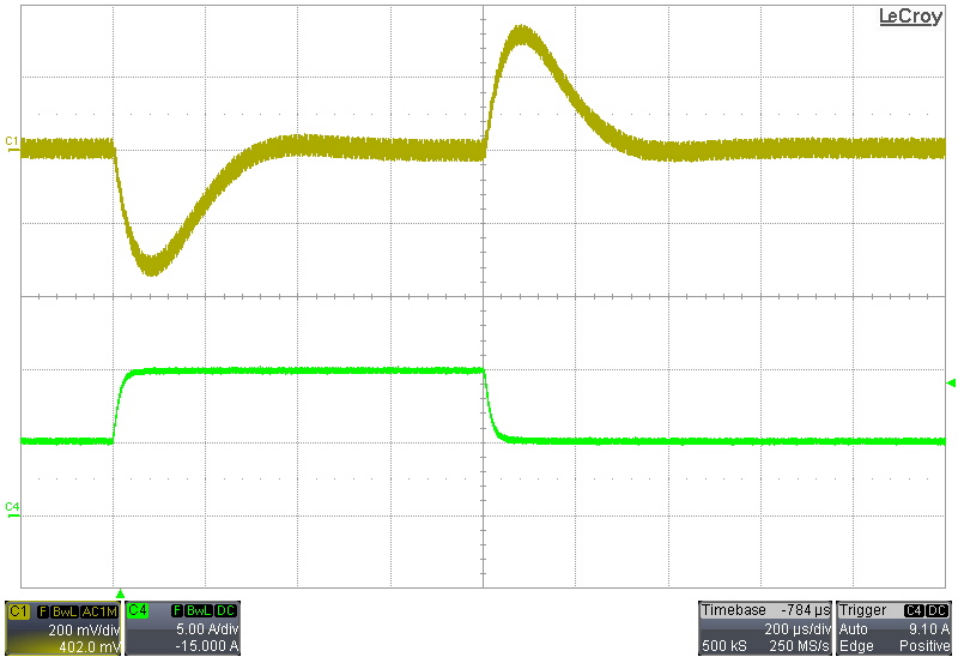
9.2 Measured Across R17



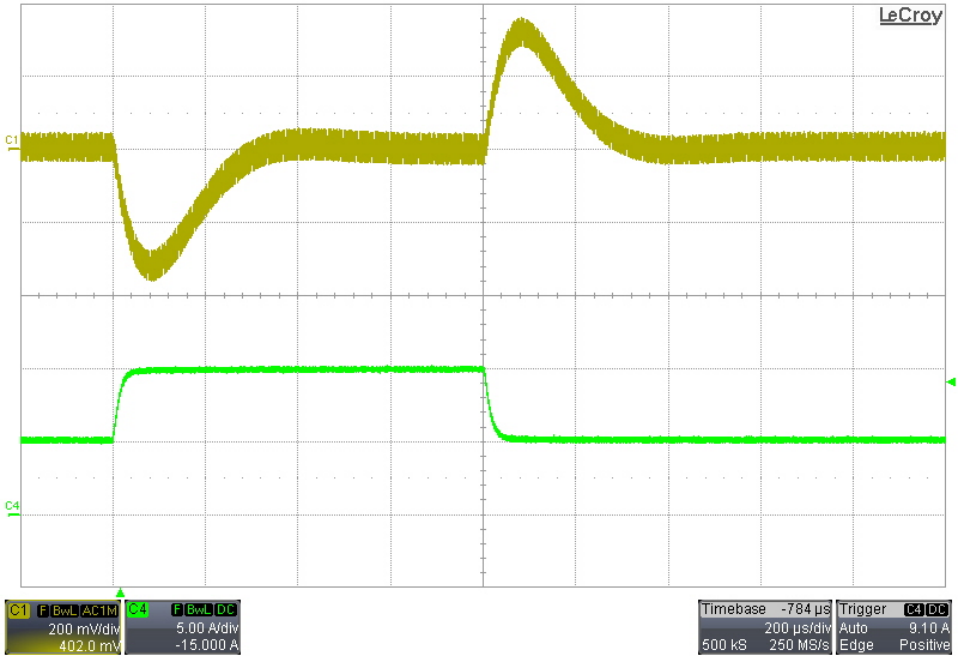
10 Load Transients

The response to a load step from 5A to 10A is shown in the images below. Channel 1: Vout (ac coupled); Channel 4: Iout

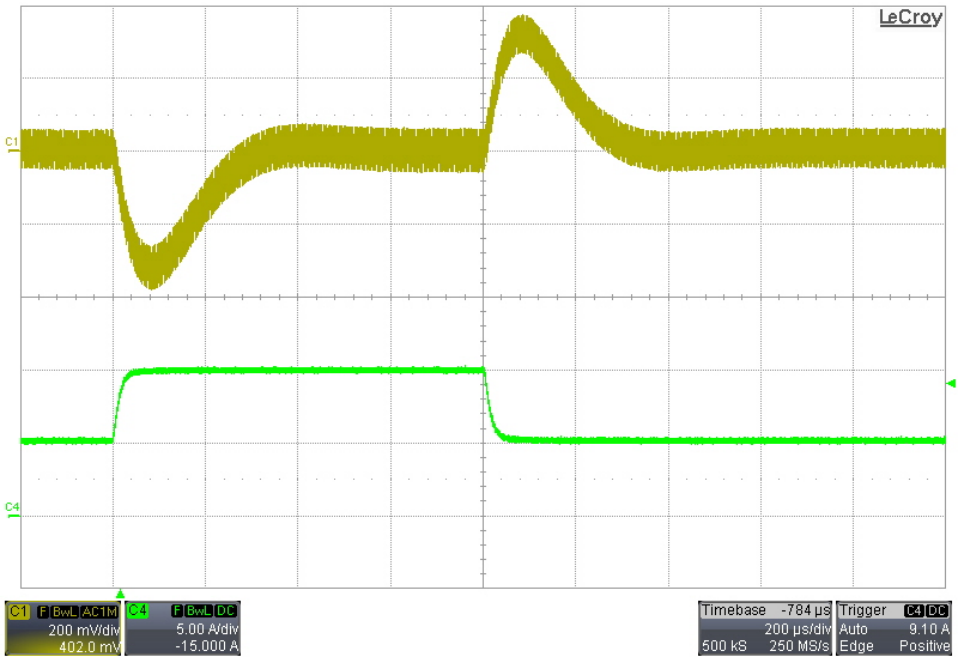
10.1 36V Input



10.2 48V Input



10.3 75V Input



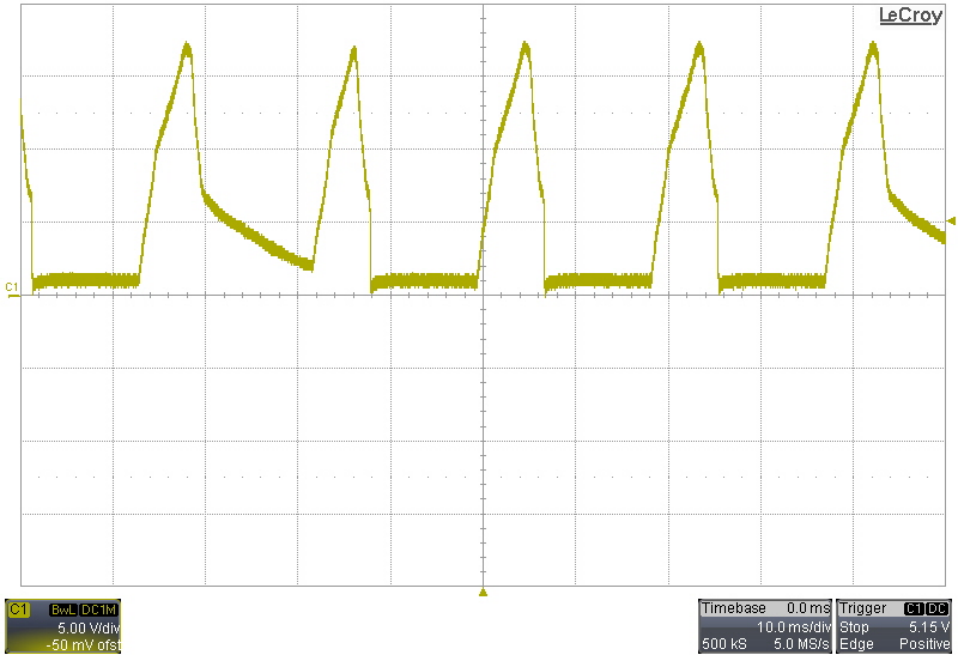
11 Input Under-Voltage Lock-Out

The turn-on and turn-off input voltages were measured and recorded below.

Turn-On	35.3 V
Turn-Off	34.8 V

12 Output Over-Voltage

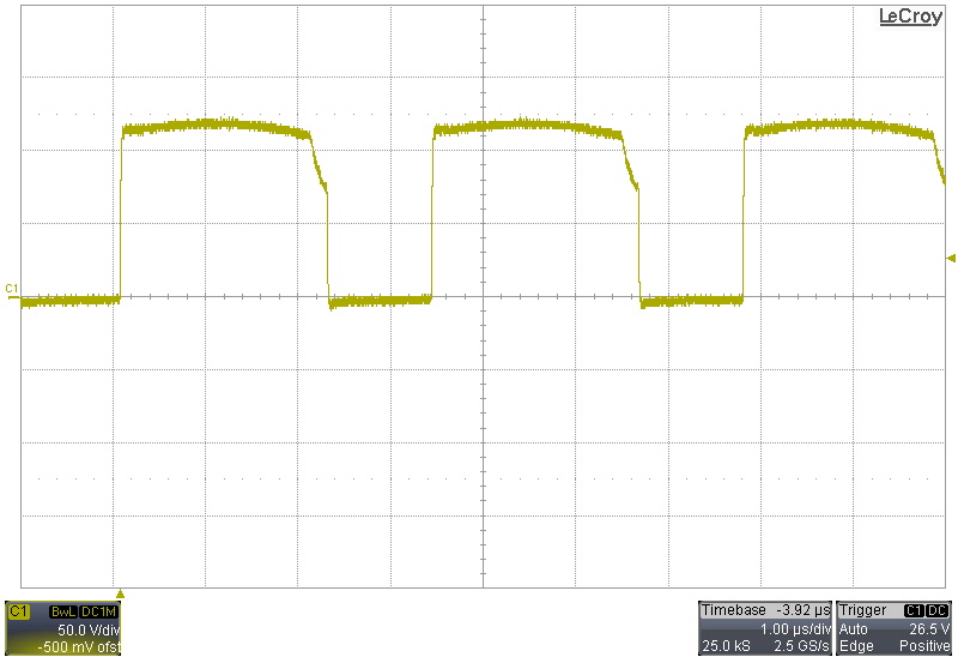
An output over-voltage was induced by shorting the +Remote Sense pin (J5) to ground. The output voltage waveform was captured and is displayed below.



13 Switching Waveforms

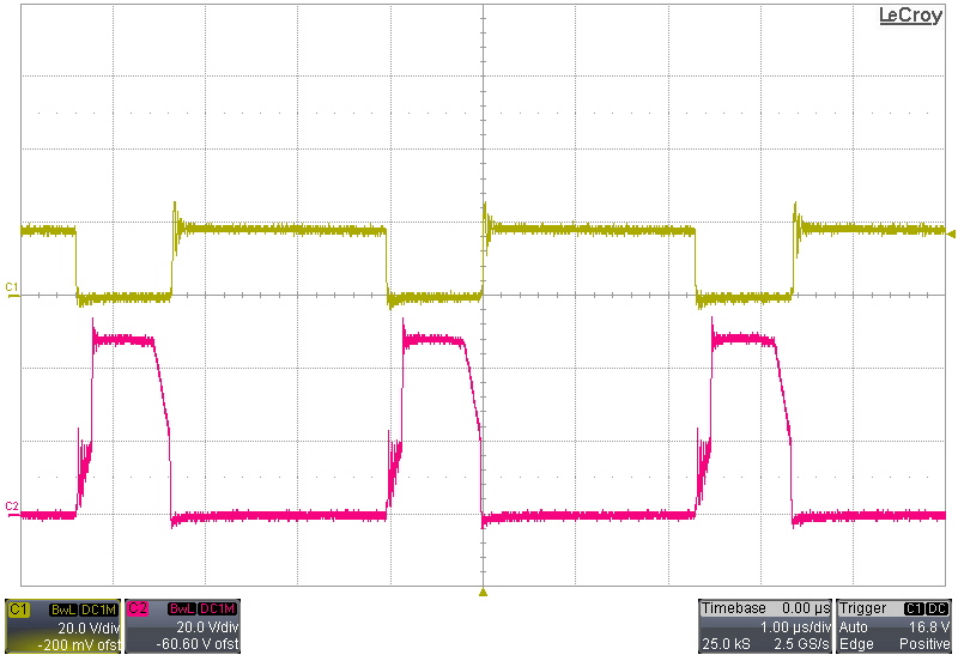
For the images below show the output was loaded with 10A.

13.1 Primary FET (Q2) Vds – 75V Input



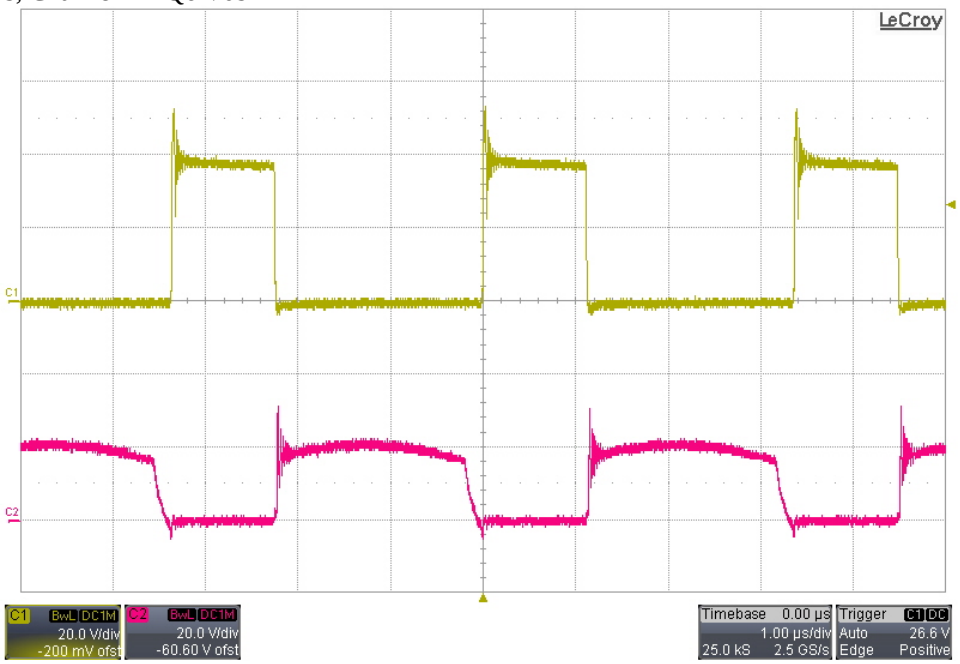
13.2 Q1 & Q6 Synchronous FETs – 36V Input

Channel 1 – Q1 Vds; Channel 2 – Q6 Vds



13.3 Q1 & Q6 Synchronous FETs – 75V Input

Channel 1 – Q1 Vds; Channel 2 – Q6 Vds



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