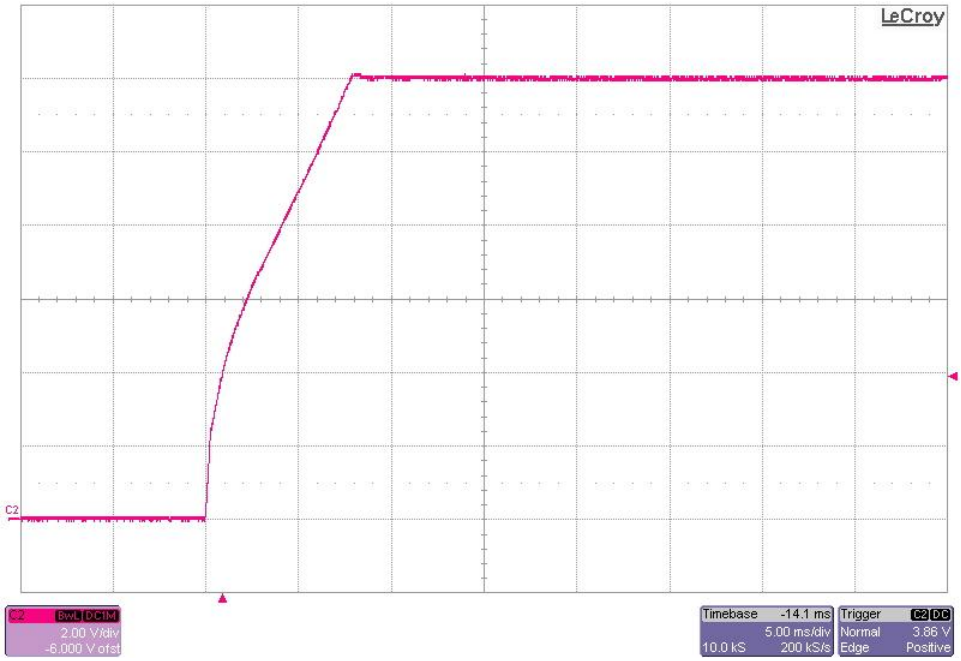
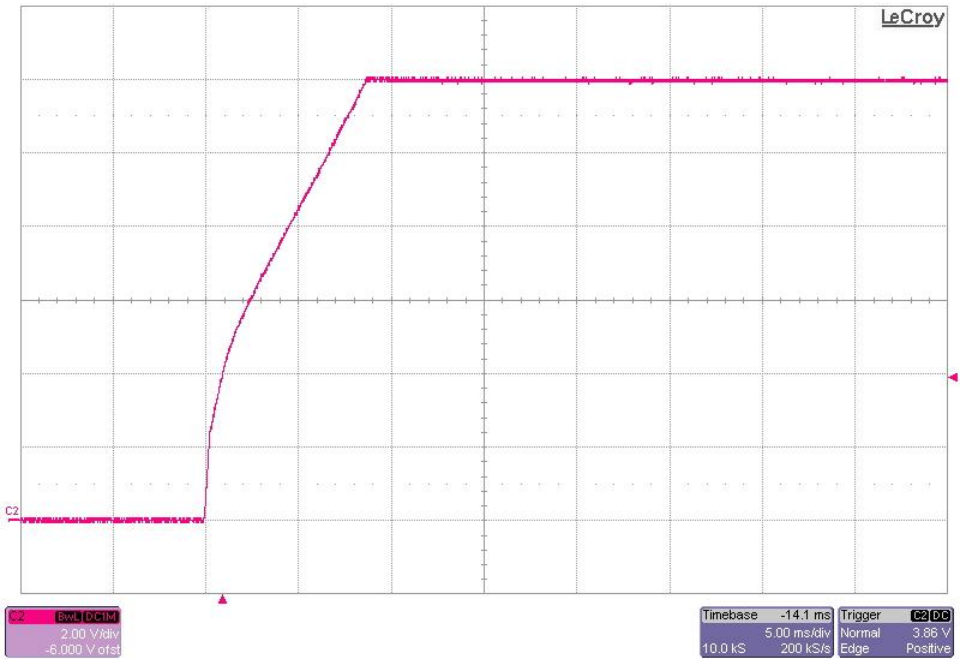
1 Startup

The photo below shows the output voltage startup waveform of a single flyback after the application of 53V in. The 12Voutput wase loaded to 0A. (2V/DIV, 5mS/DIV)

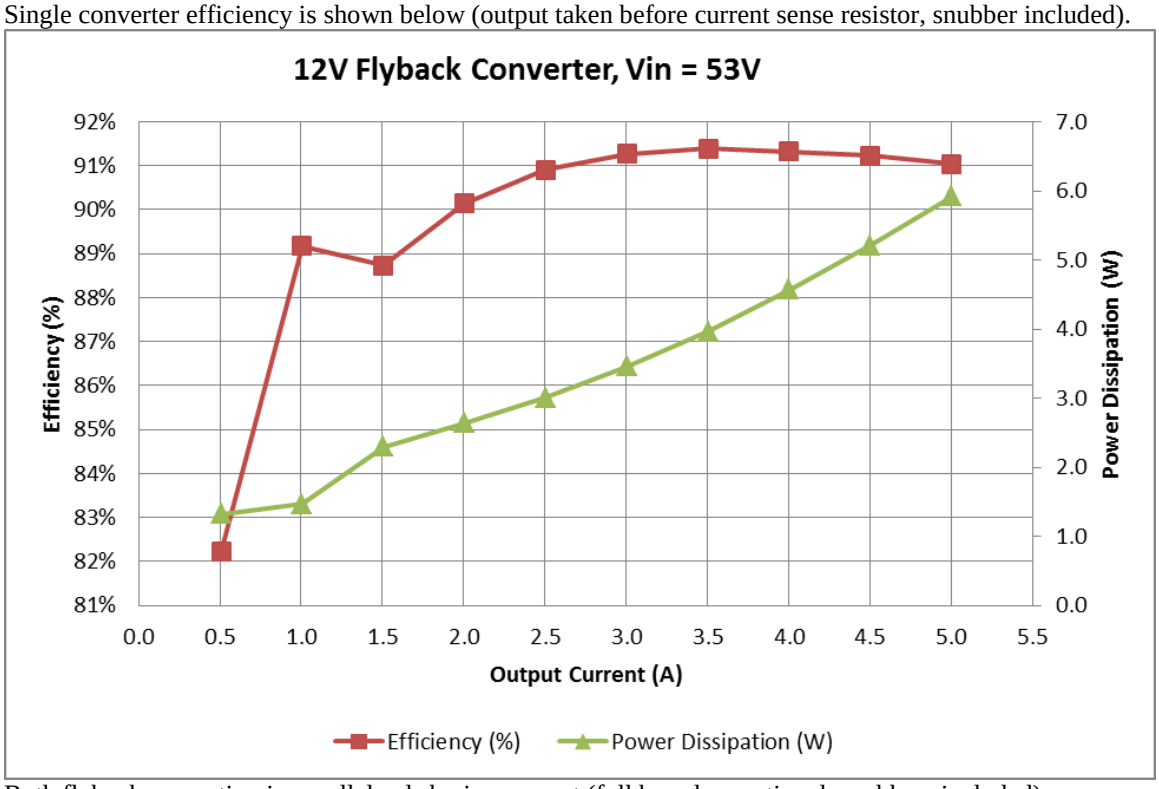


The photo below shows the output voltage startup waveform of a single flyback after the application of 53V in. The 12Voutput wase loaded to 2.5A. (2V/DIV, 5mS/DIV)

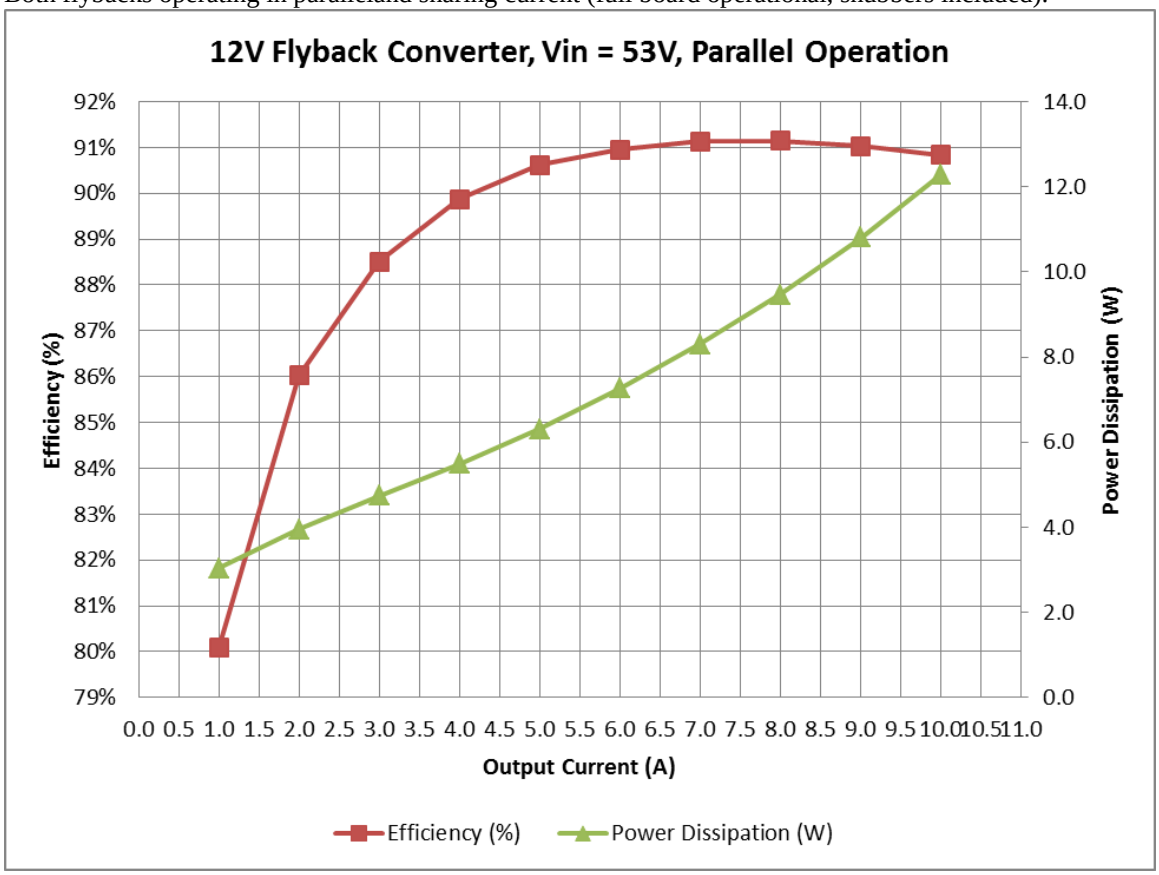


2 Efficiency

Single converter efficiency is shown below (output taken before current sense resistor, snubber included).

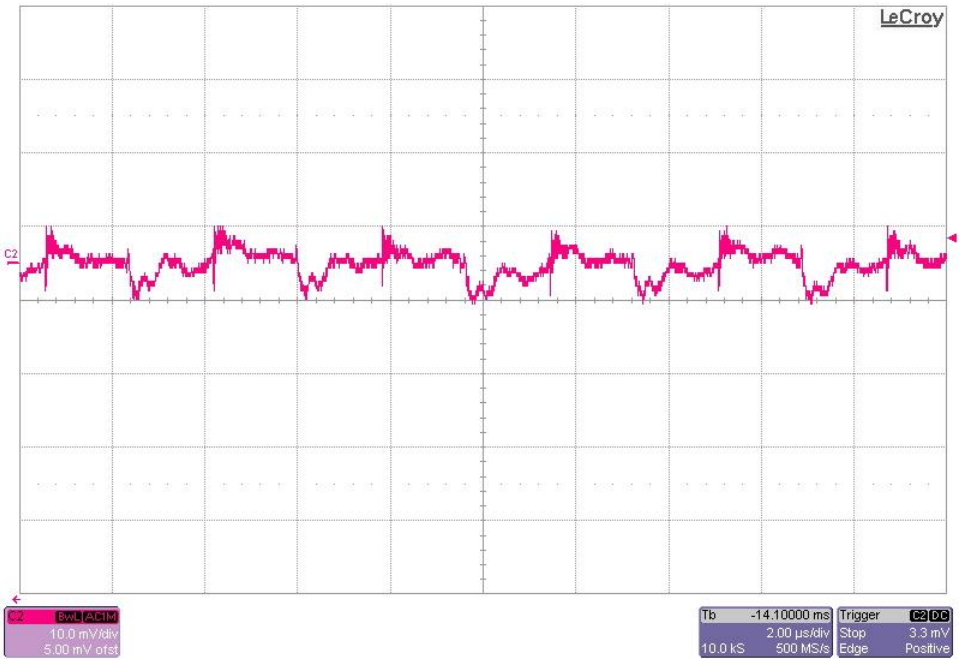


Both flybacks operating in paralleland sharing current (full board operational, snubbers included).

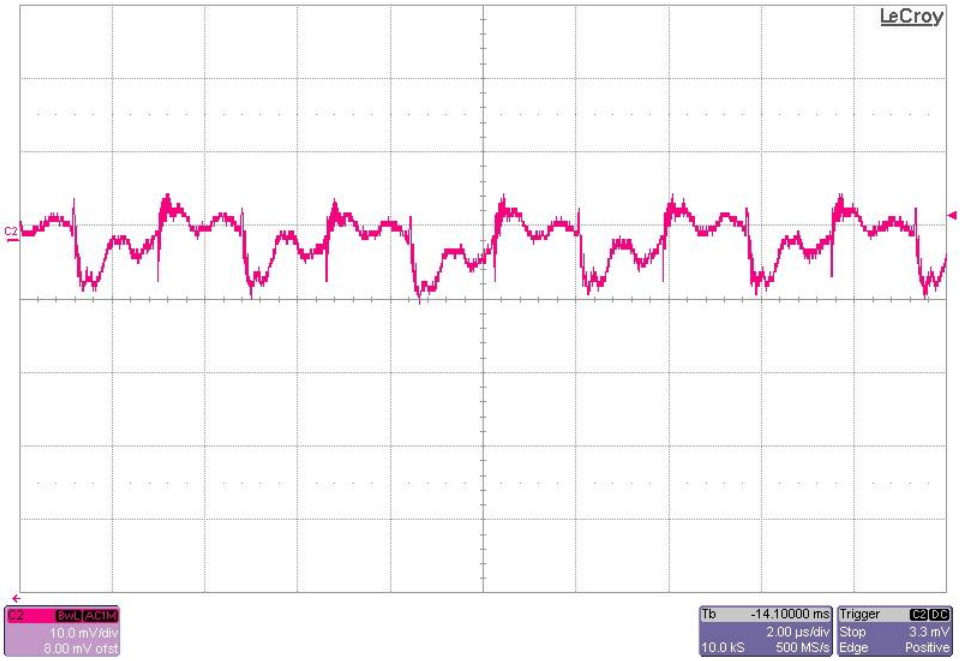


3 Output Ripple Voltage

The 12V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 2.5A. The input voltage is set to 53V. (10mV/DIV, 2uS/DIV)

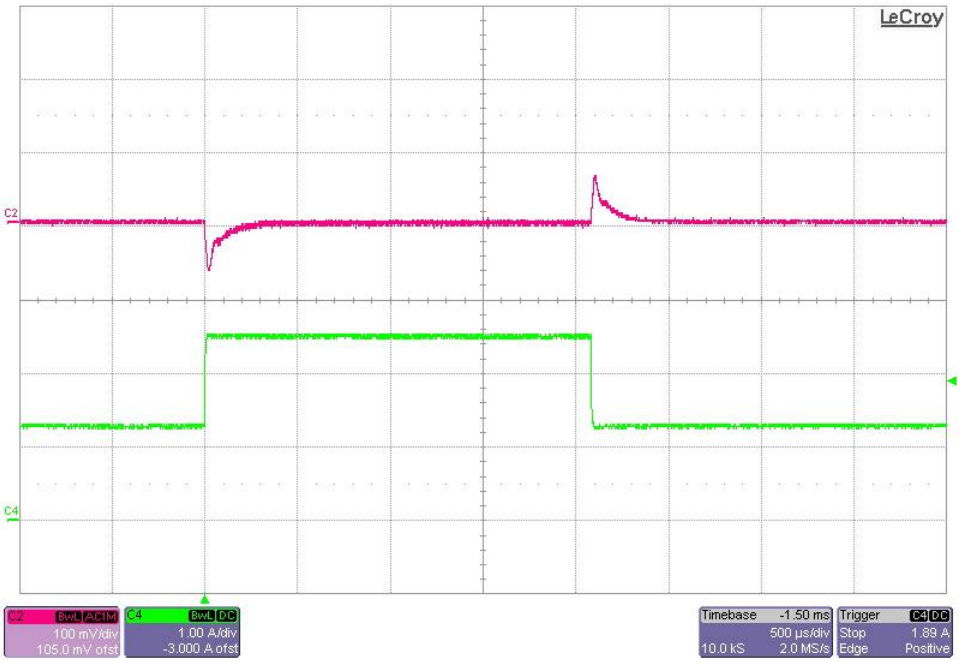


The 12V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 5A. The input voltage is set to 53V. (10mV/DIV, 2uS/DIV)

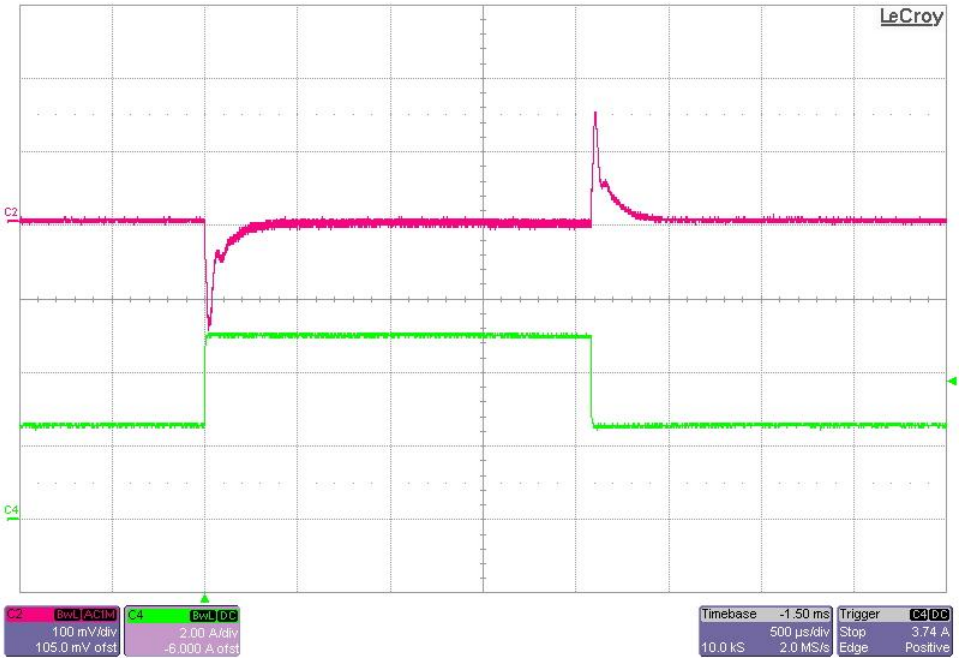


4 Load Transients

The photo below shows the single flyback output voltage (ac coupled) when the load current is stepped between 1.25A and 2.5A. Vin = 53V. (100mV/DIV, 1A/DIV, 500uS/DIV)

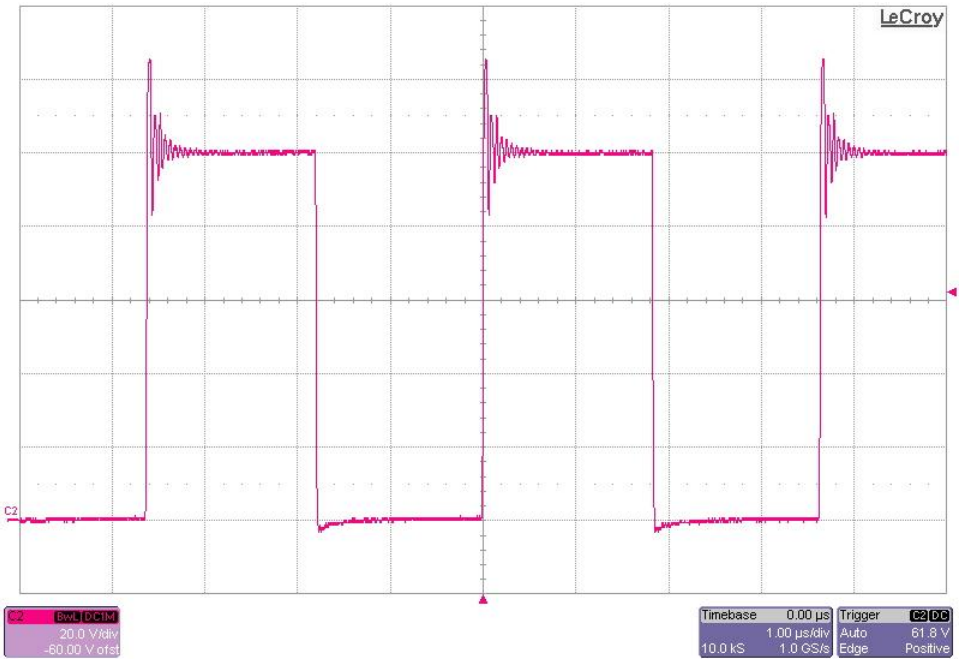


The photo below shows the single flyback output voltage (ac coupled) when the load current is stepped between 2.5A and 5A. Vin = 53V. (100mV/DIV, 2A/DIV, 500uS/DIV)

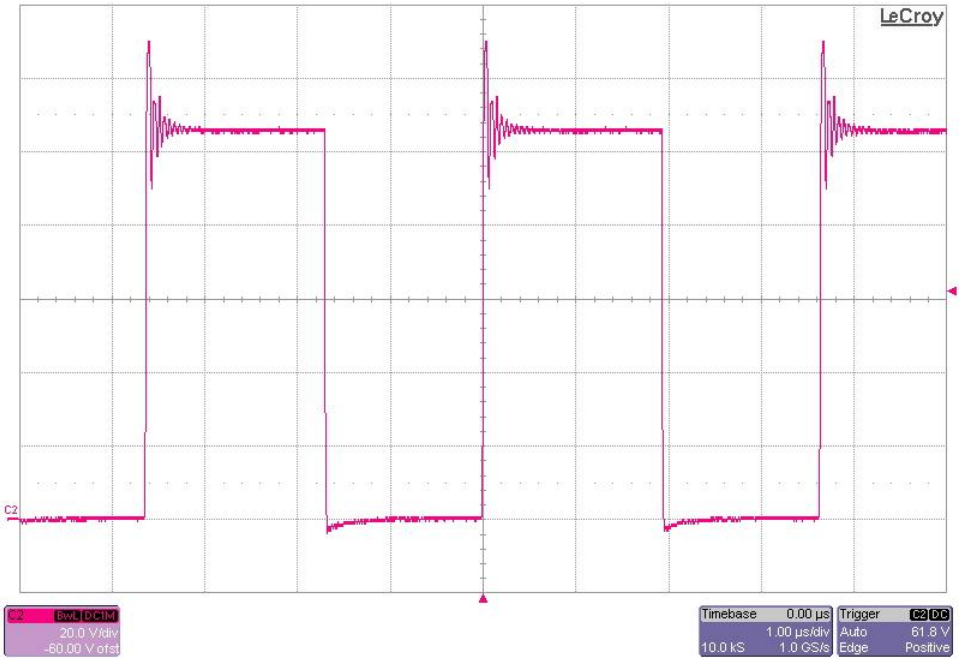


5 Switch Node Waveforms

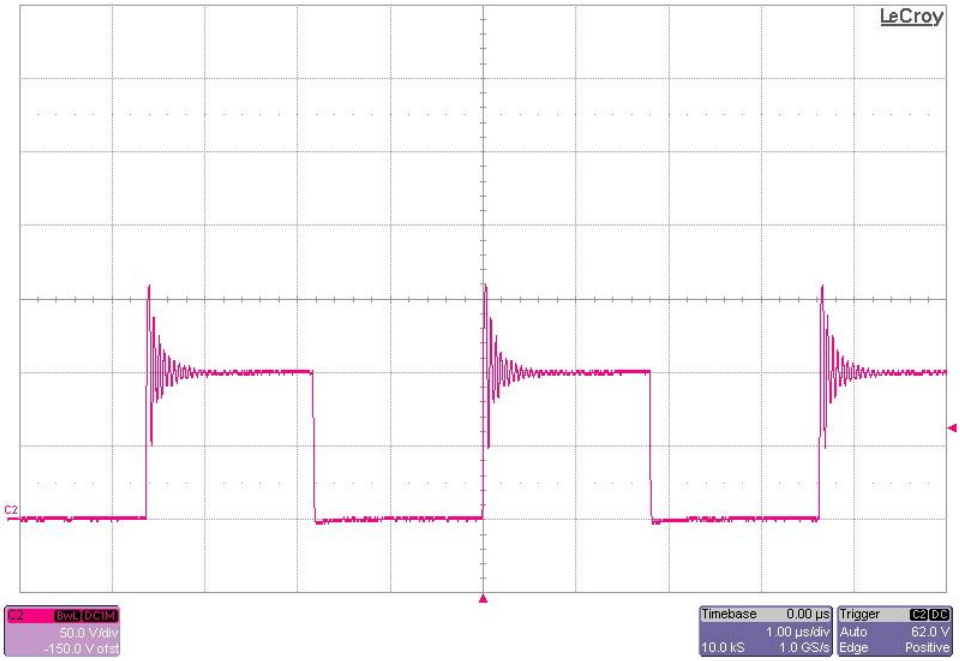
The photo below shows the 12V primary FET switching voltage. The input voltage is 51V and the output is loaded to 2.5A. (20V/DIV, 1uS/DIV)



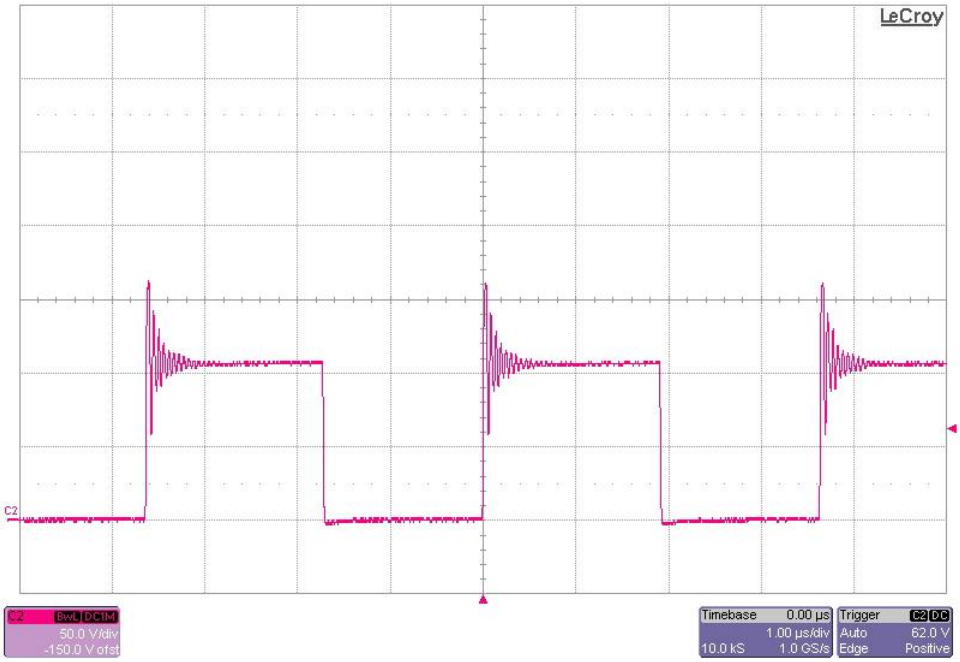
The photo below shows the 12V primary FET switching voltage. The input voltage is 57V and the output is loaded to 2.5A. (20V/DIV, 1uS/DIV)



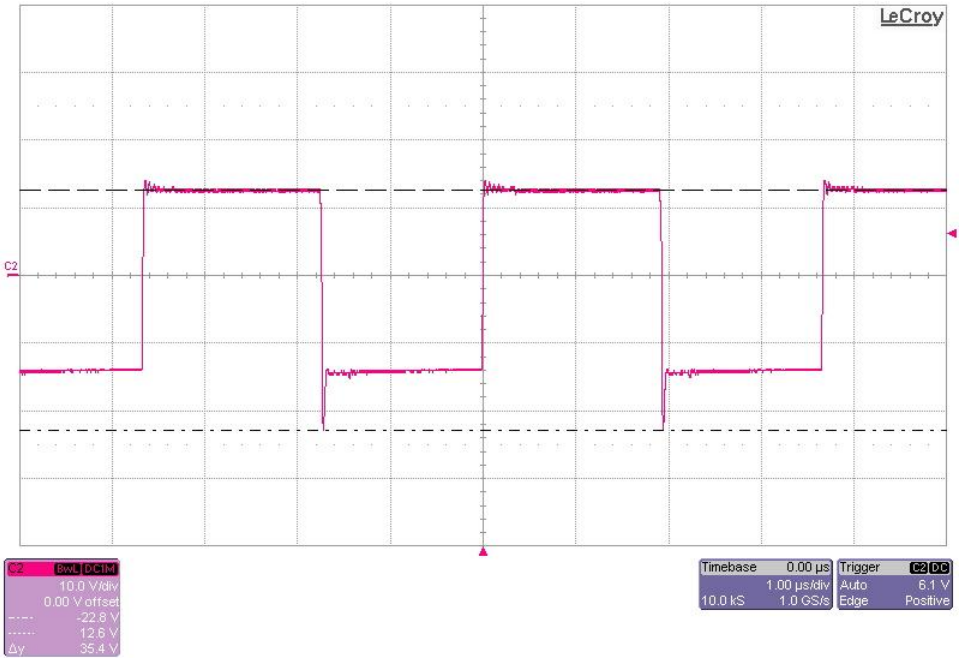
The photo below shows the 12V primary FET switching voltage. The input voltage is 51V and the output is loaded to 5A. (50V/DIV, 1uS/DIV)



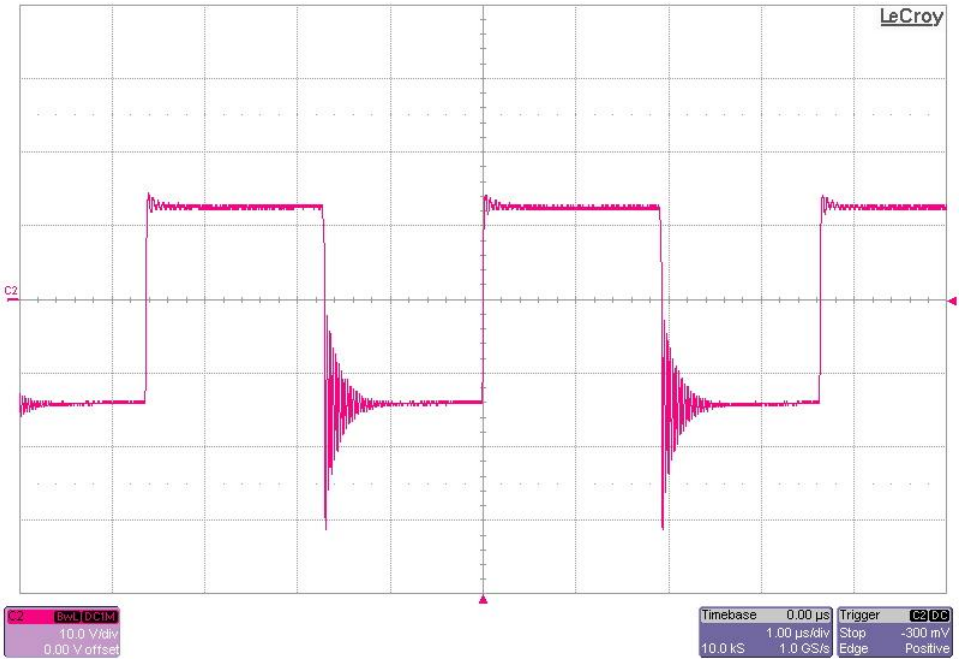
The photo below shows the 12V primary FET switching voltage. The input voltage is 57V and the output is loaded to 5A. (50V/DIV, 1uS/DIV)



The photo below shows the 12V main secondary Rectifier (D1) switching voltage. The input voltage is 57V and the output is loaded to 5A. (10V/DIV, 1uS/DIV)



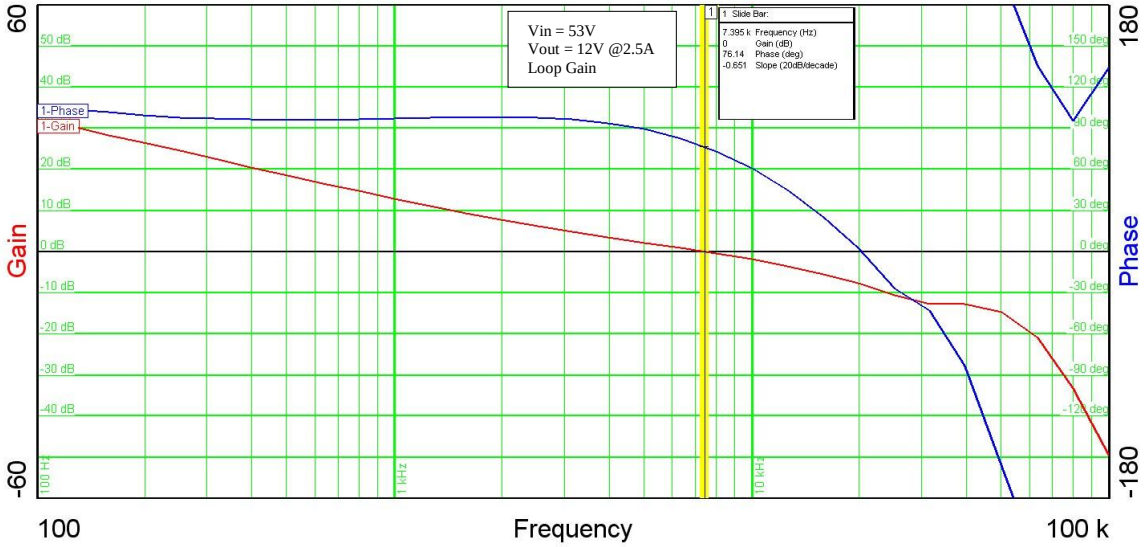
The photo below shows the 12V main secondary Rectifier (D1) switching voltage with the diode snubber **removed** (for reference). The input voltage is 57V and the output is loaded to 5A. (10V/DIV, 1uS/DIV)



6 Control Loop Gain / Stability

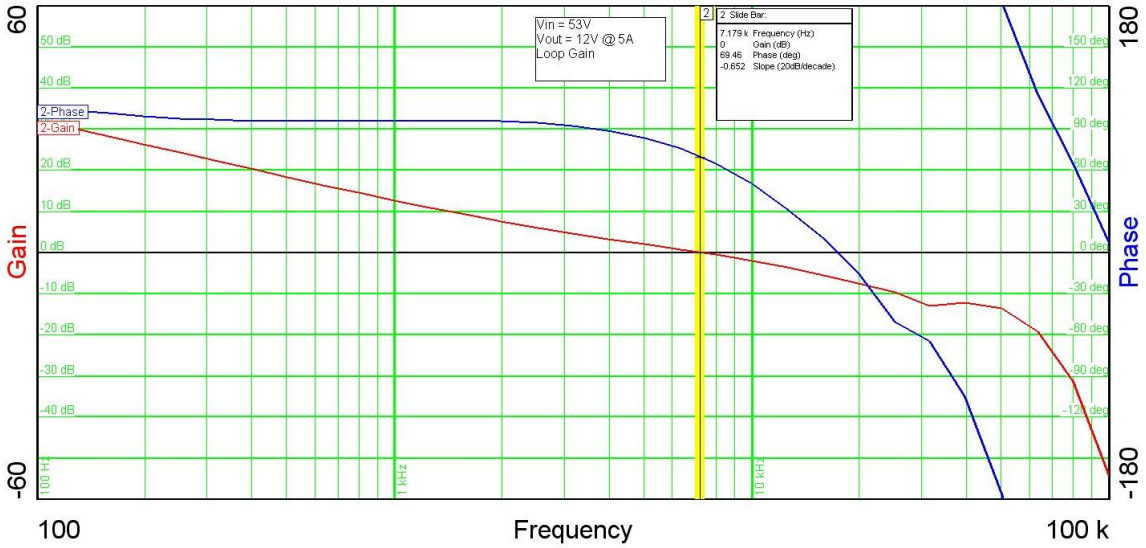
The plot below shows the 12V loop gain and phase margin with the output loaded to 2.5A (without load share controller and C22 = 2200pF, R132 = 0). The input voltage was set to 53V.

Band Width = 7.40KHz, Phase Margin = 76 degrees (12V@2.5A)



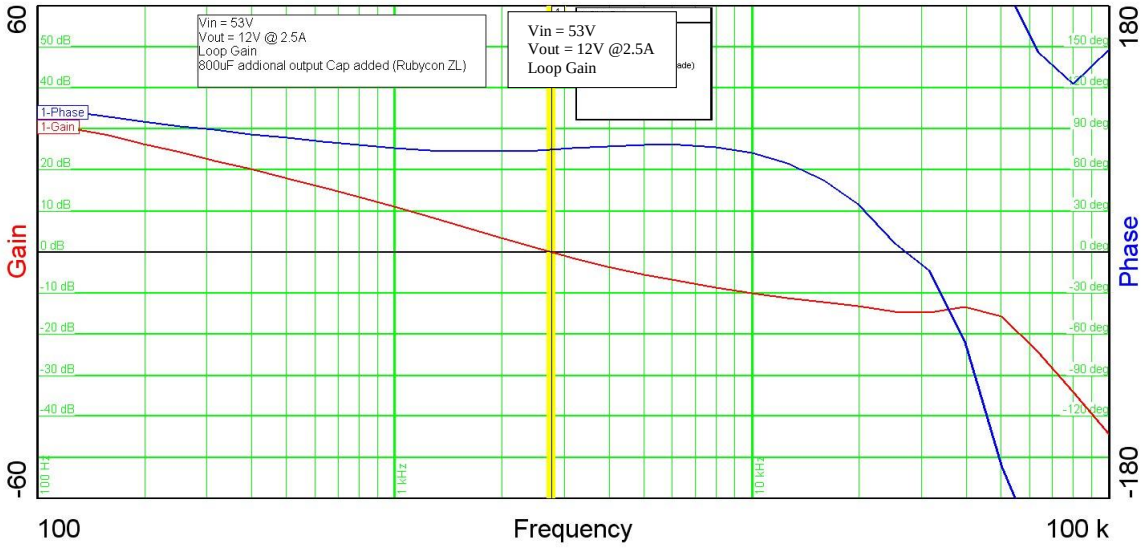
The plot below shows the 12V loop gain and phase margin with the output loaded to 2.5A (without load share controller and C22 = 2200pF, R132 = 0). The input voltage was set to 53V.

Band Width = 7.18KHz, Phase Margin = 69 degrees (12V@5A)



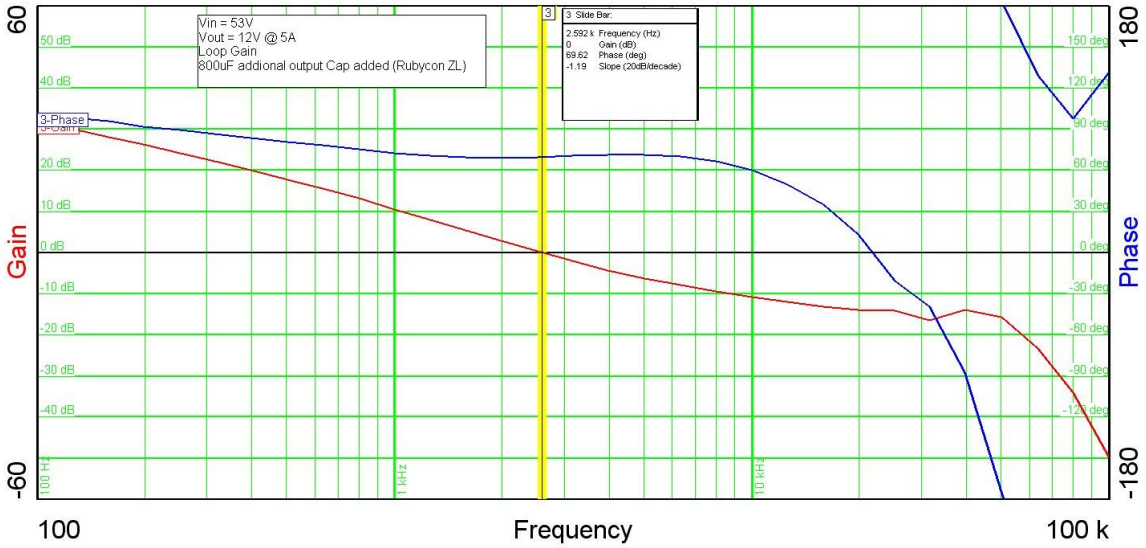
The plot below shows the 12V loop gain and phase margin with the output loaded to 2.5A (without load share controller and C22 = 2200pF, R132 = 0) and 800uF additional output cap added.
The input voltage was set to 53V.

Band Width = 2.76KHz, Phase Margin = 75 degrees (12V@2.5A)



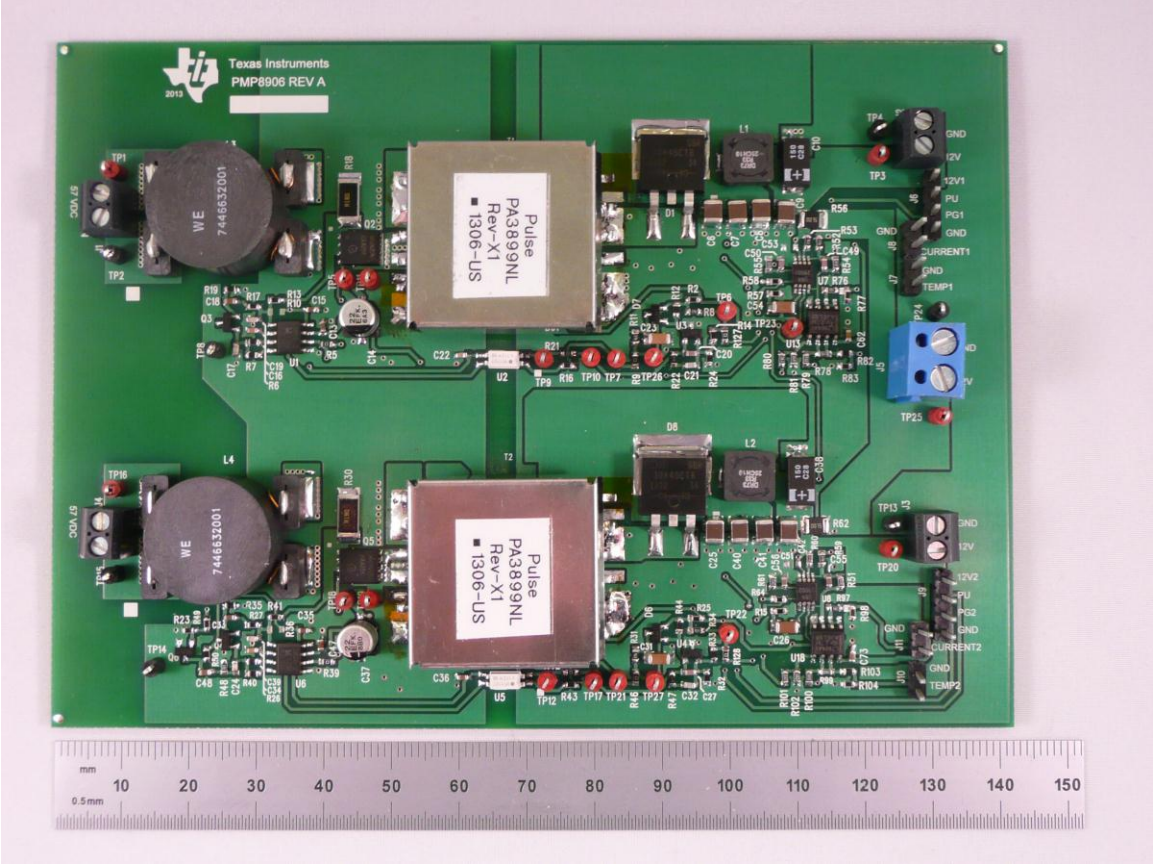
The plot below shows the 12V loop gain and phase margin with the output loaded to 5A (without load share controller and C22 = 2200pF, R132 = 0) and 800uF additional output cap added.
The input voltage was set to 53V.

Band Width = 2.59KHz, Phase Margin = 70 degrees (12V@5A)



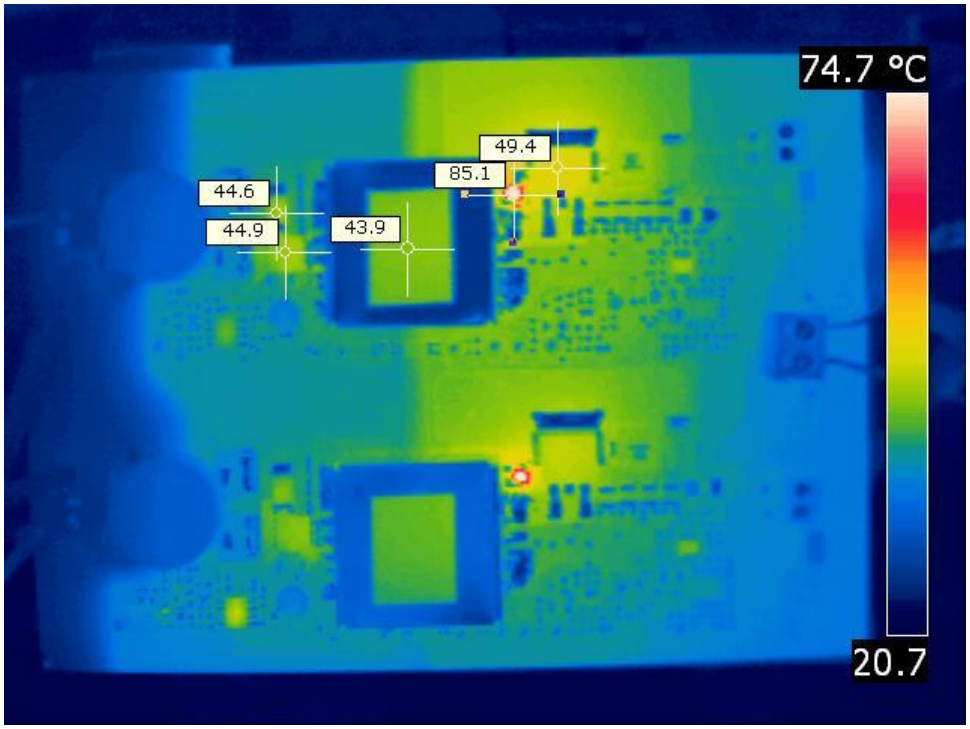
7 Photo

The photo below shows the PMP8906 REVB assy (snubbers not shown).

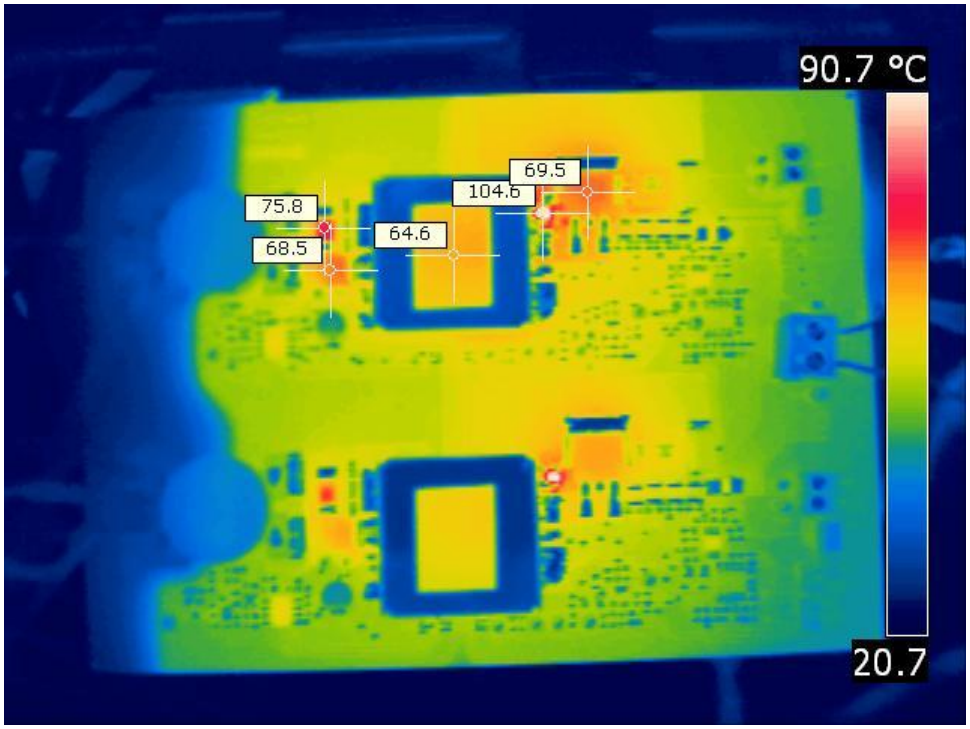


8 Thermal Image

A thermal image is shown below when operating in parallel at 53V input and 5A output (2.5A each flyback), with no airflow.



A thermal image is shown below when operating in parallel at 53V input and 10A output (5A each flyback), with no airflow.



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