

# TPSM8D6C24 Power Module Evaluation Module User's Guide



## ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPSM8D6C24EVM-2V0 evaluation module (EVM). In addition, the user's guide includes test information, descriptions, and results. A complete schematic diagram, printed circuit board layouts, and bill of materials are also included in this document.

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## Trademarks

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## 1 Description

The TPSM8D6C24 is a configurable dual-output buck converter module. The TPSM8D6C24EVM-2V0 uses a nominal 12-V bus to produce a regulated 0.8-V and 1.2-V output at up to 35 A of load current each. The TPSM8D6C24EVM-2V0 demonstrates the dual output capability.

### 1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPSM8D6C24EVM-2V0. Observe all safety precautions.



**Warning**

The TPSM8D6C24EVM-2V0 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.



**Caution**

Do not leave the EVM powered when unattended.

**WARNING**

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces, or sharp edges. Do not reach under the board during operation.

**CAUTION**

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for the system environment.

**CAUTION**

Some power supplies can be damaged by application of external voltages. If using more than one power supply, check the equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to the equipment.

**CAUTION**

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the battery-potential of the EVM.

### 1.2 Features

- Regulated 0.8-V and 1.2-V output up to 35-A<sub>DC</sub> output current each
- Convenient test points for probing critical waveforms
- PMBus® connector for easy connection with the TI USB adapter

## 2 Electrical Performance Specifications

Table 2-1 lists the electrical performance specifications in room temperature (20 to 25°C). Characteristics are given for an input voltage of  $V_{IN} = 12\text{ V}$ , unless otherwise specified.

**Table 2-1. TPSM8D6C24EVM-2V0 Electrical Performance Specifications**

Parameter	Test Conditions	MIN	TYP	MAX	Unit
<b>Input Characteristics</b>					
Input voltage range, $V_{IN}$		5	12	16	V
Full load input current	$I_{OUTA} = I_{OUTB} = 35\text{ A}$		7		A
	$V_{IN} = 5\text{ V}$ , $I_{OUTA} = I_{OUTB} = 35\text{ A}$		16.8		A
No load input current	$I_{OUTA} = I_{OUTB} = 0\text{ A}$ , switching enabled		136		mA
Enable switching threshold	Set by default resistor divider, JP3 and JP4 in UVLO position		3.92		V
Disable switching threshold	Set by default resistor divider, JP3 and JP4 in UVLO position		3.50		V
<b>Output Characteristics</b>					
VOUT_A output voltage, $V_{OUTA}$			0.8		V
VOUT_B output voltage, $V_{OUTB}$			1.2		V
VOUT_A output load current, $I_{OUTA}$		0		35	A
VOUT_B output load current, $I_{OUTB}$		0		35	A
VOUT_A output voltage regulation	Line Regulation: $V_{IN} = 5\text{ V to }16\text{ V}$		0.1		%
	Load Regulation: $I_{OUTA} = 0\text{ A to }35\text{ A}$		0.1		%
VOUT_B output voltage regulation	Line Regulation: $V_{IN} = 5\text{ V to }16\text{ V}$		0.1		%
	Load Regulation: $I_{OUTB} = 0\text{ A to }35\text{ A}$		0.1		%
VOUT_A output overcurrent fault threshold	Programmed by MSEL2		52		A
VOUT_B output overcurrent fault threshold	Programmed by MSEL2		52		A
<b>Systems Characteristics</b>					
Switching frequency	Programmed by MSEL1		550		kHz
Operating case temperature	$I_{OUTA} = I_{OUTB} = 35\text{ A}$ , Airflow = 200 LFM, 10 minute soak		100		°C

### 3 Schematic

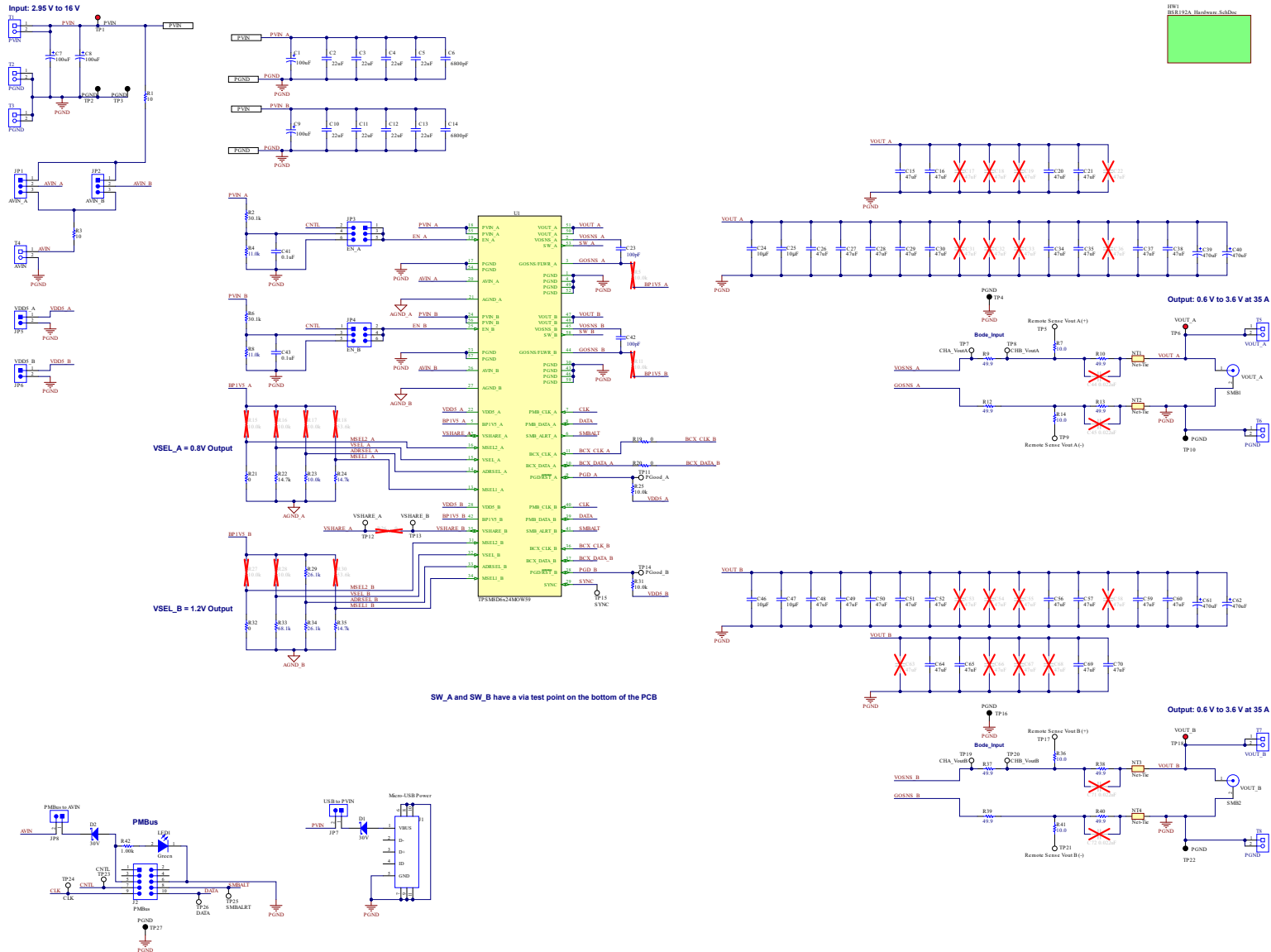


Figure 3-1. TPSM8D6C24EVM-2V0 Schematic

## 4 Test Setup

### 4.1 Test and Configuration Software

To change any of the default configuration parameters on the EVM through PMBus, obtain the *TI Fusion Digital Power Designer* software.

#### 4.1.1 Description

The *TI Fusion Digital Power Designer* is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPSM8D6C24 power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter described in [Section 4.2.6](#).

#### 4.1.2 Features

Some of the tasks the user can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data. Items such as input voltage, output voltage, output current, die temperature, and warnings and faults that are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as the following:
  - $V_{OUT}$  trim and margin
  - UVLO
  - Soft-start time
  - Warning and fault thresholds
  - Fault response
  - On/off modes

This software is available for download at [http://www.ti.com/tool/fusion\\_digital\\_power\\_designer](http://www.ti.com/tool/fusion_digital_power_designer).

### 4.2 Test Equipment

#### 4.2.1 Voltage Source

The input voltage source  $V_{IN}$  must be a 0-V to 18-V variable DC source capable of supplying a minimum of 8  $A_{DC}$  to support 35-A load with 5-V input (or 16  $A_{DC}$  to support a combined 70-A load). Connect input VIN and GND to T1 (PVIN) and T2/T3 (PGND). If the output voltage of the EVM is increased, the power supply may need to supply more current.

#### 4.2.2 Oscilloscope

An oscilloscope is recommended for measuring output noise and ripple. Output ripple must be measured using a tip-and-barrel method.

#### 4.2.3 Multimeters

TI recommends using two separate multimeters: one meter to measure  $V_{IN}$  and the other to measure  $V_{OUT}$ .

#### 4.2.4 Output Load

A variable electronic load is recommended for the test setup. To test the full load current this EVM supports, the load should be capable of sinking at least 35 A.

#### 4.2.5 Fan

During prolonged operation at high loads, it can be necessary to provide forced air cooling with a small fan aimed at the EVM. Maintain the surface temperature of the devices on the EVM below their rated temperature.

#### 4.2.6 USB-to-GPIO Interface Adapter

A communications adapter is required between the EVM and the host computer. This EVM is designed to use TI's USB-to-GPIO adapter. Purchase this adapter at <http://www.ti.com/tool/usb-to-gpio>.

### 4.2.7 Recommended Wire Gauge

- Input connection to the VIN and PGND terminal blocks (T1, T2, and T3) – The recommended wire size is AWG #12, with the total length of wire less than two feet (1-foot input, 1-foot return).
- Output load connection to the VOUT\_A, VOUT\_B, and PGND terminal blocks (T5, T6, T7, and T8) – The minimum recommended wire size is AWG #10, with the total length of wire less than two feet (1-foot output, 1-foot return). A thicker wire gauge can be required to minimize the voltage drop in the wires.

### 4.3 List of Test Points, Jumpers, and Connectors

Table 4-1 lists the test point functions.

**Table 4-1. Test Point Functions**

Test Point	Name	Description
TP1	PVIN	PVIN test point
TP2, TP3, TP4, TP10, TP16, TP22, TP27	PGND	PGND test point
TP5	Remote Sense Vout A (+)	VOUT_A remote sense + voltage point
TP6	VOUT_A	VOUT_A sensing test point
TP7	CHA_VoutA	Channel A for VOUT_A small signal loop gain measurements (B/A setup)
TP8	CHB_VoutA	Channel B for VOUT_A small signal loop gain measurements (B/A setup)
TP9	Remote Sense Vout A (-)	VOUT_A remote sense - voltage point
TP11	PGood_A	PGOOD signal of VOUT_A
TP12	VSHARE_A	VSHARE_A measurement point. Sensitive signal
TP13	VSHARE_B	VSHARE_B measurement point. Sensitive signal
TP14	PGood_B	PGOOD signal of VOUT_B
TP15	SYNC	External clock input (SYNC IN) or output to synchronize other devices (SYNC OUT)
TP17	Remote Sense Vout B (+)	VOUT_B remote sense + voltage point
TP18	VOUT_B	VOUT_B sensing test point
TP19	CHA_VoutB	Channel A for VOUT_B small signal loop gain measurements (B/A setup)
TP20	CHB_VoutB	Channel B for VOUT_B small signal loop gain measurements (B/A setup)
TP21	Remote Sense Vout B (-)	VOUT_B remote sense - voltage point
TP23	CNTL	CNTL signal on J2 header
TP24	CLK	CLK signal on J2 header
TP25	SMBALRT	SMBALERT signal on J2 header
TP26	DATA	DATA signal on J2 header

Table 4-2 lists the EVM jumpers.

**Table 4-2. Jumpers**

Jumper	Name	Description
JP1	AVIN_A	AVIN_A input source selection
JP2	AVIN_B	AVIN_B input source selection
JP3	EN_A	EN_A pin selections
JP4	EN_B	EN_B pin selections
JP5	VDD5_A	External VDD5_A connection
JP6	VDD5_B	External VDD5_B connection
JP7	USB to PVIN	Short to connect PVIN to micro USB connector
JP8	PMBus to AVIN	Short to connect USB-to-GPIO 3.3V to AVIN

Table 4-3 lists the options for the EN/UVLO pin selections on JP2 and JP4.

**Table 4-3. JP3 and JP4 Selections**

Shunt Position	Selection
CNTL_INPUT	PMBus adapter control signal
UVLO	Resistor divider to PVIN
DISABLE	EN/UVLO short to ground

Table 4-4 lists the options for the AVIN pin selections on JP1 and JP2.

**Table 4-4. JP1 and J2 Selections**

Shunt Position	Selection
AVIN	AVIN pin connected to AVIN input through 10- $\Omega$ resistor. Use this selection when testing with a split rail input.
PVIN	AVIN pin connected to PVIN through 10- $\Omega$ resistor

Table 4-5 lists the EVM connector functions.

**Table 4-5. Connector Functions**

Connector	Name	Description
J1	Micro-USB Power	Micro USB connector to power EVM from a 5-V USB source
J2	PMBus	PMBus socket for TI FUSION adapter
T1	PVIN	VIN+ connector
T2, T3	PGND	VIN- connector
T4	AVIN	External AVIN connector
T5	VOUT_A	VOUT+ connector
T6, T8	PGND	VOUT- connector

#### 4.4 Evaluating Split Rail Input

The default configuration of the EVM is for single rail input. Split rail input enables operation with 3.3-V PVIN. For split rail operation, configure the jumpers on the EVM as follows:

1. Move the jumper JP1 and JP2 to AVIN position to disconnect the AVIN pin from the PVIN pins.
2. Apply the AVIN input to T4. 4-V or greater AVIN is required to bring the VDD5 voltage high enough to enable conversion.
3. If operation with 3.3-V PVIN is needed and the CNTL jumpers (JP3 and JP4) are in UVLO position, the resistor divider at the EN/UVLO will need to be changed. Alternately, move the CNTL jumpers to CNTL\_INPUT position and use the control signal to enable conversion or use the ON\_OFF\_CONFIG and OPERATION commands to enable conversion.



## 5 EVM Configuration Using the Fusion GUI

The TPSM8D6C24 leaves the factory pre-configured. The factory default settings for the parameters can be found in the data sheet. If configuring the EVM to settings other than the factory defaults, use the software described in [Section 4.1](#). It is necessary to have the input voltage applied to the EVM prior to launching the software so that the TPSM8D6C24 can respond to the GUI and the GUI can recognize the device. The default configuration for the EVM to stop converting is set by the EN/UVLO resistor divider to a nominal input voltage of 3.5 V, therefore, if it is necessary to avoid any converter activity during configuration, an input voltage less than 3.5 V should be applied. TI recommends an input voltage of 3.3 V.

### 5.1 Configuration Procedure

1. Adjust the input supply to provide 3.3 VDC, current limited to 1 A.
2. Apply the input voltage to the EVM. See [Section 4.2](#) for connections and test setup.
3. Launch the Fusion GUI software. See the screen shots in [Section 10](#) for more information.
4. Configure the EVM operating parameters as desired.

## 6 Test Procedure

### 6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as [Section 4.2](#) and [Section 6.2](#) describe.
2. Set the electronic load to draw 0 A<sub>DC</sub>.
3. Increase V<sub>IN</sub> from 0 V to 12 V using a voltage meter to measure input voltage.
4. Use the other voltage meter to measure output voltage, V<sub>OUT</sub>.
5. Vary the load from 0 to 35 A<sub>DC</sub>. V<sub>OUT</sub> should remain in regulation as defined in [Table 2-1](#).
6. Vary V<sub>IN</sub> from 5 V to 16 V. V<sub>OUT</sub> should remain in regulation as defined in [Table 2-1](#).
7. Decrease the load to 0 A.
8. Decrease V<sub>IN</sub> to 0 V.

### 6.2 Efficiency Measurement Test Points

To evaluate the efficiency of the power train (device and inductor), it is important to measure the voltages at the correct location. This is necessary because otherwise the measurements will include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which should not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

[Table 6-1](#) shows the measurement points for input voltage and output voltage. V<sub>IN</sub> and V<sub>OUT</sub> are measured to calculate the efficiency. Using these measurement points will result in efficiency measurements that excluded losses due to the wires and connectors.

**Table 6-1. Test Points for Efficiency Measurements**

Test Point	Node Name	Description	Comment
<b>VOUT_A</b>			
TP1	PVIN	Input voltage measurement point for VIN+	The pair of test points are connected to the PVIN/PGND pins of U1. The voltage drop between input terminal to the device pins is included for efficiency measurement.
TP3	PGND	Input voltage measurement point for VIN- (GND)	
TP6	VOUT_A	Output voltage measurement point for VOUT+	The pair of test points are connected near the output terminals. The voltage drop from the output point of the inductor to the output terminals is included for efficiency measurement.
TP10	PGND	Output voltage measurement point for VOUT- (GND)	
<b>VOUT_B</b>			
TP1	PVIN	Input voltage measurement point for VIN+	The pair of test points are connected to the PVIN/PGND pins of U1. The voltage drop between input terminal to the device pins is included for efficiency measurement.
TP2	PGND	Input voltage measurement point for VIN- (GND)	

**Table 6-1. Test Points for Efficiency Measurements (continued)**

Test Point	Node Name	Description	Comment
TP18	VOUT_B	Output voltage measurement point for VOUT+	The pair of test points are connected near the output terminals. The voltage drop from the output point of the inductor to the output terminals is included for efficiency measurement.
TP22	PGND	Output voltage measurement point for VOUT- (GND)	

### 6.3 Control Loop Gain and Phase Measurement Procedure

The TPSM8D6C24EVM-2V0 includes a 49.9-Ω series resistor in the feedback loop for V<sub>OUT</sub>. The resistor is accessible at the test points TP7, TP8, TP19, and TP20 for loop response analysis. These test points should be used during loop response measurements as the perturbation injecting points for the loop. See the description in [Table 6-2](#).

**Table 6-2. List of Test Points for Loop Response Measurements**

Test Point	Node Name	Description	Comment
<b>VOUT_A</b>			
TP7	CHA_VoutA	Input to feedback divider of VOUT_A	The amplitude of the perturbation at this node should be limited to less than 30 mV.
TP8	CHB_VoutA	Resulting output of VOUT_A	Bode can be measured by a network analyzer with a CH_B/CH_A configuration.
<b>VOUT_B</b>			
TP19	CHA_VoutB	Input to feedback divider of VOUT_B	The amplitude of the perturbation at this node should be limited to less than 30 mV.
TP20	CHB_VoutB	Resulting output of VOUT_B	Bode can be measured by a network analyzer with a CH_B/CH_A configuration.

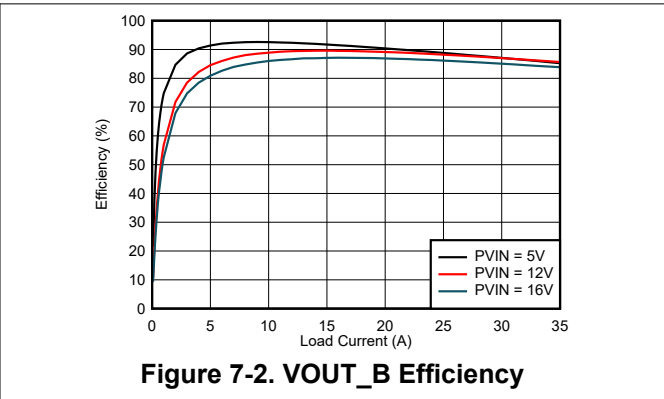
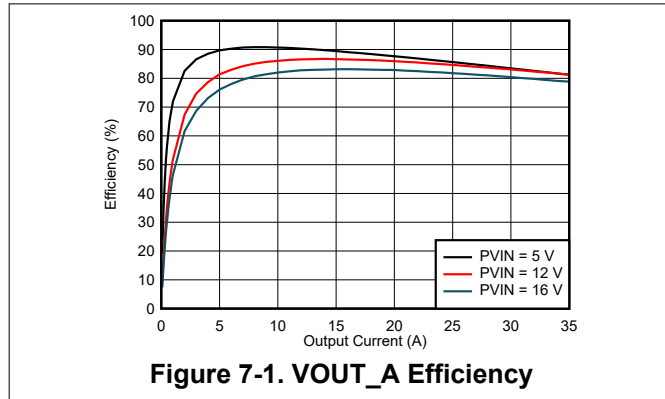
Measure the loop response with the following procedure:

1. Set up the EVM as described in [Section 4.2](#).
2. For VOUT\_A, connect the isolation transformer of the network analyzer from TP7 to TP8.
3. Connect the input signal measurement probe to TP7. Connect the output signal measurement probe to TP8.
4. Connect the ground leads of both probe channels to TP3.
5. On the network analyzer, measure the Bode as TP8/TP7 (Out/In).
6. For VOUT\_B, connect the isolation transformer of the network analyzer from TP19 to TP20.
7. Connect the input signal measurement probe to TP19. Connect the output signal measurement probe to TP20.
8. Connect the ground leads of both probe channels to TP2.
9. On the network analyzer, measure the Bode as TP20/TP19 (Out/In).

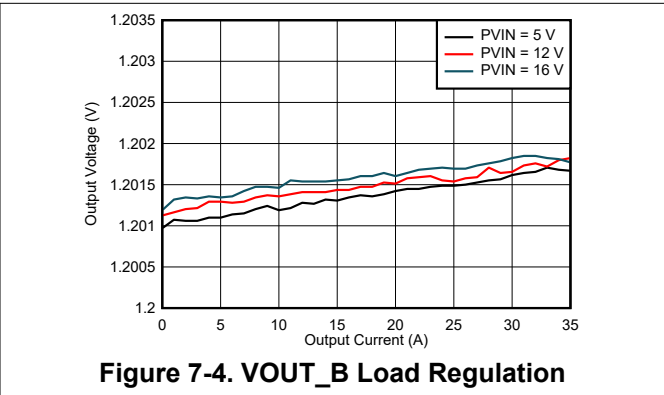
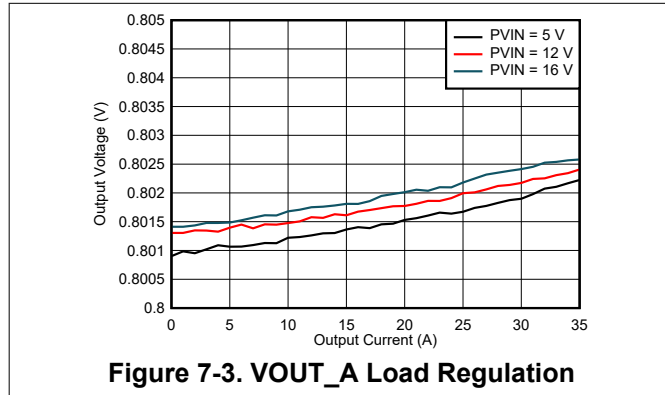
## 7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-19 present typical performance curves for the TPSM8D6C24EVM-2V0. The input voltage is 12 V and the oscilloscope measurements use 20-MHz bandwidth limiting, unless otherwise noted.

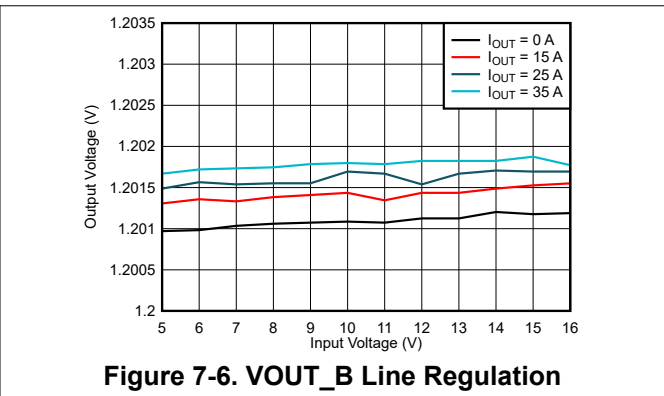
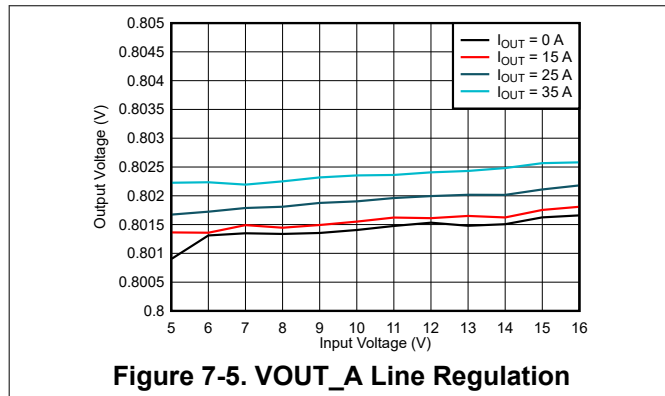
### 7.1 Efficiency



### 7.2 Load Regulation

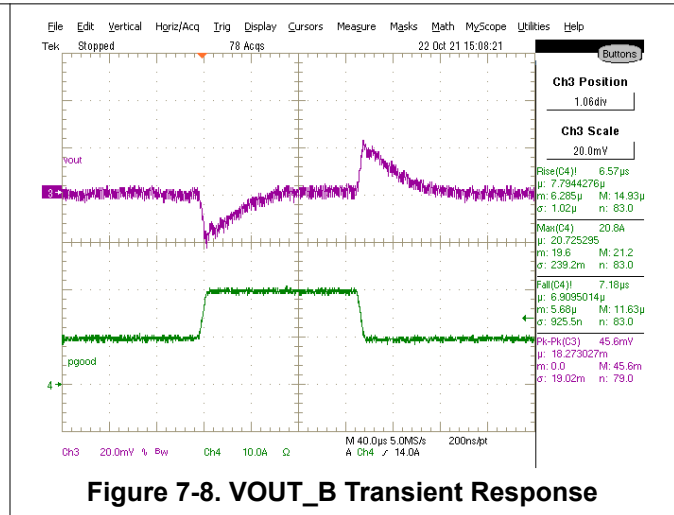
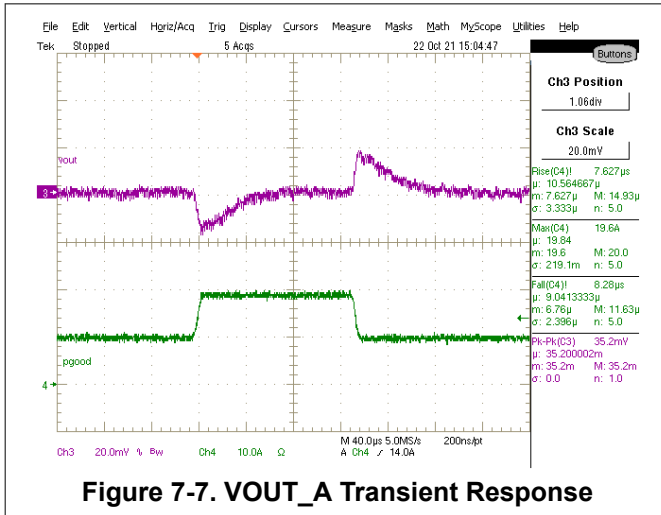


### 7.3 Line Regulation

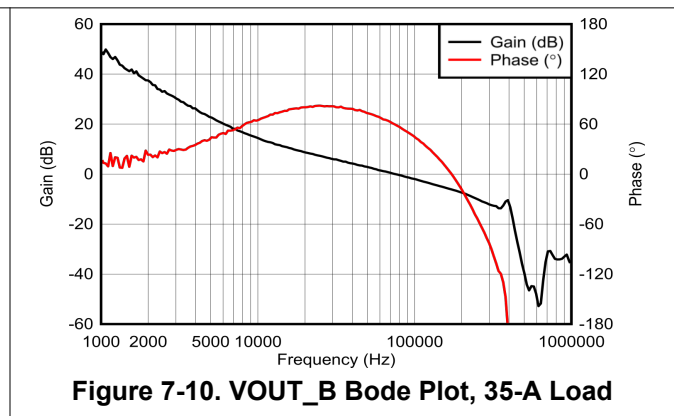
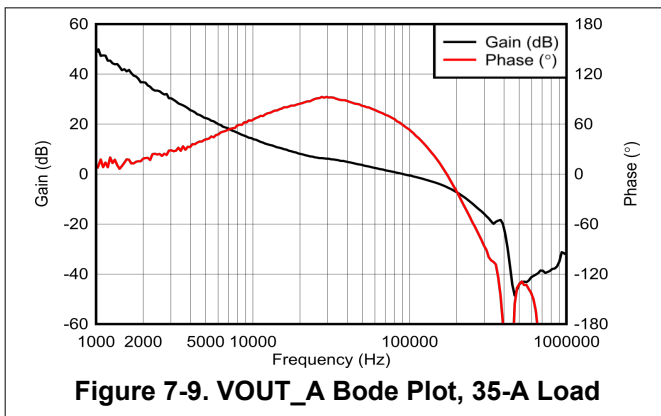


## 7.4 Transient Response

Figure 7-7 and Figure 7-8 show the transient response waveform with a 10-A to 20-A transient at 1 A/μs.

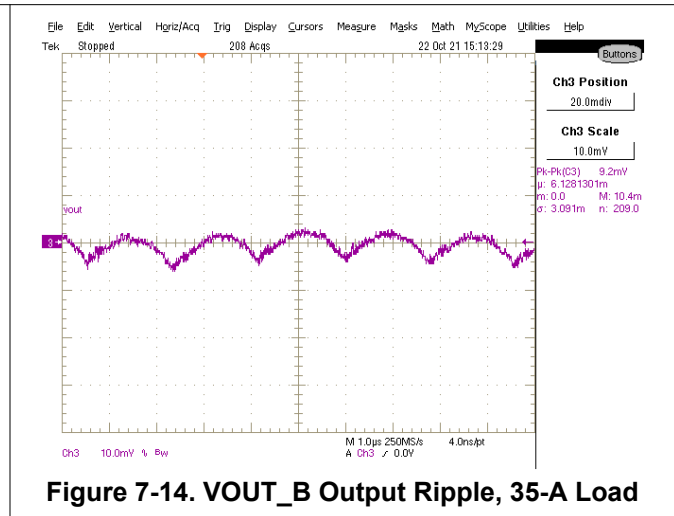
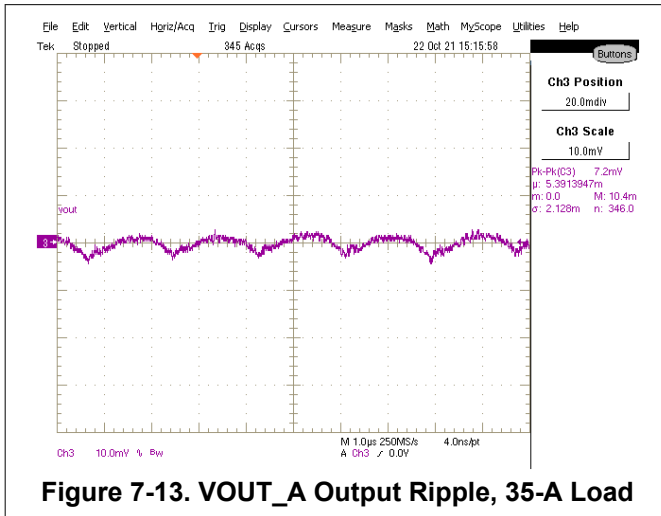
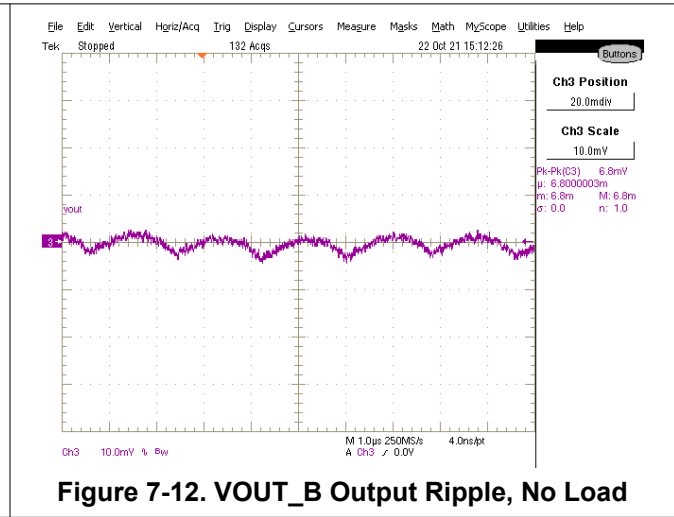
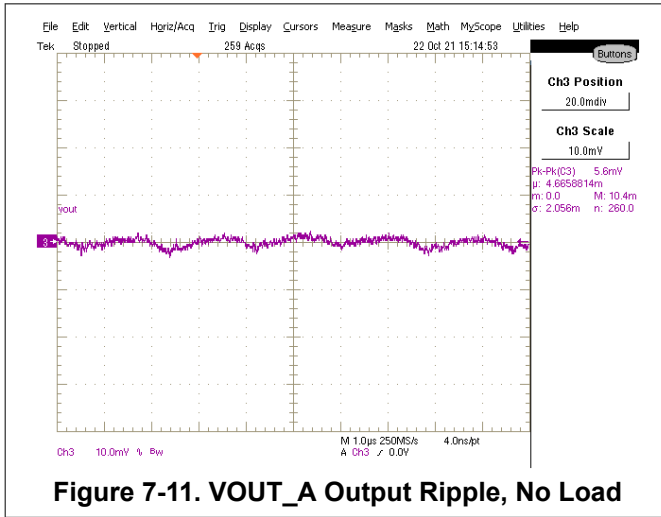


## 7.5 Control Loop Bode Plot



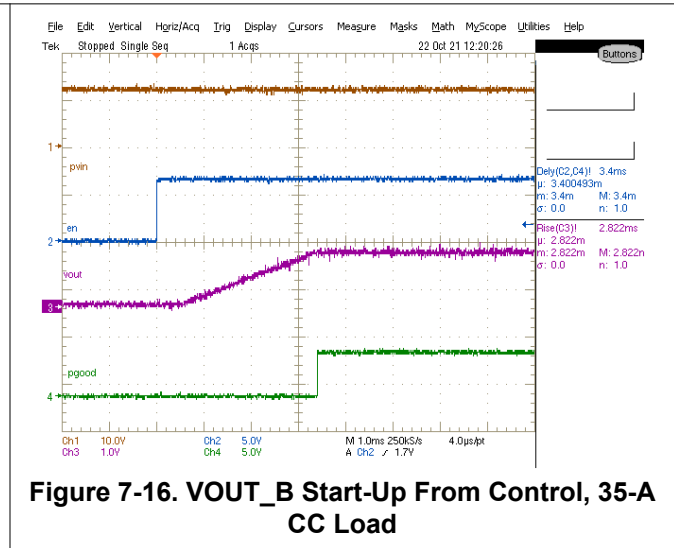
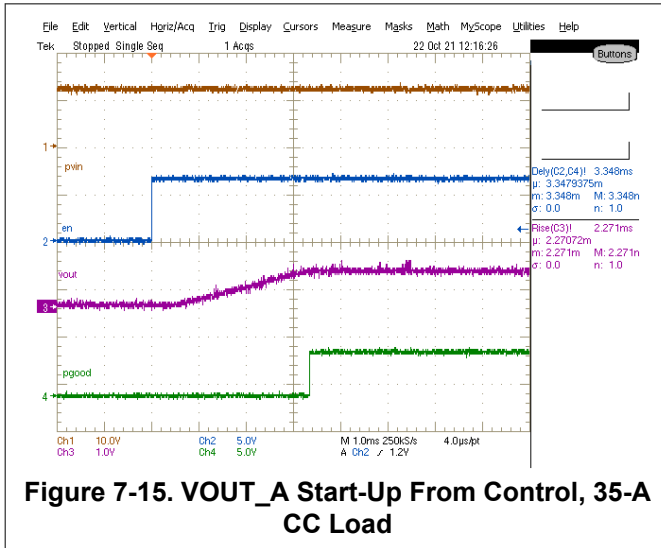
## 7.6 Output Ripple

Figure 7-11 and Figure 7-14 show the output ripple waveforms at 0-A and 35-A load.



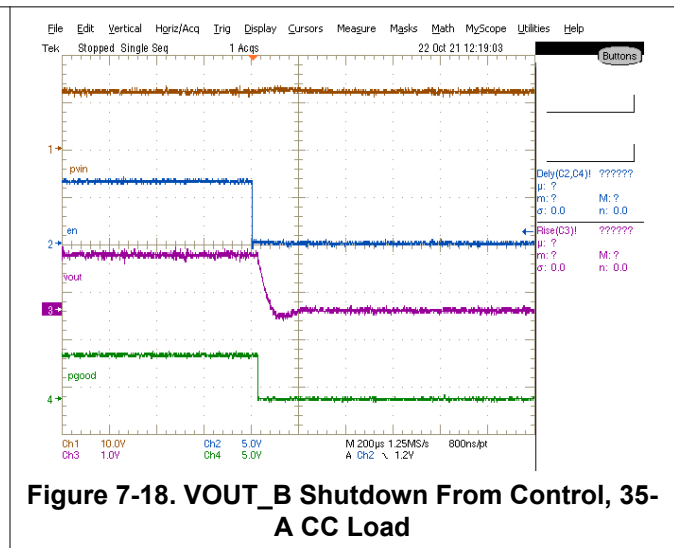
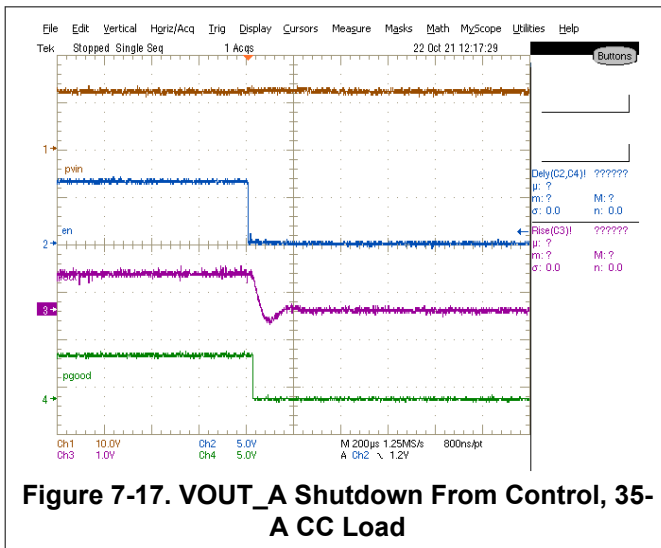
## 7.7 Control On

Figure 7-15 and Figure 7-16 illustrate the start-up from control on waveforms at 35-A outputs.



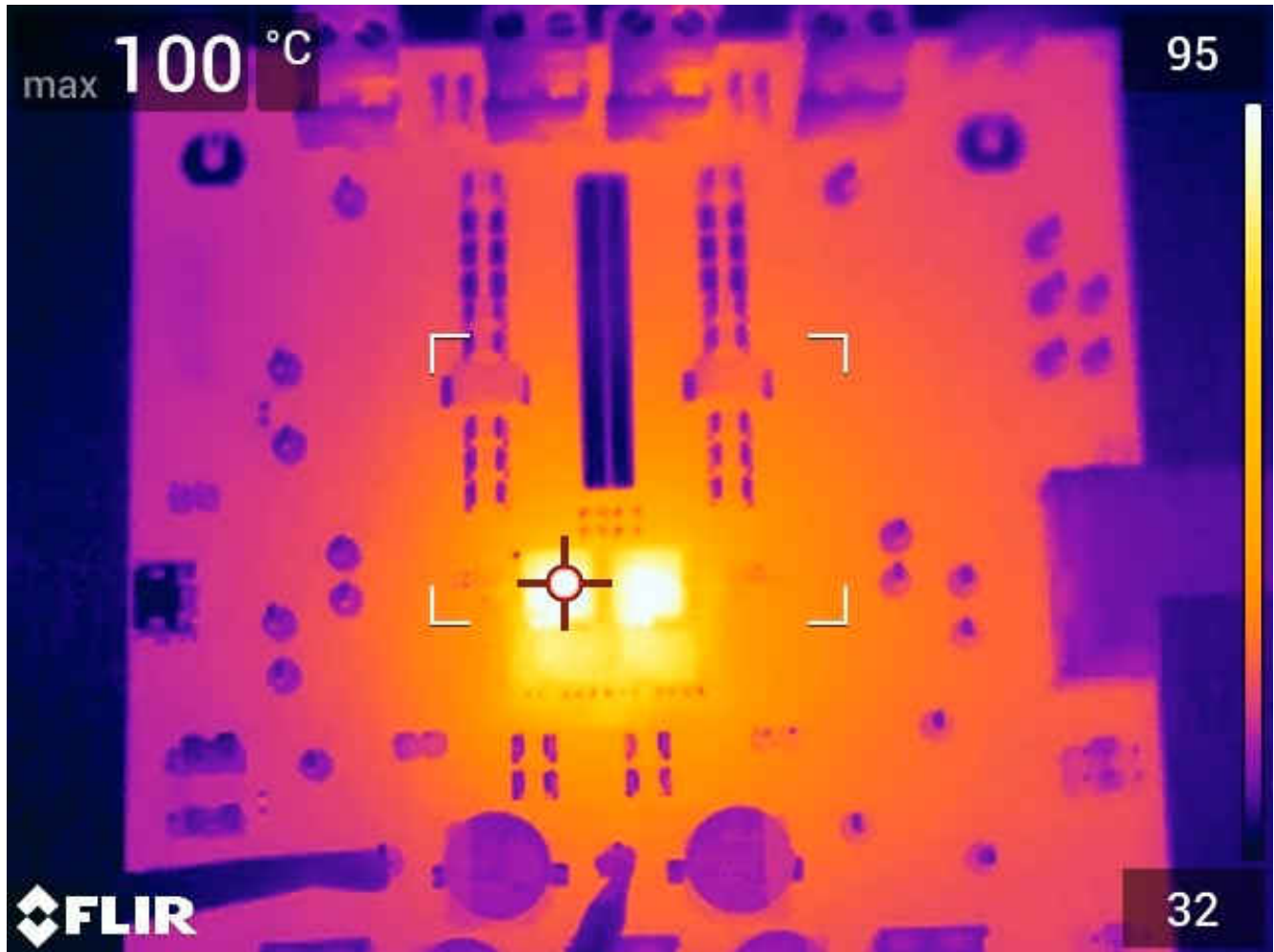
## 7.8 Control Off

Figure 7-17 and Figure 7-18 illustrate the control off waveforms at 35-A outputs.



## 7.9 Thermal Image

Figure 7-19 shows the TPSM8D6C24EVM-2V0 thermal image.



$V_{IN} = 12\text{ V}$ ,  $I_{OUTA} = 35\text{ A}$ ,  $I_{OUTB} = 35\text{ A}$ , Airflow = 200 LFM, 10 minute soak

**Figure 7-19. Thermal Image**

## 8 EVM Assembly Drawing and PCB Layout

Figure 8-1 through Figure 8-8 show the design of the TPSM8D6C24EVM-2V0 printed circuit board.

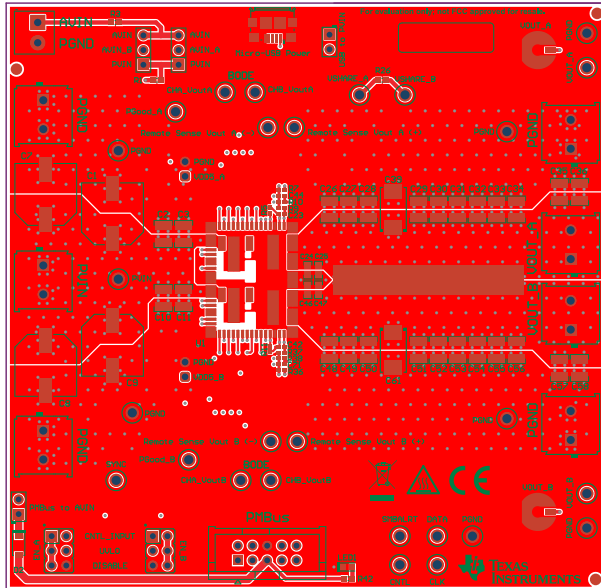


Figure 8-1. TPSM8D6C24EVM-2V0 Top Side Component View (Top View)

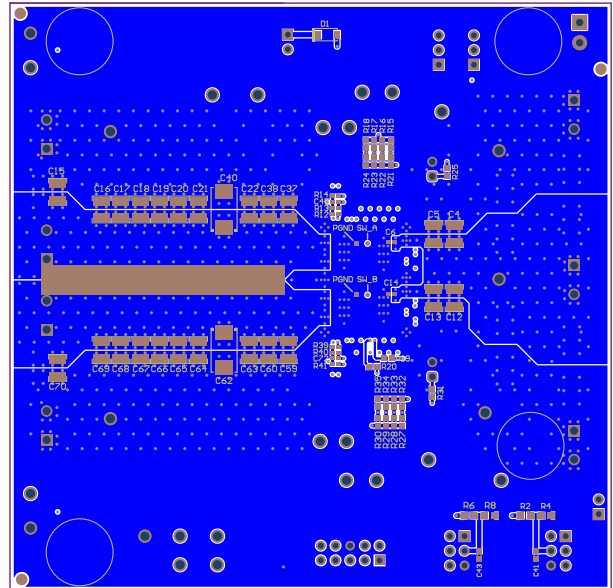


Figure 8-2. TPSM8D6C24EVM-2V0 Bottom Side Component View (Bottom View)

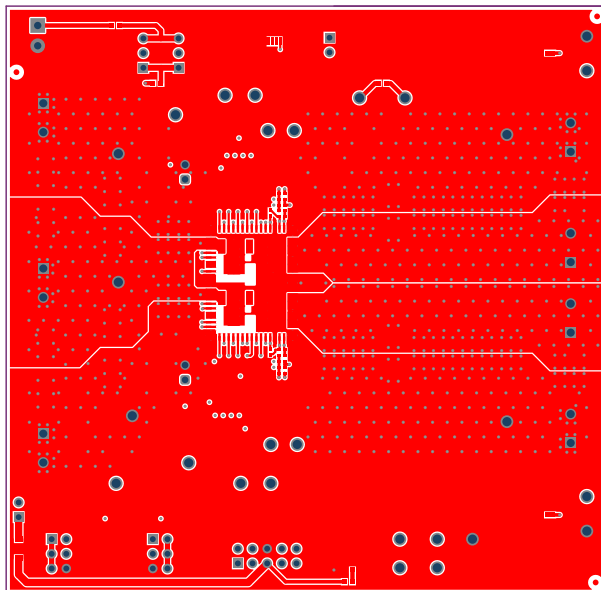


Figure 8-3. TPSM8D6C24EVM-2V0 Top Copper (Top View)

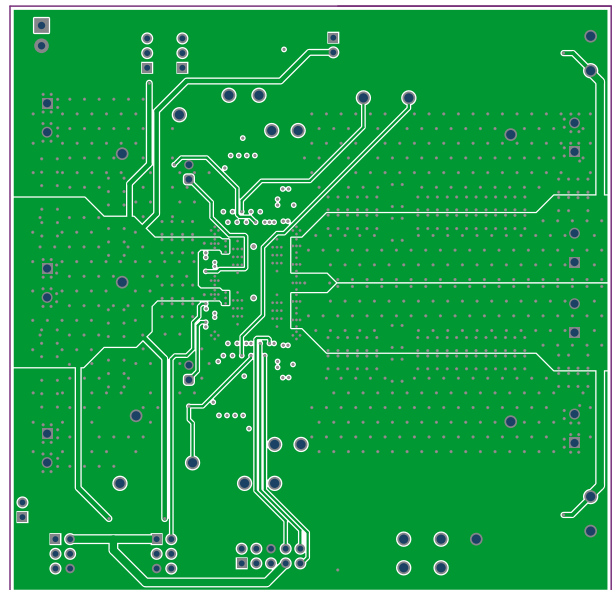
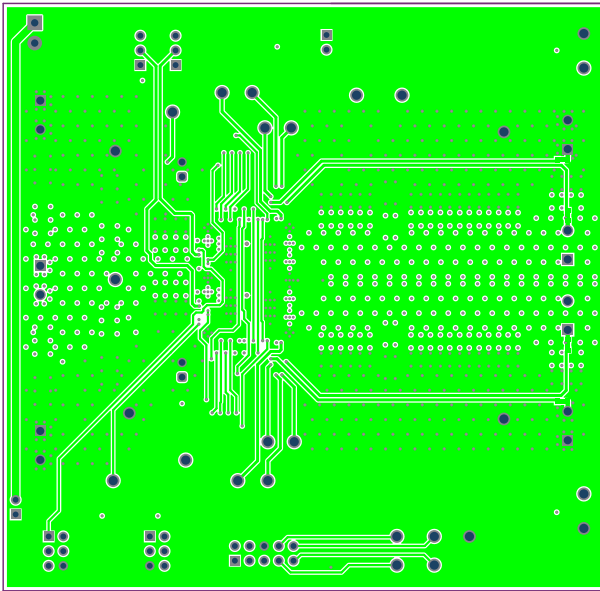
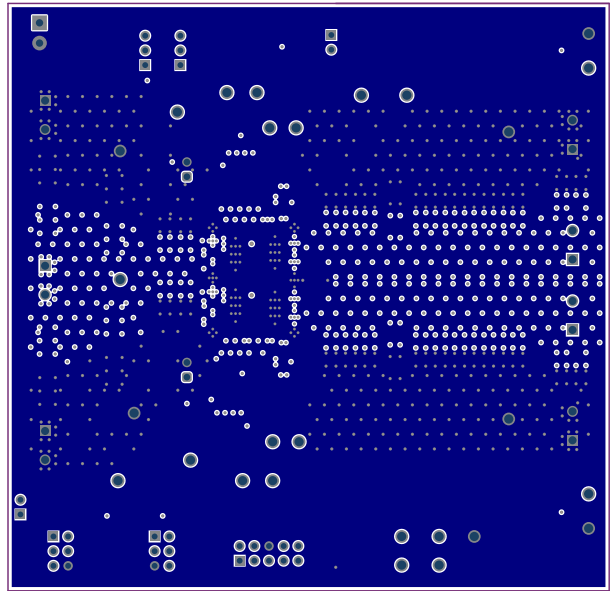


Figure 8-4. TPSM8D6C24EVM-2V0 Internal Layer 1 (Top View)

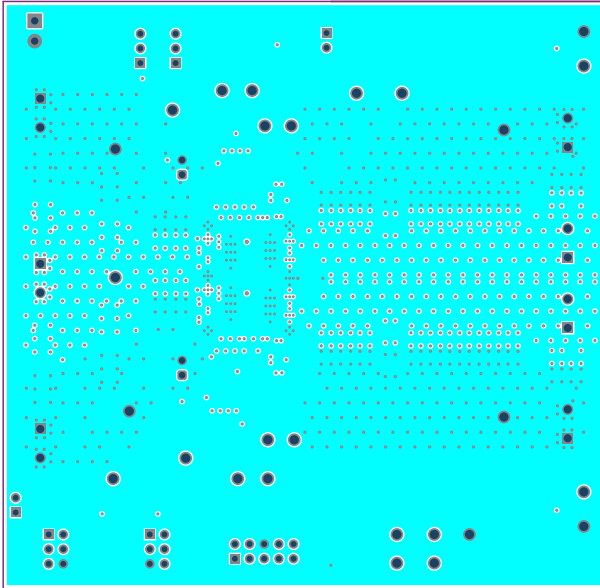




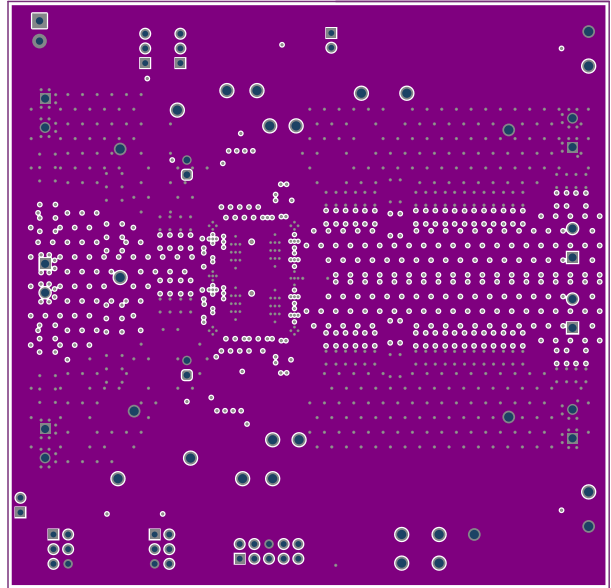
**Figure 8-5. TPSM8D6C24EVM-2V0 Internal Layer 2 (Top View)**



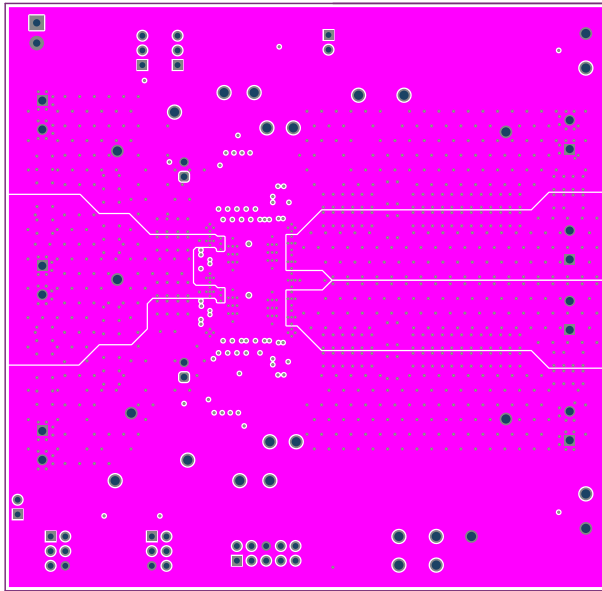
**Figure 8-6. TPSM8D6C24EVM-2V0 Internal Layer 3 (Top View)**



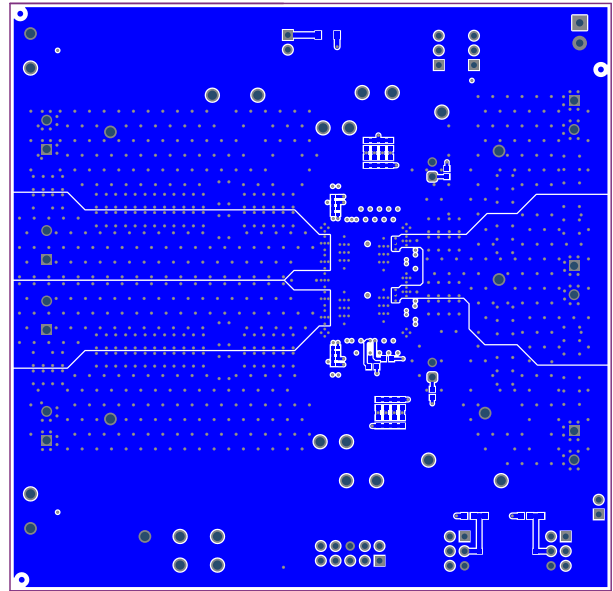
**Figure 8-7. TPSM8D6C24EVM-2V0 Internal Layer 4 (Top View)**



**Figure 8-8. TPSM8D6C24EVM-2V0 Internal Layer 5 (Top View)**



**Figure 8-9. TPSM8D6C24EVM-2V0 Internal Layer 6 (Top View)**



**Figure 8-10. TPSM8D6C24EVM-2V0 Internal Bottom Layer (Top View)**

## 9 Bill of Materials

Table 9-1 lists the BOM for the TPSM8D6C24EVM-2V0.

**Table 9-1. TPSM8D624EVM-2V0 Bill of Materials**

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		BSR192	Any		
C1, C7, C8, C9	4	100 $\mu$ F	CAP, AL, 100 $\mu$ F, 35 V, $\pm$ 20%, 0.15 $\Omega$ , SMD	SMT Radial G	EEE-FC1V101P	Panasonic		
C2, C3, C4, C5, C10, C11, C12, C13	8	22 $\mu$ F	CAP, CERM, 22 $\mu$ F, 25 V, $\pm$ 10%, X6S, 1210	1210	GRM32EC81E226KE15L	MuRata		
C6, C14	2	6800 pF	CAP, CERM, 6800 pF, 50 V, $\pm$ 10%, X7R, 0402	402	GRM155R71H682KA88D	MuRata		
C15, C16, C20, C21, C26, C27, C28, C29, C30, C34, C35, C37, C38, C48, C49, C50, C51, C52, C56, C57, C59, C60, C64, C65, C69, C70	26	47 $\mu$ F	CAP, CERM, 47 $\mu$ F, 10 V, $\pm$ 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata		
C23, C42	2	100 pF	CAP, CERM, 100 pF, 50 V, $\pm$ 10%, X7R, 0402	402	8.85012E+11	Wurth Elektronik		
C24, C25, C46, C47	4	10 $\mu$ F	CAP, CERM, 10 $\mu$ F, 10 V, $\pm$ 20%, X7R, 0603	603	GRM188Z71A106MA73D	MuRata		
C39, C40, C61, C62	4	470 $\mu$ F	CAP, Tantalum Polymer, 470 $\mu$ F, 6.3 V, $\pm$ 20%, 0.01 $\Omega$ , 7343-40 SMD	7343-40	6TPF470MAH	Panasonic		
C41, C43	2	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0603	603	C0603C104K5RACTU	Kemet		
D1, D2	2	30 V	Diode, Schottky, 30 V, 2 A, AEC-Q101, SOD-123FL	SOD-123FL	MBR230LSFT1G	ON Semiconductor		
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	MICRO USB CONN, R/A	1981568-1	TE Connectivity		

**Table 9-1. TPSM8D624EVM-2V0 Bill of Materials (continued)**

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
J2	1		Header (shrouded), 100 mil, 5 × 2, Gold, TH	5 × 2 Shrouded header	5103308-1	TE Connectivity		
JP1, JP2	2		Header, 100 mil, 3 × 1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions		
JP3, JP4	2		Header, 100 mil, 3 × 2, Gold, TH	Sullins 100 mil, 2 × 3, 230 mil above insulator	PBC03DAAN	Sullins Connector Solutions		
JP5, JP6	2		Header, 2.54 mm, 2 × 1, Gold, TH	Header, 2.54 mm, 2 × 1, TH	61300211121	Würth Elektronik		
JP7, JP8	2		Header, 100mil, 2 × 1, Tin, TH	Header, 2 × 1, 100 mil, TH	5-146278-2	TE Connectivity		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	PCB Label 0.650 × 0.200 inch	THT-14-423-10	Brady		
LED1	1	Green	LED, Green, SMD	LED_0603	150060GS75000	Würth Elektronik		
R1, R3	2	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310R0JNEA	Vishay-Dale		
R2, R6	2	30.1 k	RES, 30.1 k, 1%, 0.1 W, 0603	603	RC0603FR-0730K1L	Yageo		
R4, R8	2	11.0 k	RES, 11.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0711KL	Yageo		
R7, R14, R36, R41	4	10	RES, 10.0, 1%, 0.063 W, 0402	402	CRCW040210R0FKED	Vishay-Dale		
R9, R10, R12, R13, R37, R38, R39, R40	8	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	402	ERJ-2RKF49R9X	Panasonic		
R19, R20, R21, R32	4	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic		
R22	1	14.7 k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3EKF1472V	Panasonic		
R23	1	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RCG060310K0FKEA	Vishay Draloric		
R24, R35	2	14.7 k	RES, 14.7 k, 1%, 0.1 W, 0603	603	RC0603FR-0714K7L	Yageo		
R25, R31	2	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo		
R29, R34	2	26.1 k	RES, 26.1 k, 1%, 0.1 W, 0603	603	CRCW060326K1FKEA	Vishay-Dale		
R33	1	68.1 k	RES, 68.1 k, 0.1%, 0.1 W, 0603	603	RG1608P-6812-B-T5	Susumu Co Ltd		

**Table 9-1. TPSM8D624EVM-2V0 Bill of Materials (continued)**

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R42	1	1.00 k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031K00FKEA	Vishay-Dale		
SH-JP1, SH-JP2, SH-JP3, SH-JP4	4	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
SMB1, SMB2	2		Connector, Receptacle, 50 Ω, TH	SMB Connector	SMBR004D00	JAE Electronics		
T1, T2, T3, T5, T6, T7, T8	7		Therminal Block, 5 mm, 2-pole, Tin, TH	TH, 2-Leads, Body 10 × 10mm, Pitch 5 mm	282856-2	TE Connectivity		
T4	1		Terminal Block, 3.5-mm Pitch, 2 × 1, TH	7.0 × 8.2 × 6.5 mm	ED555/2DS	On-Shore Technology		
TP1, TP6, TP18	3		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone		
TP2, TP3, TP4, TP10, TP16, TP22, TP27	7		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone		
TP5, TP7, TP8, TP9, TP11, TP12, TP13, TP14, TP15, TP17, TP19, TP20, TP21, TP23, TP24, TP25, TP26	17		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone		
U1	1		TPSM8D6x24MOW59	MODULE_MOW0059A	TPSM8D6x24MOW59	Texas Instruments		Texas Instruments
C17, C18, C19, C22, C31, C32, C33, C36, C53, C54, C55, C58, C63, C66, C67, C68	0	47 μF	CAP, CERM, 47 μF, 10 V, ±10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata		
C44, C45, C71, C72	0	0.022 μF	CAP, CERM, 0.022 μF, 50 V, ±10%, X7R, 0402	402	GRM155R71H223KA12D	MuRata		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
R5, R11	0	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0402	402	ERJ-2RKF1002X	Panasonic		

**Table 9-1. TPSM8D624EVM-2V0 Bill of Materials (continued)**

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R15, R16, R17, R27, R28	0	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RCG060310K0FKEA	Vishay Draloric		
R18, R30	0	53.6 k	RES, 53.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060353K6FKEA	Vishay-Dale		
R26	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic		

## 10 Using the Fusion GUI

### 10.1 Opening the Fusion GUI

The Fusion GUI should include `IC_DEVICE_ID` in the scanning mode to find TPSM8D6C24. The EVM needs power to be recognized by the Fusion GUI. See [Section 5](#) for the recommended procedure.

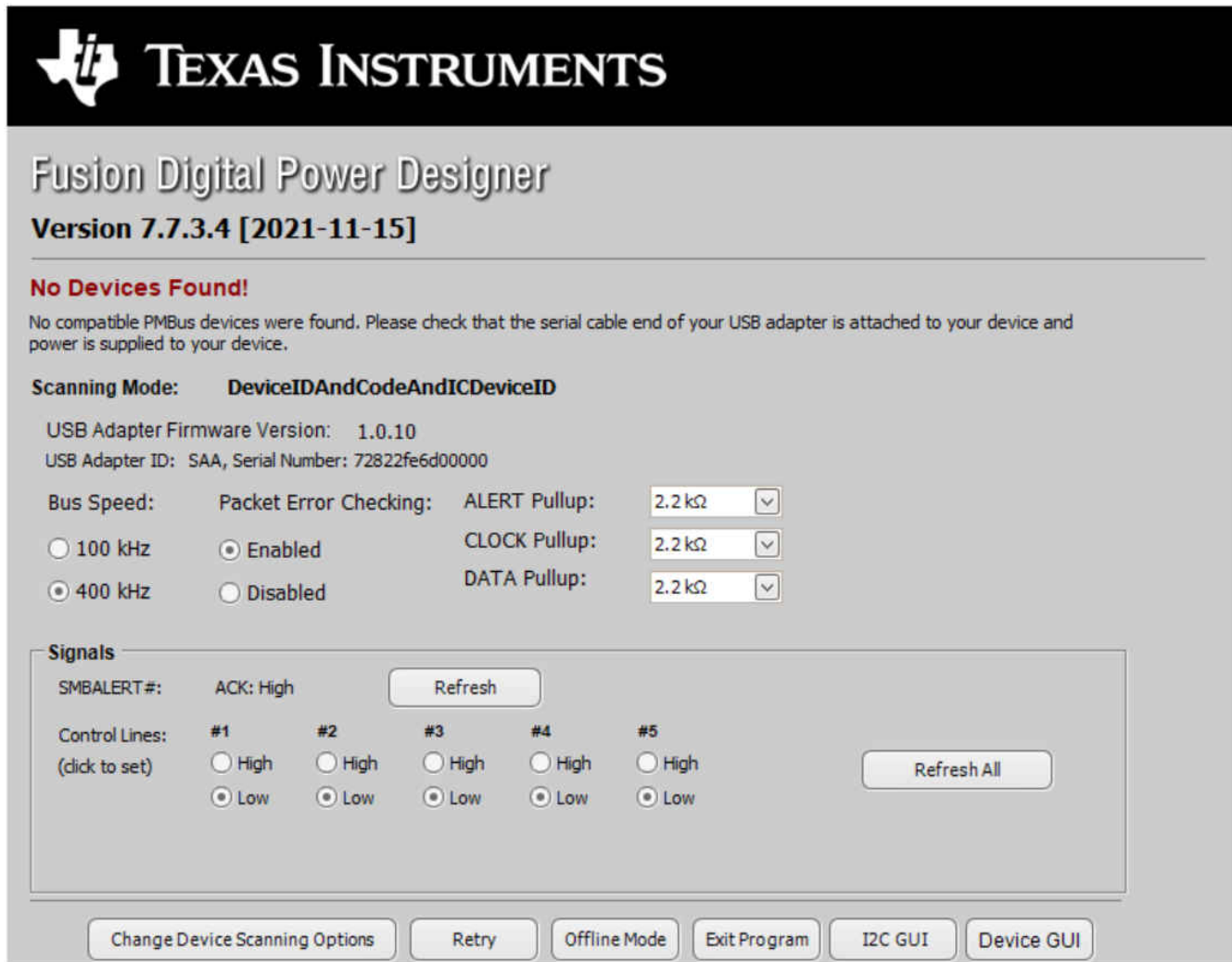


Figure 10-1. Select Device Scanning Mode

## 10.2 General Settings

Figure 10-2 shows the *General Settings* that can be used to configure the following:

- $V_{OUT}$  settings, power good limits, and margin voltages
- OC fault, OC warn, and fault response
- OT fault, OT warn (die temperature) and fault response
- $V_{IN}$  on and off UVLO
- On/Off config
- Soft start (output rise time), other turn-on timing and turn-off timing
- Switching frequency
- Compensation

After clicking *Write to Hardware* to make changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking *Store Config to NVM*. This action prompts a pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in nonvolatile memory.

Both the loop controller device and the loop follower device are tied to same bus interface. In a two-phase stacking system, the loop controller device will receive and respond to all PMBus communication and loop follower devices do not need to be connected to the PMBus. If the controller receives commands which require updates to the PMBus registers of the follower, the controller will relay these commands to the followers. All commands on this tab are for PHASE = 0xFF.

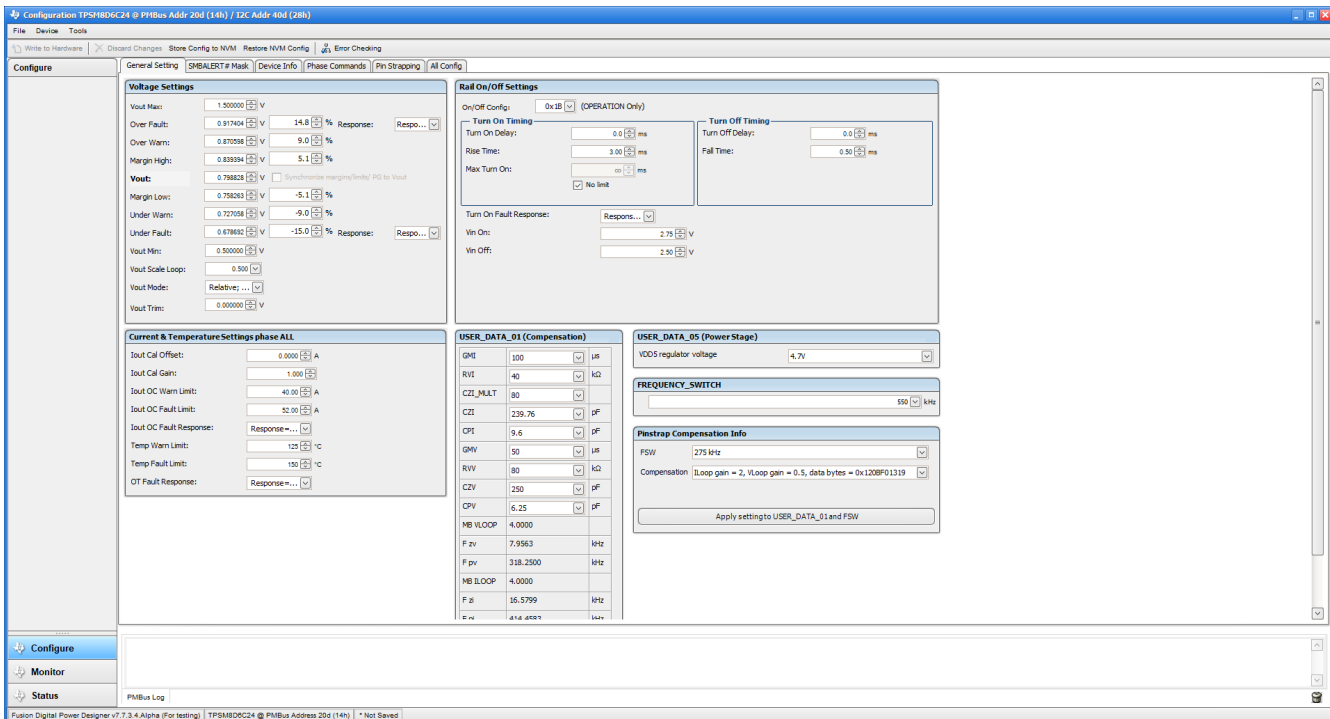


Figure 10-2. General Settings

## 10.3 Changing ON\_OFF\_CONFIG

Changing the *On/Off Config* prompts a pop-up window with details of the options shown in Figure 10-3. This pop-up gives multiple options on what turns on and off power conversion. By default the TPSM8D6C24 is configured to *CONTROL Pin Only*. This is the EN/UVLO pin.



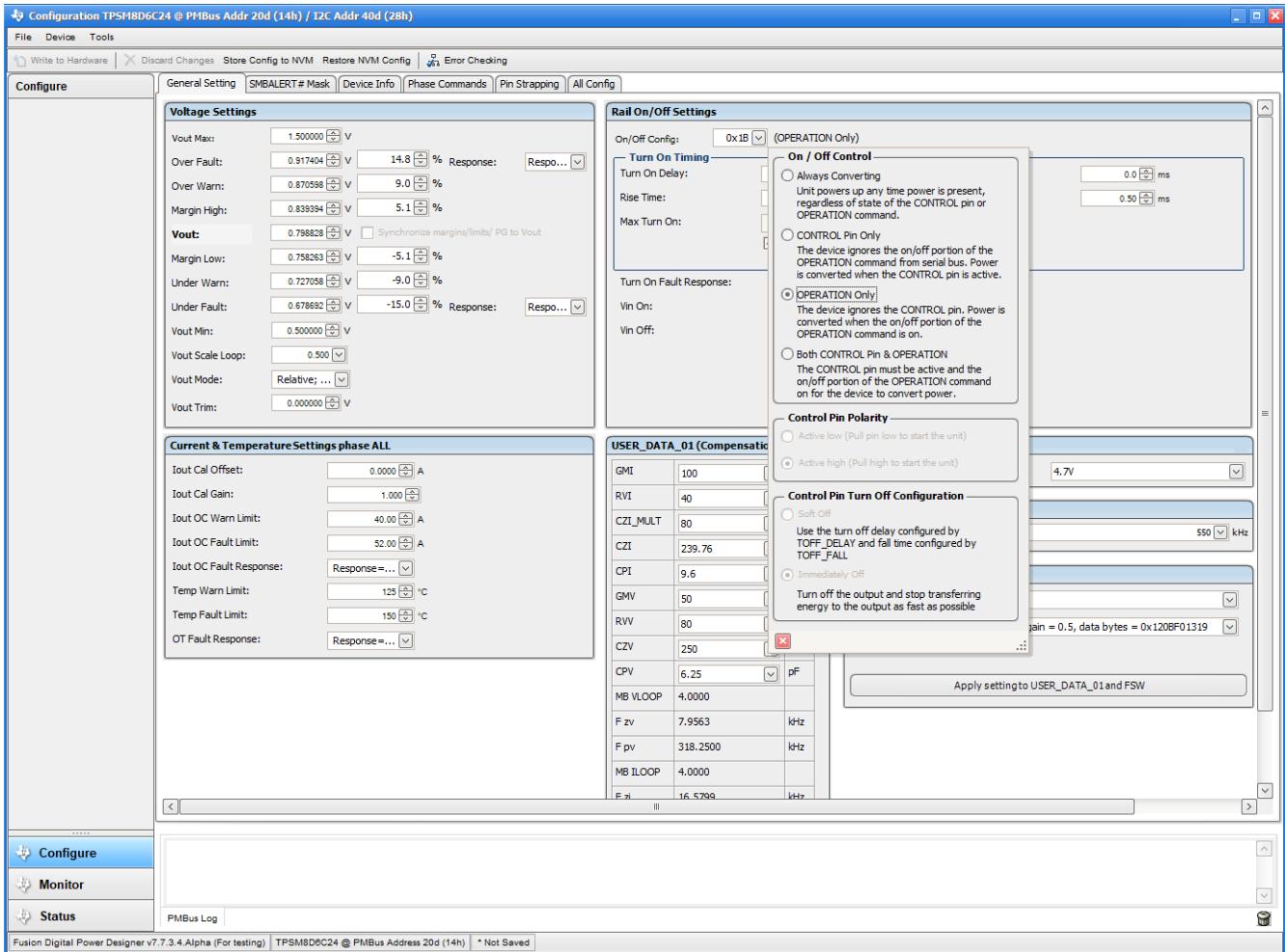
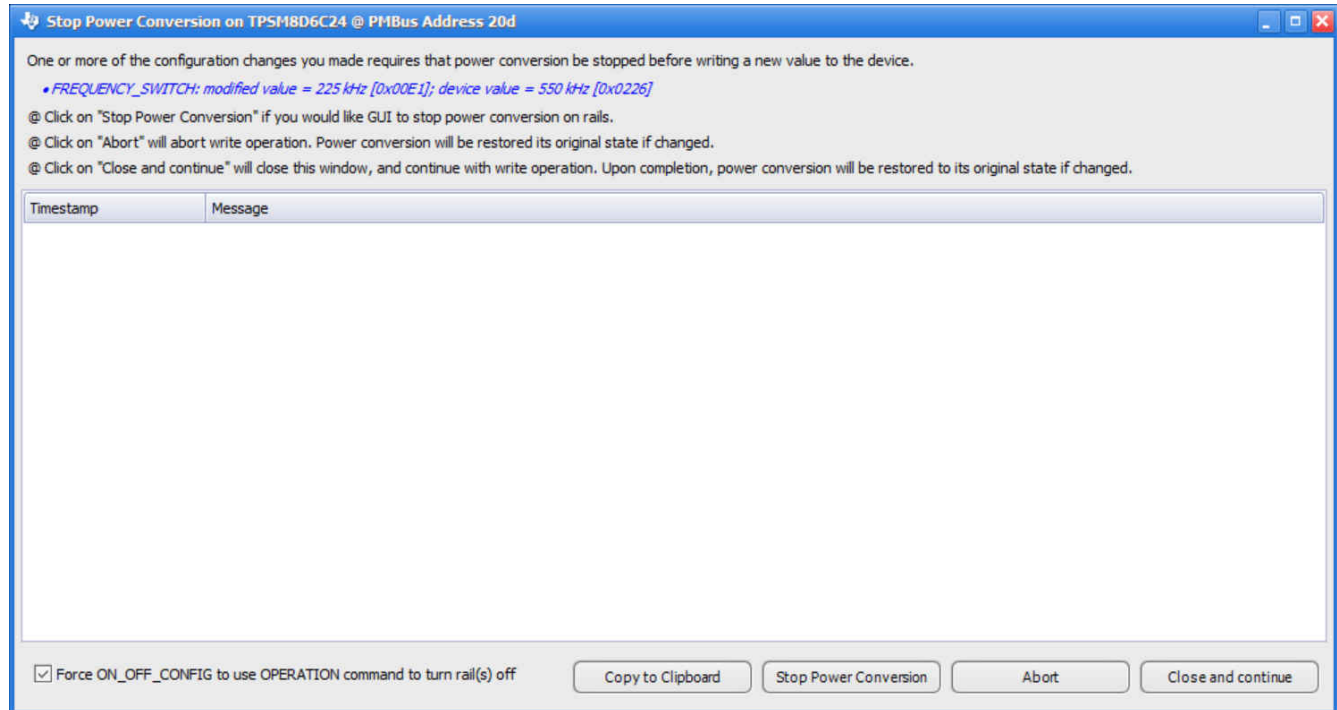


Figure 10-3. Configure – ON\_OFF\_CONFIG

## 10.4 Pop-Up for Some Commands While Conversion is Enabled

Some commands will cause a pop-up like the one shown in [Figure 10-4](#) when trying to change them while conversion is enabled. The settings in the GUI which will cause this pop-up include *FREQUENCY\_SWITCH*, *USER\_DATA\_01 (Compensation)*, *Vout Mode*, and *Vout Scale Loop*. To change these settings to a new value, click on *Stop Power Conversion* then *Close and continue*. The GUI will automatically disable conversion, write the new value, and enable conversion again.



**Figure 10-4. Pop-up When Trying to Change FREQUENCY\_SWITCH With Conversion Enabled**

## 10.5 SMBALERT# Mask

The sources of SMBALERT which can be masked are found and configured on the *SMBALERT # Mask* tab (Figure 10-5).

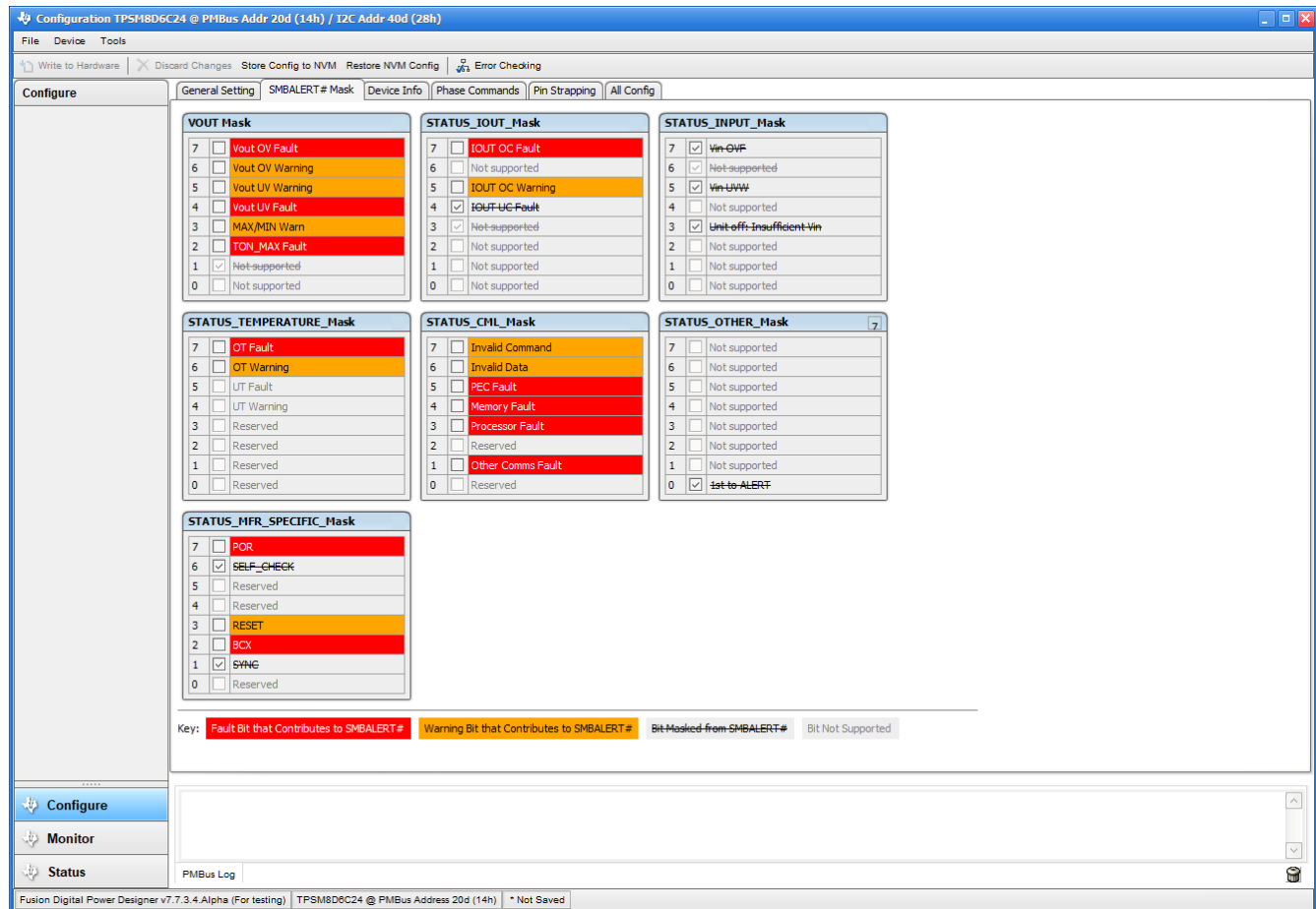


Figure 10-5. Configure – SMBALERT # Mask

## 10.6 Device Info

The device information, Write Protection options, the configuration of *Vout Scale Loop*, *Vout Transition Rate*, and *Iout Cal Offset* are found on the *Device Info* tab (see [Figure 10-6](#)).

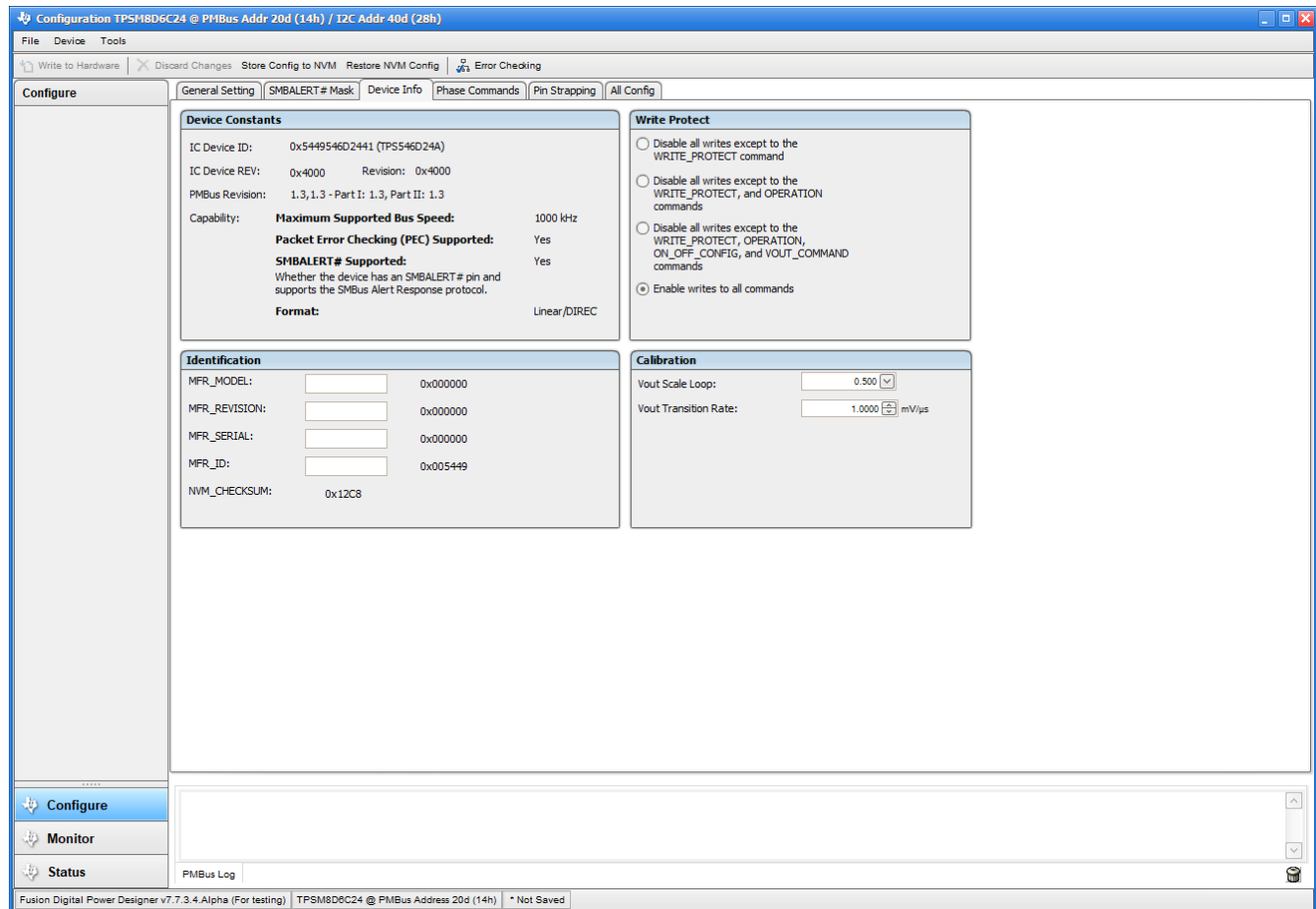
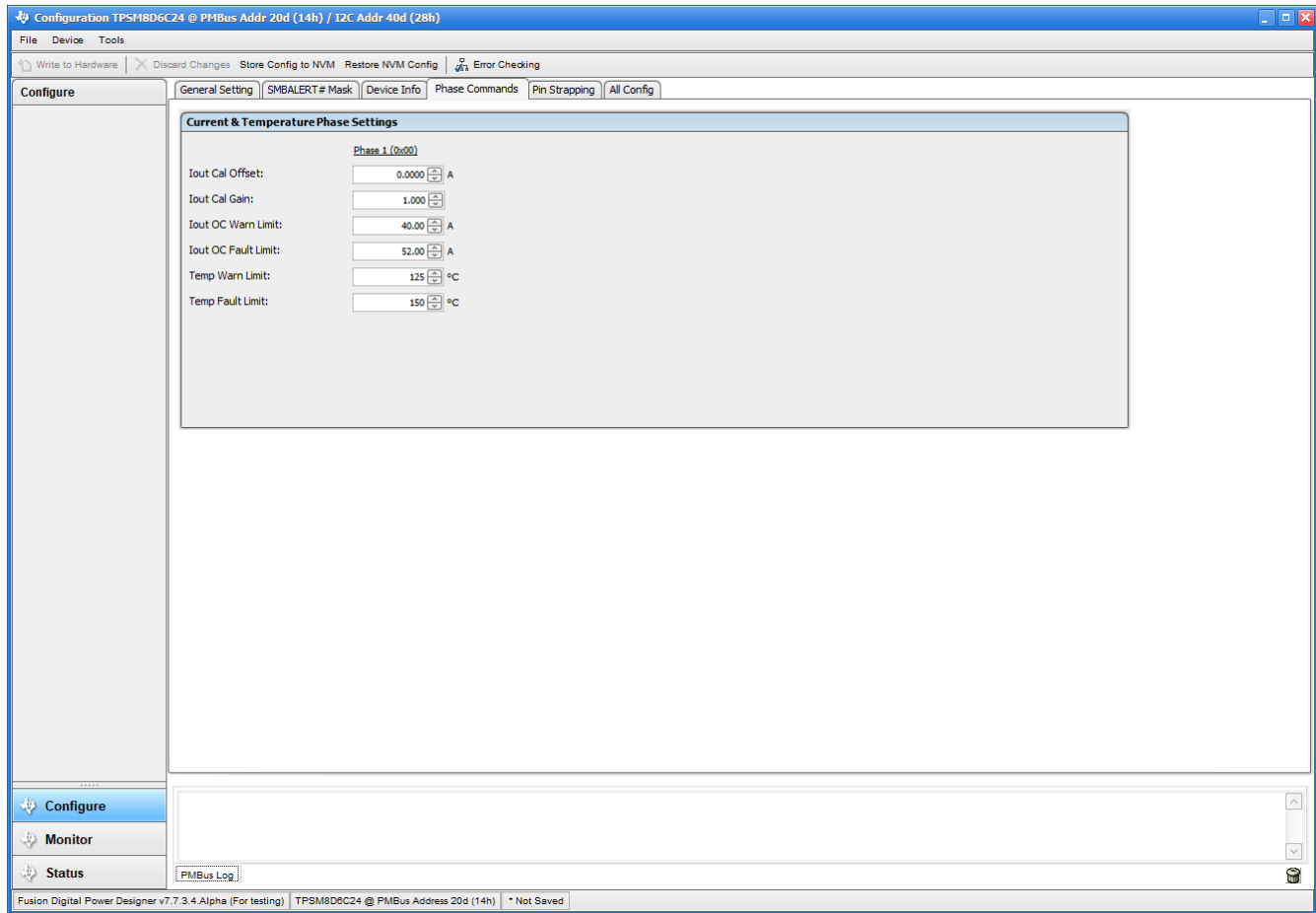


Figure 10-6. Configure – Device Info

## 10.7 Phase Commands

Use the *Phase Command* tab (see [Figure 10-7](#)) to calibrate the *IOUT/Temp* of each phase.



**Figure 10-7. Phase Commands**

## 10.8 All Config

Use the *All Config* tab (Figure 10-8) to configure all of the configurable parameters, which also shows other details like Hex encoding.

The screenshot displays the 'All Config' tab in the Fusion GUI. The main area is divided into two panes, each containing a table of configuration parameters. The left pane lists parameters under various categories, and the right pane shows manufacturer information and status parameters. The bottom of the window features a PMBus Log and system information.

Command	Code	Value/Edit	Hex/Edit
<b>Calibration</b>			
VOUT_TRIM	0x22	0.000000 V	0x0000
VOUT_SCALE_LOOP	0x29	0.500	0xC840
IOUT_CAL_GAIN phase ALL	0x38	1.000	0xC880
IOUT_CAL_OFFSET phase ALL	0x39	0.0000 A	0xE000
<b>Configuration</b>			
WRITE_PROTECT	0x10	0x00	0x00
SMBALERT_MASK_CML	0x1B	00000000	0x00
SMBALERT_MASK_INPUT	0x1B	11101000	0xE8
SMBALERT_MASK_IOUT	0x1B	00011000	0x18
SMBALERT_MASK_MFR_SPECIFIC	0x1B	01000010	0x42
SMBALERT_MASK_OTHER	0x1B	00000001	0x01
SMBALERT_MASK_TEMPERATURE	0x1B	00000000	0x00
SMBALERT_MASK_VOUT	0x1B	00000010	0x02
VOUT_MODE	0x20	Relative...	0x97
VOUT_COMMAND	0x21	0.798828 V	0x0199
VOUT_MAX	0x24	1.500000 V	0x0300
VOUT_MARGIN_HIGH	0x25	0.839394 V	0x021A
VOUT_MARGIN_LDW	0x26	0.758283 V	0x01E6
VOUT_TRANSITION_RATE	0x27	1.0000 mV/μs	0xE010
VOUT_MIN	0x2B	0.500000 V	0x0100
FREQUENCY_SWITCH	0x33	550 kHz	0x0226
INTERLEAVE	0x37	Group ID...	0x0020
IC_DEVICE_ID	0xAD	0x54495...	0x54...
IC_DEVICE_REV	0xAE	0x4000	0x4000
TELEMETRY_CONFIG [MFR 00]	0xD0	VOUT; Pr...	0x03...
PGOOD_CONFIG [MFR 19]	0xE3	PGOOD O...	0x009F
<b>Manufacturer Info</b>			
CAPABILITY	0x19	0x00	0x00
PMBUS_REVISION	0x98	0x33	0x33
MFR_ID	0x99		0x00...
MFR_MODEL	0x9A		0x00...
MFR_REVISION	0x9B		0x00...
MFR_SERIAL	0x9E		0x00...
<b>On/Off Configuration</b>			
OPERATION	0x01	0x84	0x84
ON_OFF_CONFIG phase ALL	0x02	0x1B	0x1B
TON_DELAY	0x60	0.0 ms	0xF800
TON_RISE	0x61	3.00 ms	0xF00C
TON_MAX_FAULT_LIMIT	0x62	0 ms	0xF800
TON_MAX_FAULT_RESPONSE	0x63	Click...	0x3B
TOFF_DELAY	0x64	0.0 ms	0xF800
TOFF_FALL	0x65	0.50 ms	0xF002
<b>Status</b>			
STATUS_BYTE	0x78	01000000	0x40
STATUS_WORD	0x79	Click...	0x0000
STATUS_VOUT	0x7A	00000000	0x00
STATUS_IOUT	0x7B	00000000	0x00
STATUS_INPUT	0x7C	00000000	0x00
STATUS_TEMPERATURE	0x7D	00000000	0x00
STATUS_CML	0x7E	00000000	0x00
STATUS_OTHER	0x7F	00000000	0x00
READ_VIN phase ALL	0x88	4.758 V	0xCA61
READ_VOUT phase ALL	0x88	0.794922 V	0x0197

17:18:29.654: USB-SAA #1: CONTROL1 now Low  
 17:18:29.656: USB-SAA #1: CONTROL2 now Low  
 17:18:29.657: USB-SAA #1: CONTROL3 now Low  
 17:18:29.658: USB-SAA #1: CONTROL4 now Low  
 17:18:29.659: USB-SAA #1: CONTROL5 now Low

Fusion Digital Power Designer v7.3.4.Alpha (For testing) TPSM8D6C24 @ PMBus Address 20d (14h) \* Not Saved

Figure 10-8. Configure – All Config

## 10.9 Pin Strapping

Use the *Pin Strapping* tab (Figure 10-8) to aid in selection of external pin strapping resistors used to program some of the PMBus commands at power up. The *EEPROM Value* column shows the values currently configured to the related PMBus commands.

Pin	PMBus Command	Pinstrap Setting	Info	Pin Detect Override				EEPROM Value	*
				R_Divider		R_Bot			
				Code	kΩ	Code	kΩ		
MSEL1	COMPENSATION CONFIG	ILOOP gain = EEPROM; VLOOP gain = EE...	EEPROM	Open	DNP	Open	DNP	ILOOP gain = 4, VLOOP gain = 4 (0x1240422246)	*
	FREQUENCY SWITCH	275 kHz						550.000 kHz	*
MSEL2	OC FAULT/OC_WARN	OCF = 52, OCW = 40 A						52 / 40 A	
	TON_RISE	0.50 ms		0	21.500 kΩ	0	4.640 kΩ	3 ms	
	Num Slaves sharing VOUT	None, Stand alone						0 slave	
	Voltage Range	EEPROM						0.5 to 1.5 V	
VSEL	VOUT COMMAND	EEPROM		Open	DNP	Short	0.000 Ω	0.798828125 V	

Figure 10-9. Configure – Pin Strapping

## 10.10 Monitor

When the *Monitor* screen (Figure 10-10) is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of *Vout*, *Iout*, *Vin*, *Pout*, and *Temperature*
- *Start and Stop Polling* which turns ON or OFF the realtime display of data
- Quick access to *On/Off Config*
- Control pin activation and *OPERATION* command
- Margin control
- Clear Fault: Selecting **Clear Faults** clears any prior fault flags.

With two devices stacked together, the *Iout* reading is the total load supported by both devices. There is also an *Iout* which shows the current in each phase.

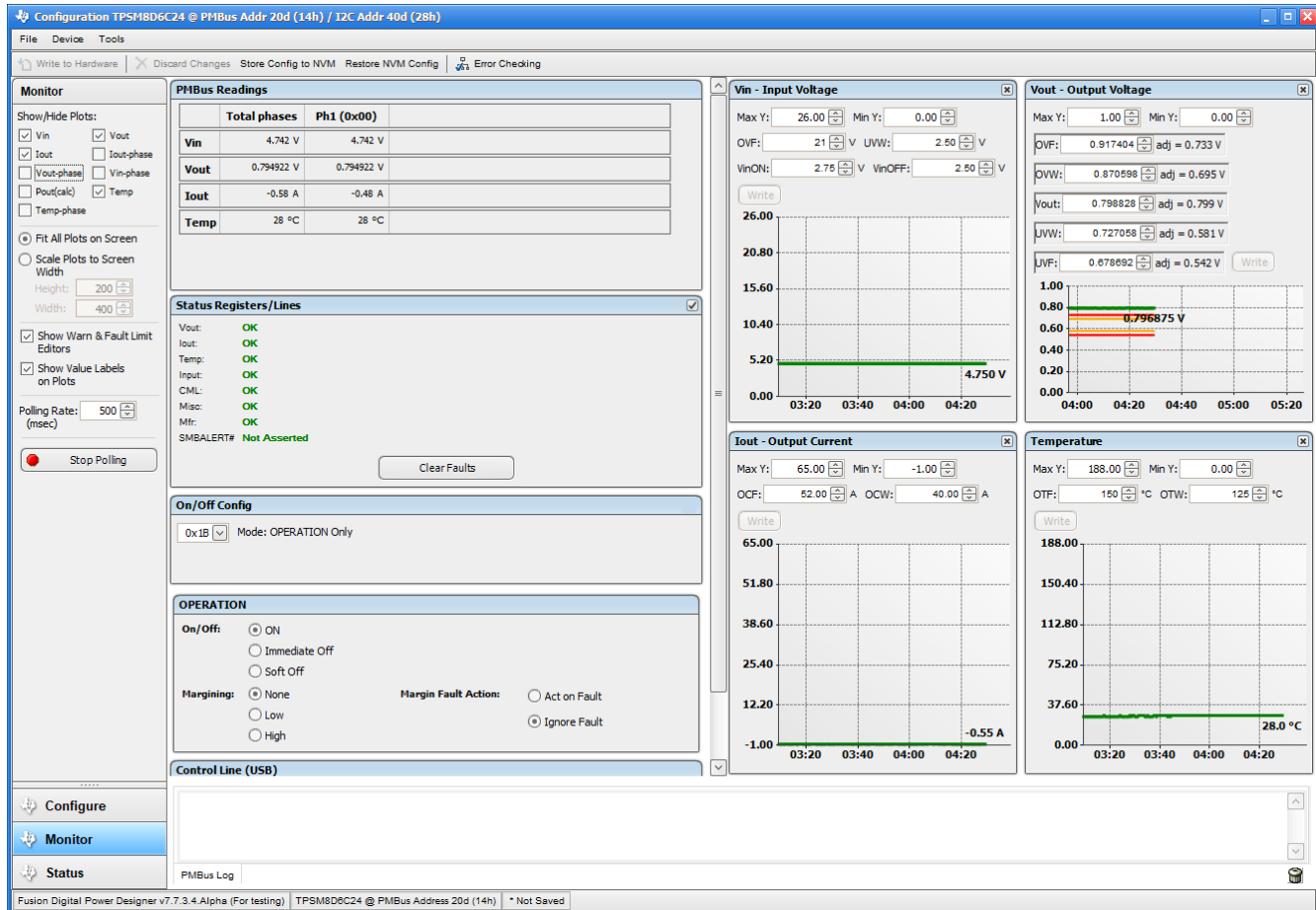


Figure 10-10. Monitor Screen



## 10.11 Status

Selecting *Status* screen from lower left corner (Figure 10-11) shows the status of the device.

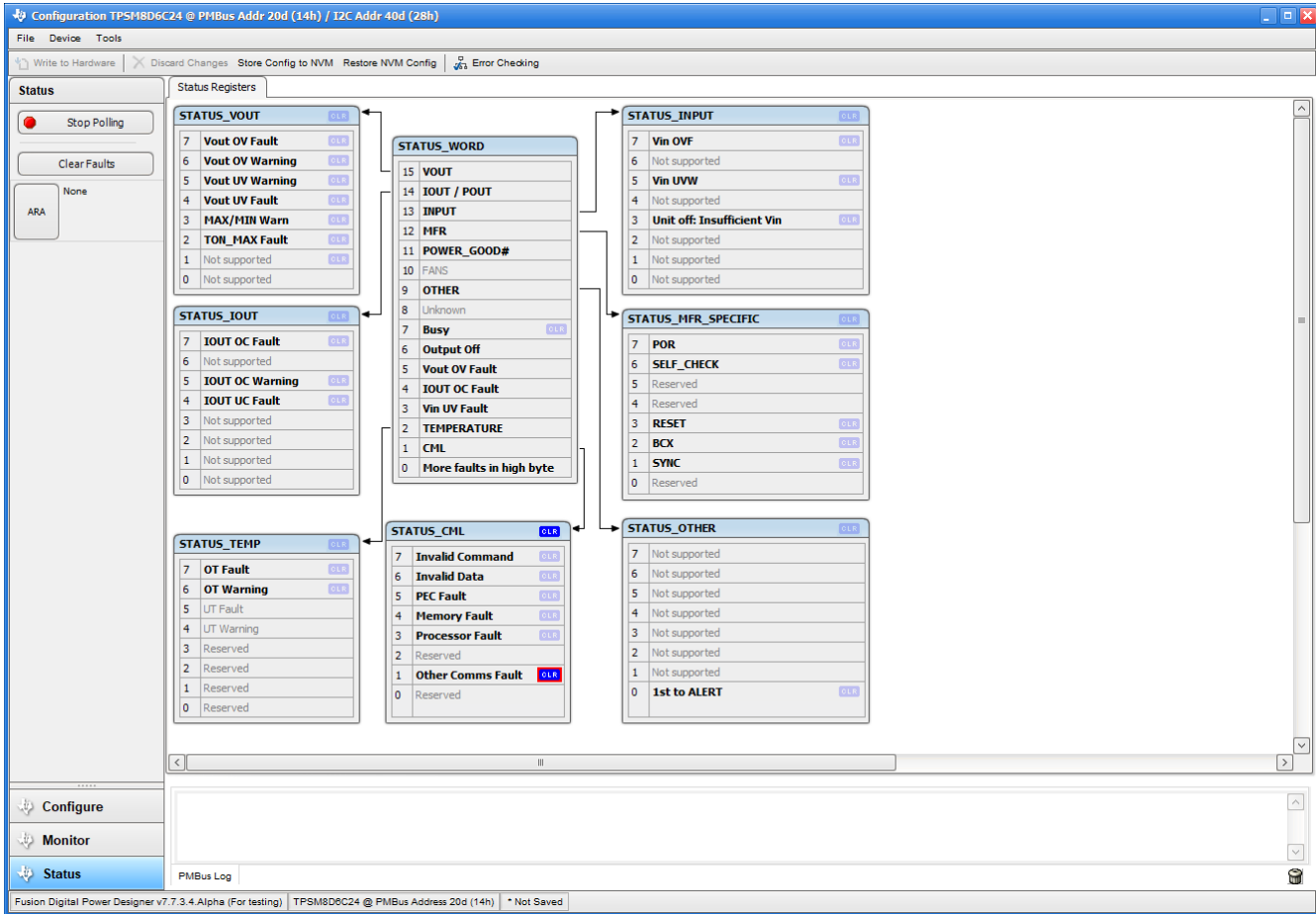


Figure 10-11. Status Screen

## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	3
• Updated user's guide title.....	3

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