Application Report

SLVA210B–August 2005–Revised March 2010

Using Ceramic Output Capacitors with the TPS6420x Buck Controllers

Jeff Falin, Arvind Raj, Ankur Verma

ABSTRACT

This application report describes the design process required while using ceramic capacitors or capacitors with low ESR at the output of TPS6420x buck controllers. Additional passive components are required to ensure the proper operation of the circuit.

1 Introduction

The TPS6420x buck controllers have comparators that monitor the output voltage ripple in order to determine when to turn on or turn off the high-side FET. For the comparator to operate properly, the output ripple should be proportional to and in phase with the inductor current. This depends upon the output capacitor, whose behavior for different ESR values is shown below:

1. ESR in the range of 30mΩ to 150mΩ produce in-phase ripple voltage, and work properly without the need of any additional components.
2. ESR larger than 150mΩ also works, but typically generate an unacceptably high ripple voltage. Larger value inductors reduce the inductor ripple current, thereby reducing the output ripple voltage
3. With ESR less than 30mΩ, a ceramic output capacitor produces output ripple that is dominated by the output capacitance and has a phase lag relative to the inductor current ripple. This phase lag causes the control loop to turn on and turn off the switch at the wrong time. At light load, the output ripple is larger than expected resulting in poor regulation. The transient performance also suffers. At heavy load, the switching frequency is faster than predicted resulting in poorer efficiency. There may be significant duty cycle jitter also. To use a ceramic capacitor or other low ESR output capacitors with the TPS6420x, three additional passive components are required.

This document explains the design process when the output capacitors used fall into the third range.

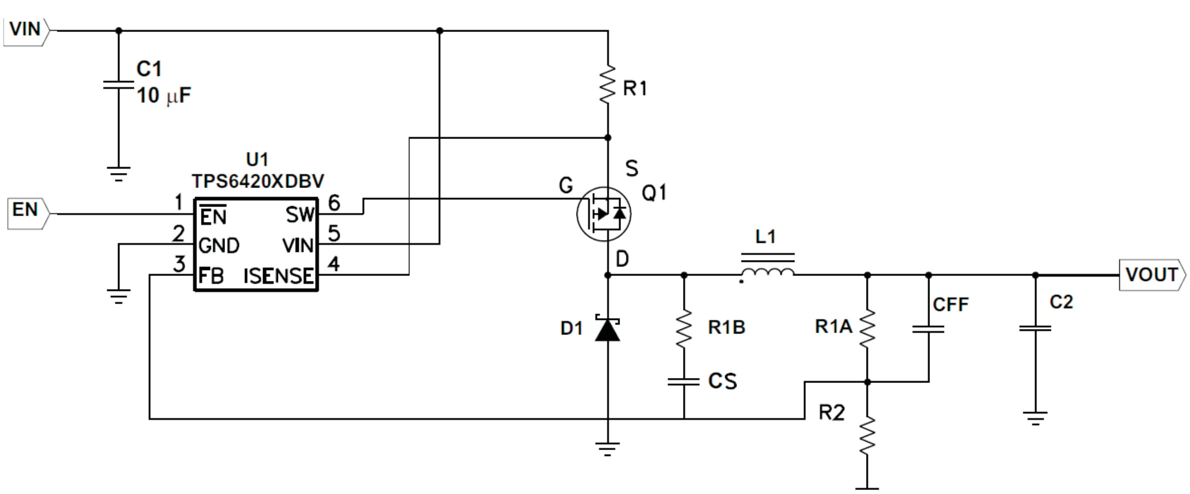

Figure 1. Step-Down Converter Using TPS6420x With Ceramic Output Capacitors

2 Design Process

The three components required, as shown in Figure 1 are:

1. **Feedforward resistor, R1B:** The feedforward resistor R1B injects the required ripple into the FB pin from the switch node.
2. **DC blocking capacitor, C_S:** The series capacitor C_S eliminates the effect of R1B on R1A; and therefore, the DC output voltage regulation point. At higher load currents, this capacitor stores the voltage drop across the inductor's DCR. This drop introduces an offset to the DC output voltage regulation point.
3. **Feedforward capacitor, C_{ff}:** The feedforward capacitor C_{ff} provides an ac coupling path between V_{OUT} and the FB pin which reduces the output ripple. Therefore, the user must ensure that the impedance of C_{ff} is less than R1A at the operating frequency.

During the on-time of the high-side FET, the constant current of (V_{IN} -V_{OUT}) / R1B charges C_{ff}. Based on:

$$\frac{V_{IN} - V_{OUT}}{R1B} = \frac{C_{ff} \ x \ V_{HYS}}{t_{on}} \tag{1}$$

Where:

V_{IN} = Input voltage
V_{OUT} = Output voltage
V_{HYS} = Hysteresis of the internal comparator, assumed to be 12mV
t_{on} = Minimum on time of the TPS6420x

Assuming a fixed value for C_{ff} and $C_S \approx 20$ times C_{ff},

$$R1B = \frac{\left(V_{IN} - V_{OUT}\right) \ x \ \left(t_{on}\right)}{C_{ff} \ x \ V_{HYS}} \tag{2}$$

Similarly, during the off time of the high-side FET, the voltage across C_{ff} ramps down due to the current sink of V_{OUT} / R1B. Therefore, again based on :

$$\frac{V_{OUT}}{R1B} = \frac{C_{ff} \ x \ V_{HYS}}{t_{off}} \tag{3}$$

Assuming a fixed value for C_{ff} and $C_S \approx 20$ times C_{ff}:

$$R1B = \frac{V_{OUT} \ x \ \left(t_{off}\right)}{C_{ff} \ x \ V_{HYS}} \tag{4}$$

The lesser of the two calculated values of R1B is selected so that, the minimum ripple on the FB pin is V_{HYS}, irrespective of whether the part is operating in minimum on-time or the minimum off-time mode. C_S is chosen such that its value is approximately 20 times higher than C_{ff}.

3 Example

Example given below using the TPS64200 justifies the above theory. The TPS64200 has a minimum on-time of 1.6µs and a minimum off-time of 0.55µs. At the following specifications, using the design spreadsheet tool at SLVS038, switching frequency, operation mode and other parameters are determined.

Input Voltage = 3.3V
Output Voltage = 1.5V
Output Current (Max) = 3A
Switching frequency = 363KHz
Operation Mode = Minimum-on time
Setting R2 = 365K and using R1A = R2 x (V_{OUT}/V_{REF} - 1) gives R1A = 86.6K.

Fixing C_{ff} = 470pF, R1B is 196K using the lesser of the values calculated using Equation 2 and Equation 4. Capacitance of 0.01µF is used for C_S.

The 200-mA to 2.8-A load transient step response is shown in Figure 2. The bottom trace is the output voltage (200mV/div) and the top trace is the inductor current (1A/div).

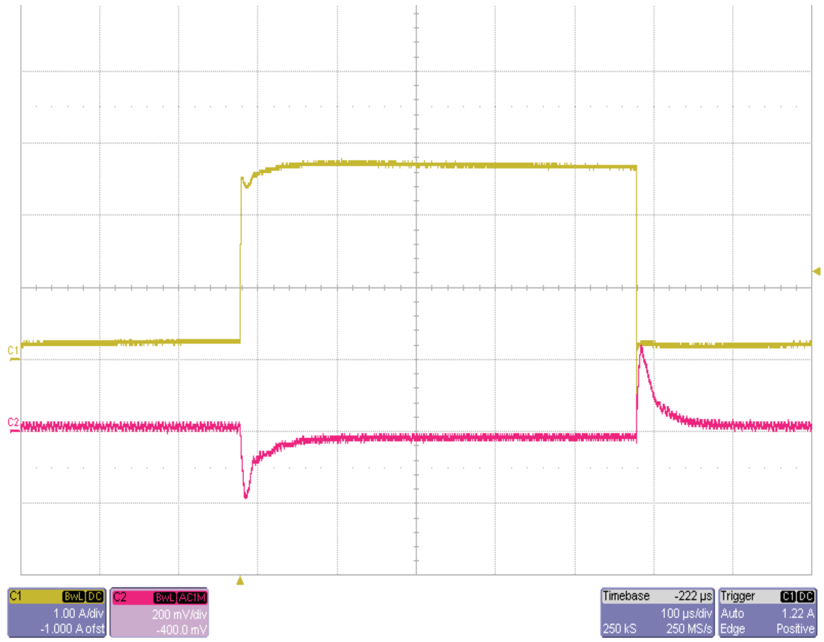

Figure 2. Load Transient Response

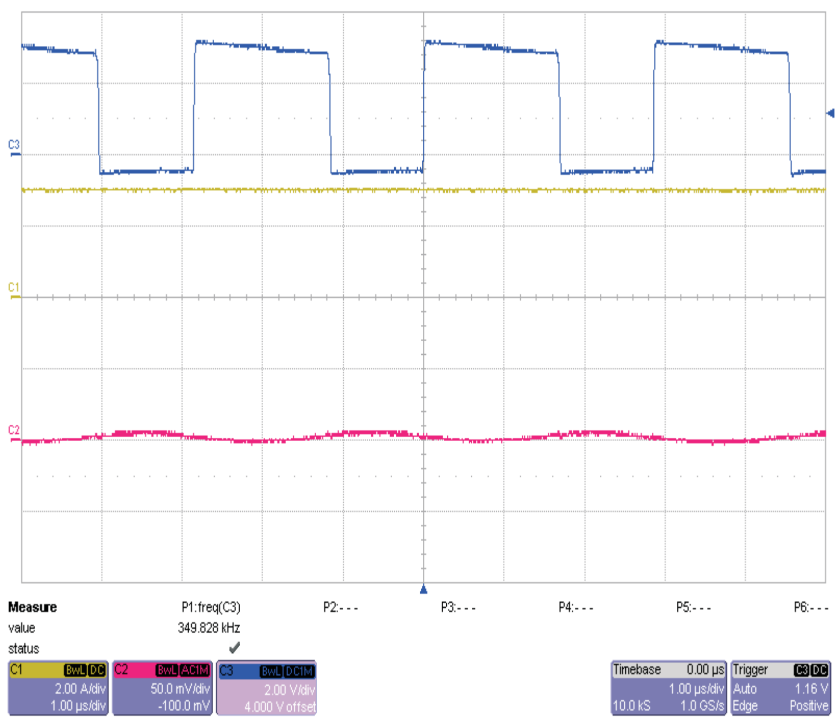

Figure 3. Switch Node (2V/div), Output Current (2A/div), and Output Ripple (50mV/div) at 2.8-A Load Current

The predicted switching frequency at heavy load per the spreadsheet tool is 363 kHz, while the measured switching is within an acceptable margin at approximately 350 kHz.

Figure 4 shows the output ripple at light load (I_{OUT} = 100mA).

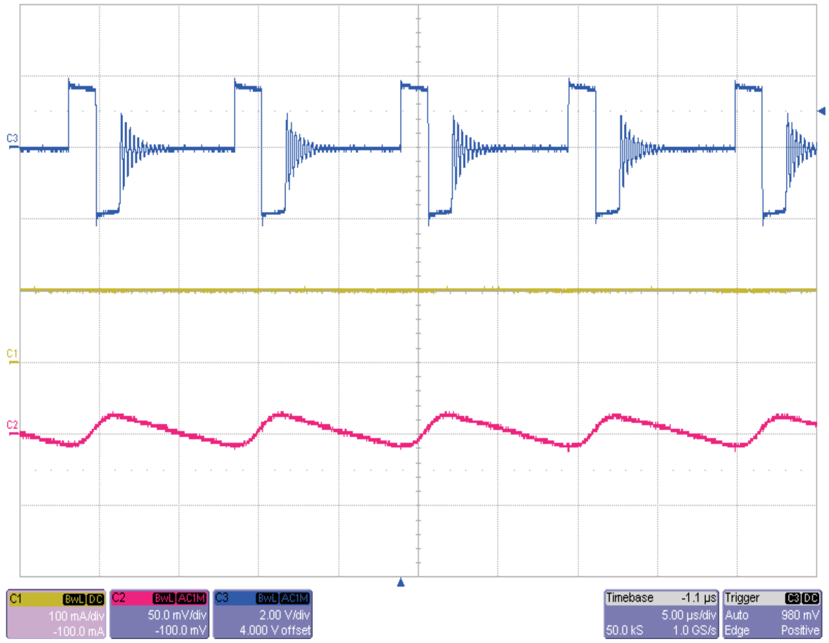

Figure 4. Switch Node (2V/div), Output Current (100mA/div), and Output Ripple (50mV/div) at Light-Load Current

4 Alternate Design Process

To reduce the wider load regulation caused by C_S, the user can remove C_S and connect a large R1B directly to the FB node. In this case, the parallel combination of R1B and R1A, i.e., R1 = R1A||R1B, sets the DC output voltage regulation point. So, for a given R2, set R1B to at least 4 x R1A to minimize the current through it and its resulting error in regulation. Then solve Equation 5 for R1A:

$$R1A = \frac{1}{\frac{1}{R1B} - \frac{1}{R2 \times \left(\frac{V_{OUT}}{1.213V} - 1\right)}} \tag{5}$$

After solving Equation 1 and Equation 3 for C_{ff}, compute two new C_{ff} values using R1B = 4 x R1A, and choose the lower of those two values.

5 Conclusion

This application note provides a quick and easy way to size the additional passive components when using ceramic output capacitors with the TPS6420x family without affecting the load transient and the stability of the system.