Application Report

SLVA334B–October 2009–Revised June 2010

1.8-V - 5.5-V Input, 3.3-V Output, High Efficiency DC/DC Converter

PMP - DC/DC Low-Power Converters

ABSTRACT

This reference design is presented to help application designers and others who are trying to use the MSP430 in a system with an input voltage in the range of 1.8 V to 5.5 V, and who must increase the application run time by making use of the complete battery voltage range while still maintaining high efficiency over the entire battery life.

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1 Introduction

This reference design is for the MSP430 family of microcontroller devices and Stellaris devices, and accounts for the voltage and current requirements as described herein. The MSP430 devices require only a single voltage supply; no sequencing is required. The operating input voltage for this reference design is between 1.8 V to 5.5 V, allowing applications operating from a battery supply to benefit from the complete battery capacity. This design is optimized for a wide input voltage range, a small solution size, and low component count.

For more information and other reference designs, see the Reference section at the end of this document or visit www.ti.com/processorpower.

1.1 Features

- 1.8-V to 5.5-V input voltage range
- Fixed 3.3-V output eliminates need for external voltage-setting resistors
- Capable of driving up to 800 mA when operating in boost mode (TPS63001)
- Capable of driving up to 500 mA when operating in boost mode (TPS63031)
- High efficiency (up to 94%)
- Low quiescent current (less than 50 µA)
- Small QFN packages: 2.5 mm × 2.5 mm (TPS63031) or 3 mm x 3 mm (TPS63001)

2 Requirements

The power requirements for each MSP430 family are listed below. The power given is based on the amount of current the core consumes per megahertz (MHz). The *Analog I_{MAX}* column indicates the amount of current added if the additional functional blocks are used.

For more information and other reference designs, please visit www.ti.com/processorpower.

Table 1. CC43 Family Power Requirements

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz)	ANALOG I_{MAX} (µA)	SEQUENCING ORDER	TIMING DELAY	COMMENTS
		MIN	MAX					
F613x, F513x	A_{VCC}, D_{VCC}[1]	1.8	3.6	250[2]	I_{REF} = 140	n/a	n/a	+Maximum CPU speed of 20 MHz

(1) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

(2) Maximum value for CPU clocked at 20 MHz at 3 V shown. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

Table 2. MSP430x1xx Family Power Requirements[1]

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) [2]	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
x11x1A	V_{CC}	1.8	3.6	350	Comp_A = 60	C11x1: 300 µA/MHz max
F12x	V_{CC}	1.8	3.6	350	Comp_A+ = 60	
F11x2, 12x2	V_{CC}	1.8	3.6	350	ADC10 = 1200, I_{REF} = 400	
F13x, 14x[1]	A_{VCC}, D_{VCC} [3]	1.8	3.6	560	Comp_A = 60, ADC12 = 1600, I_{REF} = 800	F13x, 14x: Comp_A, ADC12 F14x1: Comp_A
F15x, 16x, 161x	A_{VCC}, D_{VCC} [3]	1.8	3.6	600	Comp_A = 60, ADC12 = 1600, I_{REF} = 800, DAC12 = 1500	DAC outputs not loaded; DAC12 currents for a single DAC, max of two DAC12s in device)

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 8-MHz maximum CPU clock speed (ex. Imax_x11x1 = 8 MHz × 350 µA = 2.8 mA). V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated.

Table 3. MSP430x2xx Family Power Requirements[1]

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} [2] (µA/MHz)	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
F20xx	V_{CC}	1.8	3.6	370	Comp_A+ = 60 ADC10 = 1200, ADC10_I_{REF} = 400 SD16_A + I_{REF} = 1700 RefBuffer = 600	20x1: Comp_A+ 20x2: ADC10 20x3: SD16_A
F21x1	V_{CC}	1.8	3.6	410	Comp_A+ = 60	
F21x2	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A+ = 60 ADC10 = 1200, I_{REF} = 400	
F22xx	A_{VCC}, D_{VCC} [3]	1.8	3.6	550	ADC12 = 1200, I_{REF} = 400 OA = 290	22x2: ADC10 22x4: ADC10, 2 OAs OA currents for a single amplifier
F23x0	A_{VCC}, D_{VCC} [3]	1.8	3.6	550	Comp_A + = 60	

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 16 MHz maximum CPU clock speed (ex. Imax_20xx = 16 MHz × 370 µA = 5.90 mA). V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

Table 3. MSP430x2xx Family Power Requirements[(1)] (continued)

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} [(2)] (μA/MHz)	ANALOG I_{MAX} (μA)	COMMENTS
		MIN	MAX			
F23x, 24x[1], 2410	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	445	Comp_A + = 60, ADC12 = 1000, I_{REF} = 700	224x1: Comp_A+ 23x, 24x, 2410: Comp_A+, ADC12
F241x, 261x	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	560	Comp_A + = 60, ADC12 = 1000, I_{REF} = 700 DAC12 = 1500	241x: Comp_A+, ADC12 261x: Comp_A+, ADC12, two DAC12s DAC12 outputs not loaded; DAC12 currents for a single DAC

Table 4. MSP430x4xx Family Power Requirements[(1)]

DEVICE FAMILY	PIN NAME [(2)]	VOLTAGE (V)		CPU I_{MAX} (μA/MHz) [(3)]	ANALOG I_{MAX} (μA)	COMMENTS
		MIN	MAX			
x41x	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A = 60	C41x: 300 μA/MHz max
FW42x	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A = 60 Scan IF = 650	
F42x	A_{VCC}, D_{VCC}	1.8	3.6	500	SD16 + I_{REF} = 1550 Ref Buffer = 600	SD16 current is for a single A/D (three on device)
FE42x[a], 42x2	A_{VCC}, D_{VCC}	1.8	3.6	500	ESP430CE1 = 4900 Ref Buffer = 600	ESP430 current for 4-MHz operation
F43x[1], F44x	A_{VCC}, D_{VCC}	1.8	3.6	560	Comp_A = 60, ADC12 = 1600, I_{REF} = 800	
F42x0	A_{VCC}, D_{VCC}	1.8	3.6	520	SD16_A + I_{REF}=1800 Ref Buffer = 600 DAC12=1500	DAC12 output not loaded
FG42x0	A_{VCC}, D_{VCC}	1.8	3.6	560	SD16_A + I_{REF}=1800 Ref Buffer = 600 DAC12 = 1500, OA = 290	DAC12 output not loaded; OA current for a single amplifier (two OAs in device)
FG43x	A_{VCC}, D_{VCC}	1.8	3.6	570	Comp_A = 60, ADC12 = 1600, I_{REF} = 800, DAC12 = 1500, OA = 490	DAC12 outputs not loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device)
FG46xx	A_{VCC}, D_{VCC}	1.8	3.6	740	Comp_A = 60, ADC12 = 1600, V_{REF} = 800, DAC12 = 1500, OA = 490	DAC12 outputs no loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device)
F47xx	A_{VCC}, D_{VCC}	1.8	3.6	560	Comp_A = 60, SD16_A + I_{REF} = 1700 Ref Buffer = 600	16 MHz max CUP frequency; SD16 current is for a single A/D (four on device)

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated.

(3) 8 MHz maximum CPU clock speed (ex. Imax_x41x = 8 MHz × 350 μA = 2.8 mA). (F47xx max CPU clock = 16 MHz) V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately. LCD current not included.

Table 5. MSP430x5xx Family Power Requirements[1]

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) [2]	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
F54xx	A_{VCC}, D_{VCC} [3]	2.2	3.6	348	ADC12_A = 220, I_{REF} = 190	18 MHz maximum CPU clock speed

(1) Additional 5-mA maximum required when writing/erasing Flash In-system.
(2) 16 MHz maximum at 3-V CPU clock speed. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.
(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

3 Description of Power Solution

Using a buck-boost topology for battery-driven applications enables users to benefit fully from the available charge given from the chemistry.

The TPS630xx devices belong to a fully-integrated family of converters that automatically regulate the preset output voltage over the entire input voltage range of 1.8 V to 5.5 V.

In the case of a fixed 3.3-V output, the converter operates in step-down mode for periods when the input voltage is greater than 3.3 V. Once the input voltage drops below the required 3.3 V, the converter automatically transitions into boost mode without the need of any external control signals or circuitry.

The buck-boost converter architecture is based on a fixed-frequency pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters a Power Save mode to maintain high efficiency over a wide load current range. Power Save mode can be disabled using the PS/SYNC pin, forcing the converter to operate at a fixed switching frequency.

During shutdown, the load is disconnected from the battery.

In cases where budgeting the power of the TPS63001 is required but the overall solution size is critical, the TPS63011 in an available WCSP is recommended.

In applications where overall power consumption is a critical parameter, the MSP430 should operate at a lower input voltage such as 2.2 V; this lower input level allow all blocks to run optimally. In this case, see the adjustable versions of the TPS63000 and TPS63030 buck-boost converter device families.

4 Power Supply Option 1: TPS63031

The TPS63031 supports 500 mA when operating in boost mode (V_{IN} > 2.4V) and greater than 800 mA when working in step-down mode (V_{IN} = 3.6 V to 5.5 V). The overall solution size and the entire device efficiency, as well as the provided power budget, make this converter an ideal fit for portable, battery-driven applications. For a more detailed description of the device characteristics as well as functionality, refer to the device data sheet.

The device can be evaluated by itself using the TPS63030EVM-417 evaluation module. By default, the EVM contains the adjustable device TPS63030. In order to evaluate the 3.3-V version, simply replace device U1 on the EVM board with the TPS63031 device. Furthermore, R1 must be replaced with a 0-Ω resistor; the R2 position remains open.

The following description as well as the results are taken from the TPS63030EVM-417 User Guide.

4.1 Schematic

Figure 1 illustrates the TPS63030EVM-417 schematic.

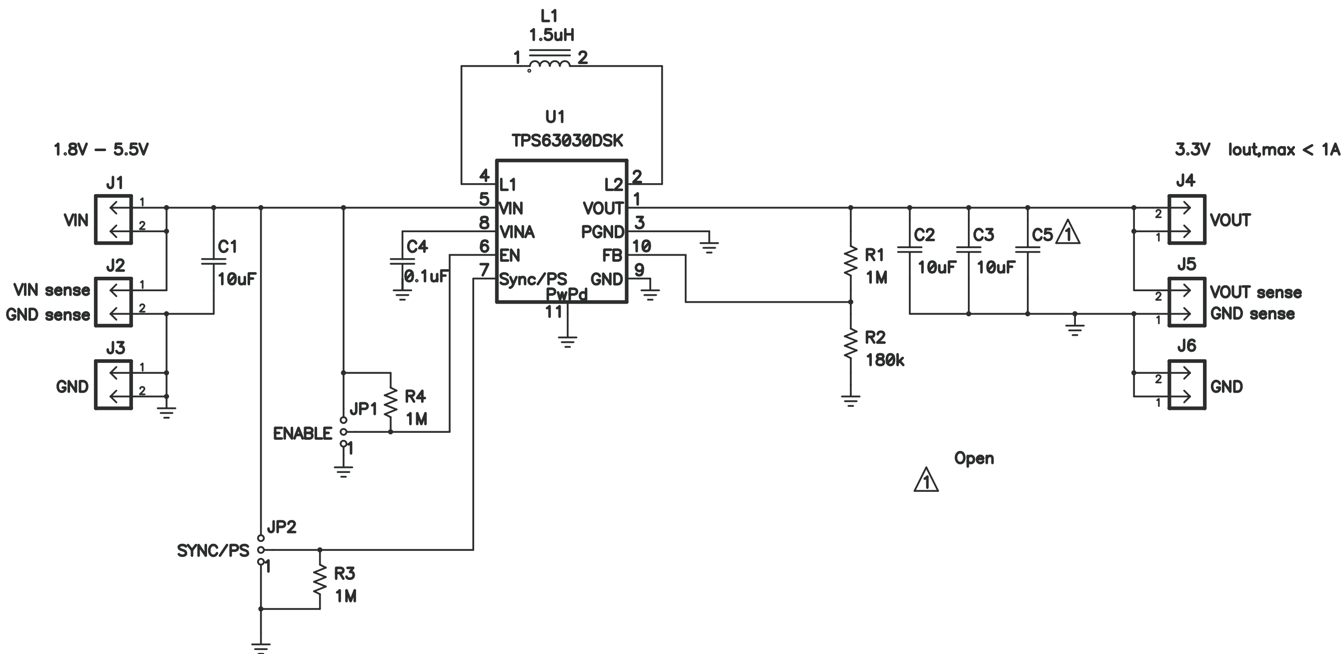

Figure 1. TPS63030EVM-417 Schematic

4.2 List of Materials TPS63030EVM-417

Table 6 shows the bill of materials (BOM) for this design.

Table 6. List of Materials TPS63030EVM-417

QTY	REF DES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
3	C1, C2, C3	10 µF	Capacitor, ceramic, 6.3-V, X7R, 10%	0603	GRM188R60J106ME84D	Murata
1	C4	0.1 µF	Capacitor, ceramic, 6.3-V, X7R, 10%	0603	GRM188R70J104KA01B	Murata
0	C5	Open	Capacitor, ceramic, 6.3-V, X7R, 10%	0603	GRM188R60J106ME84D	Murata
1	L1	1.5 µH	Inductor, SMT, 1.3-A, 110-mΩ	0.118 × 0.118	LPS3015-152MLB	Coilcraft
3	R1, R3, R4	1 MΩ	Resistor, chip, 1/16-W, 1%	0603	Std	Std
1	R2	180 kΩ	Resistor, chip, 1/16-W, 1%	0603	Std	Std
1	U1		IC, dc/dc converter	DSK	TPS63030DSK	TI

4.3 Test Results TPS63031

The following results are based on the TPS63030EVM-417 settings and are included as representative examples of the device functionality and performance.

Figure 2 represents the device behavior during the start-up phase. Figure 3 demonstrates the small output ripple at a typical load of 150 mA.

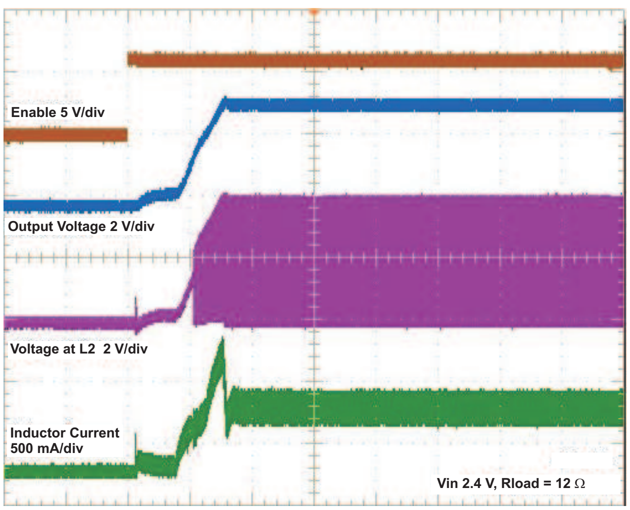

Figure 2. Turn ON into Load, V_{IN} = 2.2 V

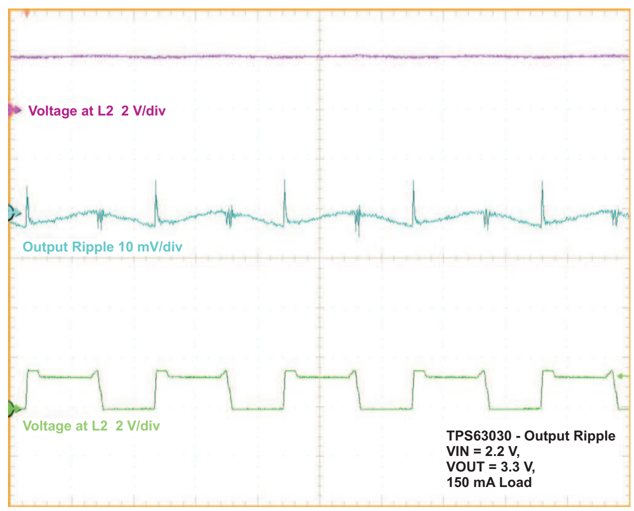

Figure 3. Output Ripple, V_{IN} = 2.2 V

5 Power Supply Option 2: TPS63001

The TPS63001 supports 800 mA when operating in boost mode (V_{IN} > 2.4 V) and greater than 1200 mA when working in step-down mode (V_{IN} = 3.6 V to 5.5 V). The overall solution size and the entire device efficiency, as well as the provided power budget, make the converter an ideal fit for portable, battery-driven applications. For a more detailed description of the device characteristics as well as functionality, refer to the device data sheet.

The device can be evaluated by itself using the TPS63000EVM-148 evaluation module. By default, the EVM contains the TPS63000 adjustable device. In order to evaluate the 3.3-V version, simply replace device U1 on the EVM board with the TPS63001. Furthermore, R1 must be replaced with a 0-Ω resistor; the R2 position remains open.

The following description as well as the results are taken from the TPS63000EVM-148 Users Guide.

5.1 Schematic

Figure 4 shows the reference design schematic.

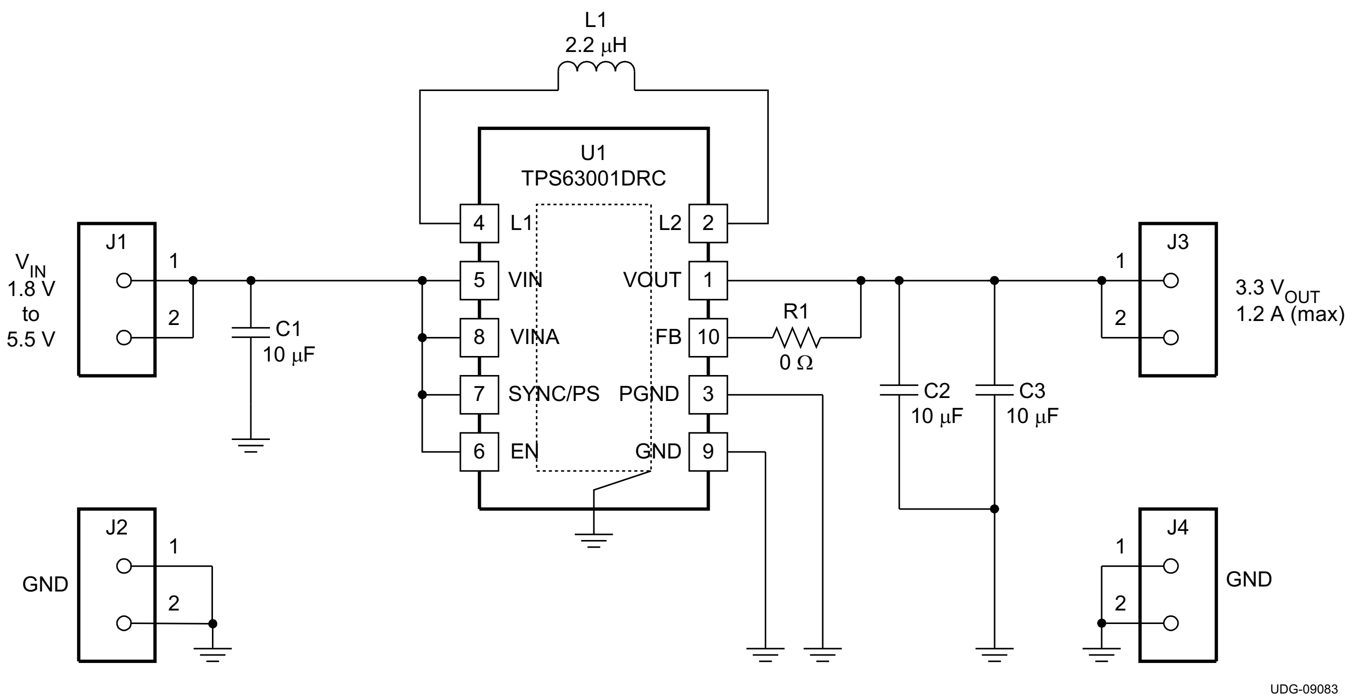

Figure 4. PMP4778 Reference Design Schematic

5.2 List of Materials PMP4778

Table 7 lists the materials for this design.

Table 7. List of Materials PMP4778

REF DES	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2, C3	3	10 µF	Capacitor, ceramic, 6.3V, X5R, 20%	0603	C1608X5R0J106M	TDK
L1	1	2.2 µH	Inductor, SMT, 1.5A, 110 mOhm	0.116" x 0.116"	LPS3015-222ML	Coilcraft
R1	1	0 Ω	Resistor, chip, 1/16W, 1%	0603	Std	Std
U1	1		IC, buck-boost converter	QFN-10	TPS63001DRC	TI

5.3 Test Results TPS63001

The input and output startup waveforms are shown in Figure 5 through Figure 10. The output ripple voltages are shown in Figure 11 through Figure 13. Figure 14 through Figure 16 shows the transient responses. The switching node waveforms are shown in Figure 17 through Figure 19. The efficiency versus the output current is shown in Figure 20.

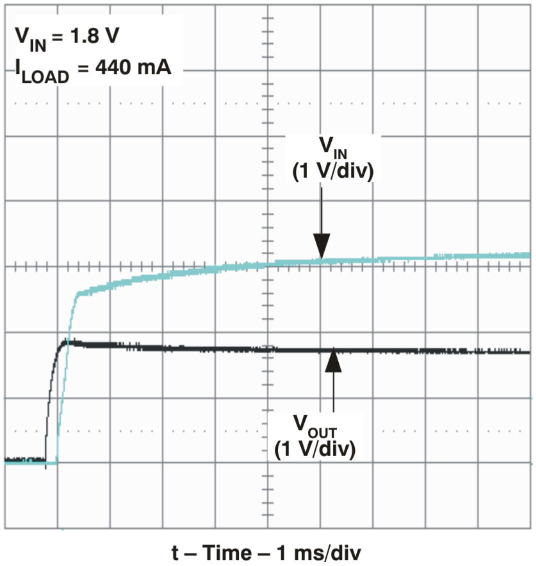

Figure 5. Startup

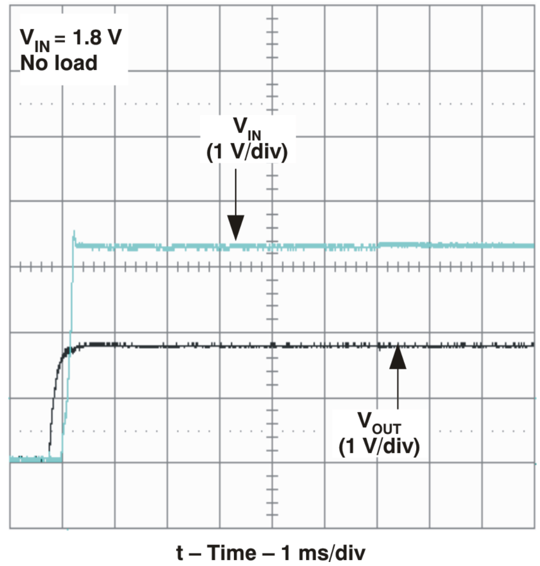

Figure 6. Startup

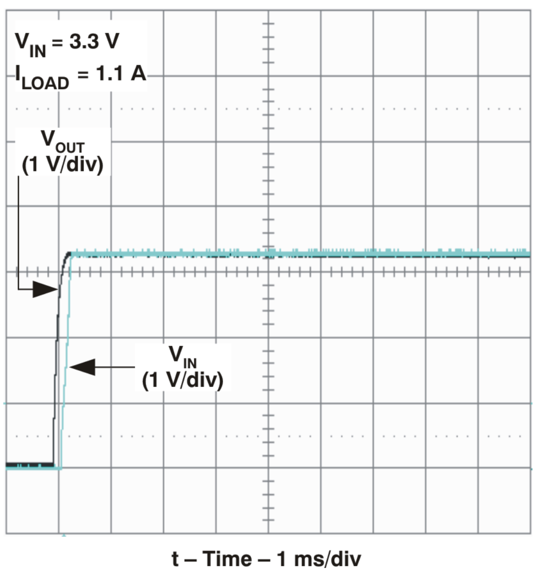

Figure 7. Startup

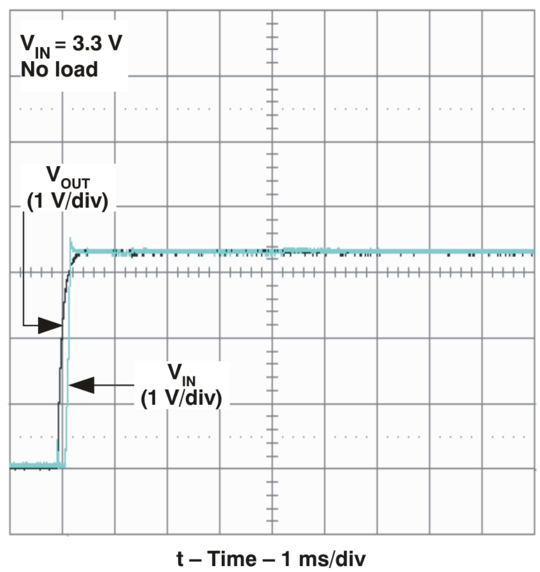

Figure 8. Startup

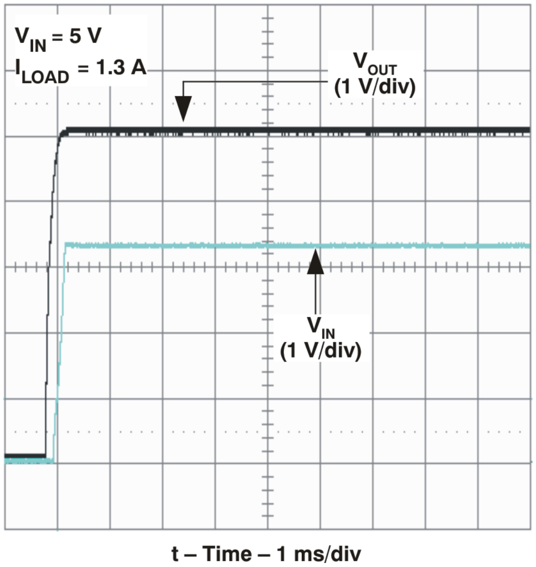

Figure 9. Startup

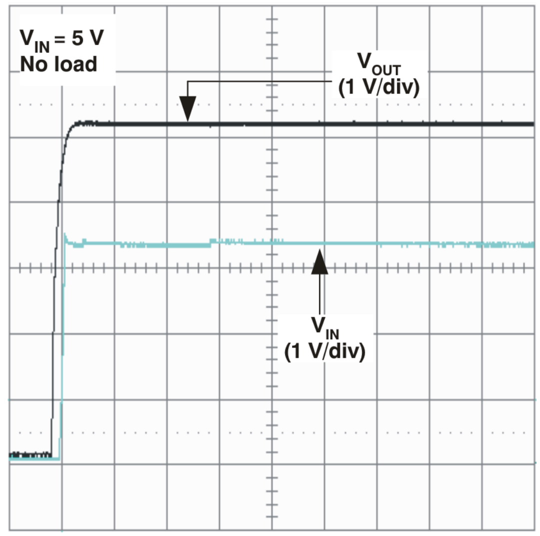

Figure 10. Startup

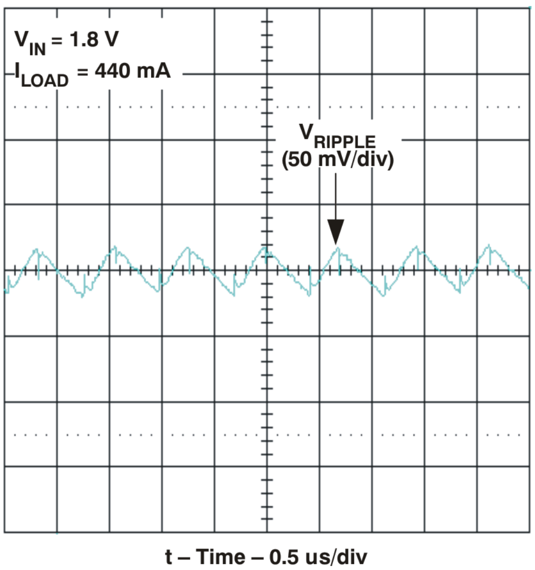

Figure 11. Output Ripple Voltage

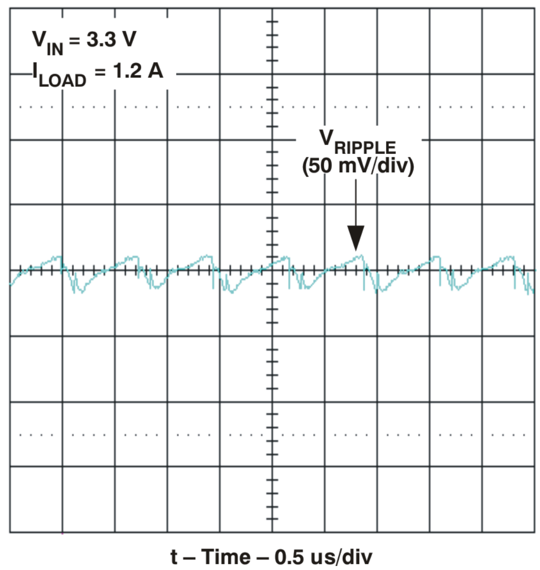

Figure 12. Output Ripple Voltage

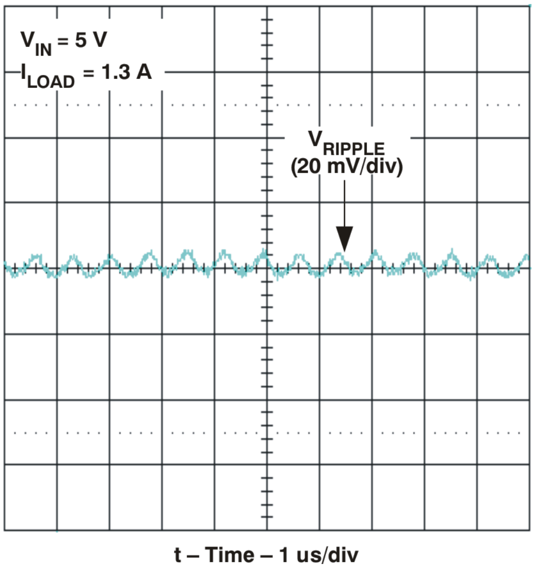

Figure 13. Output Ripple Voltage

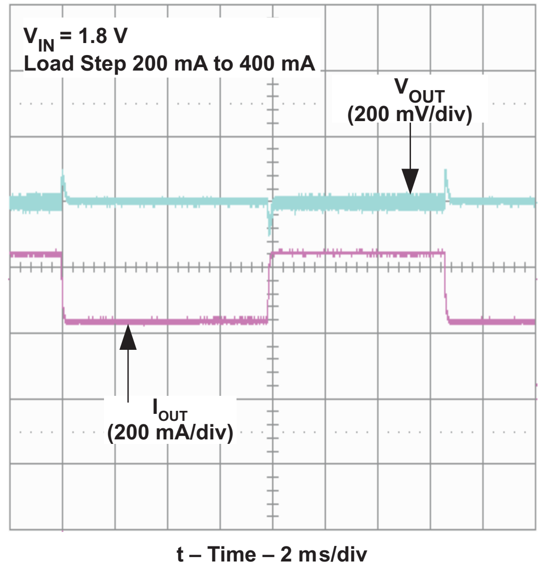

Figure 14. Load Transient

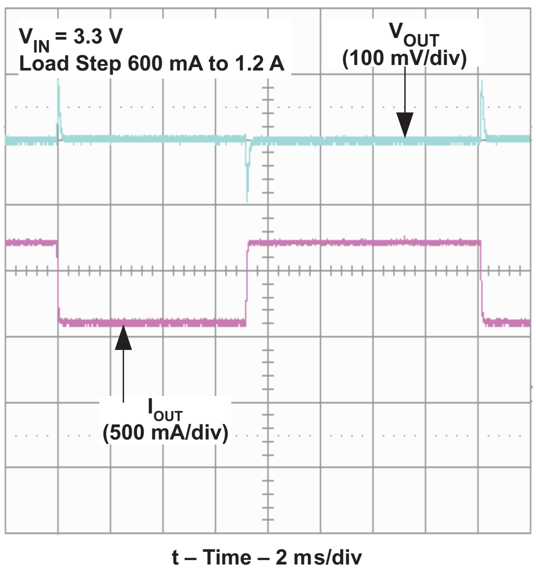

Figure 15. Load Transient

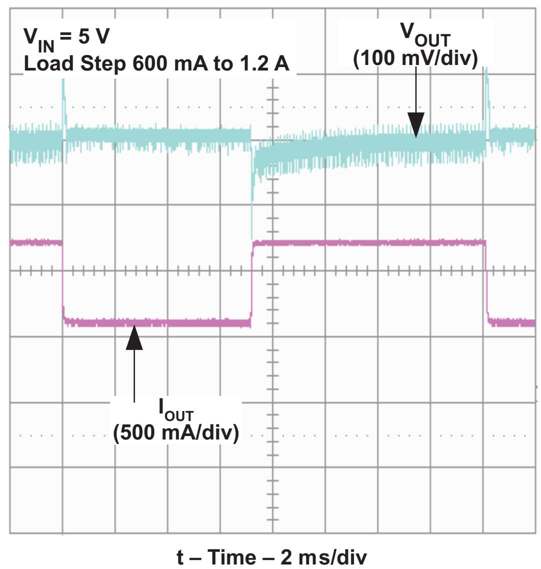

Figure 16. Load Transient

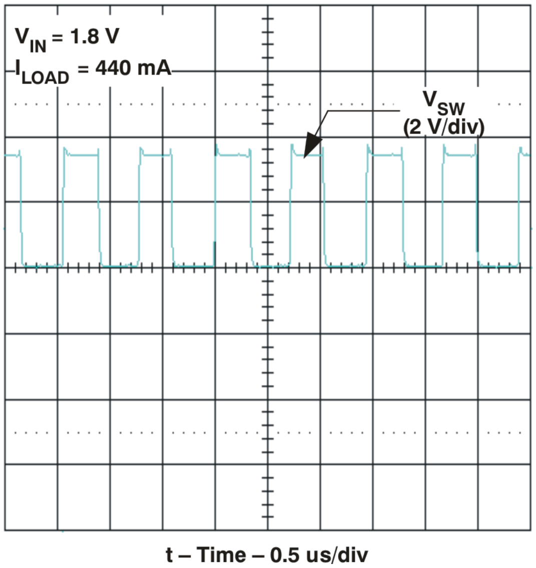

Figure 17. Switching Node Waveform

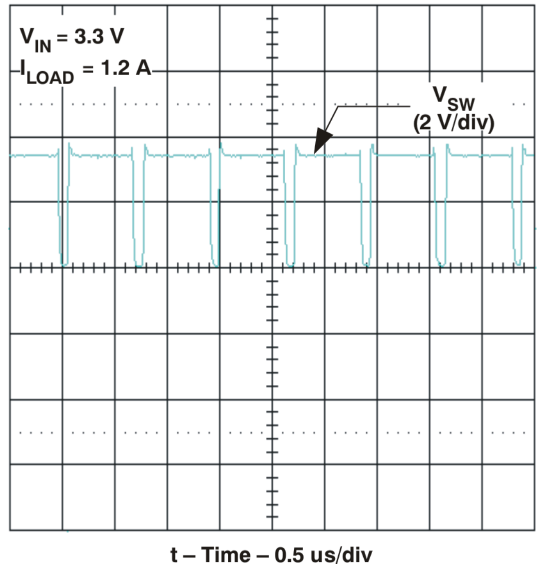

Figure 18. Switching Node Waveform

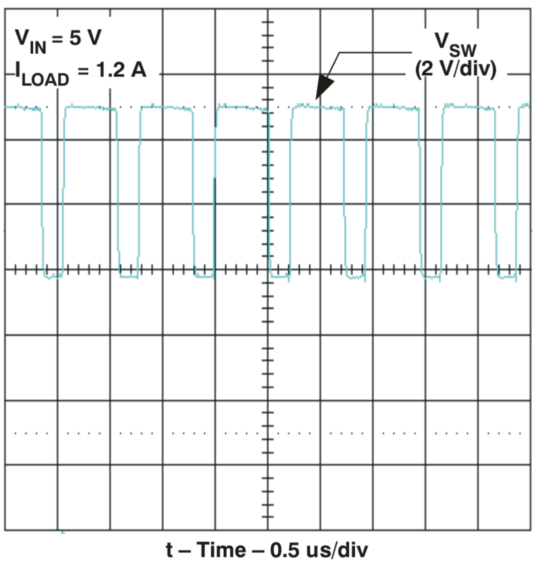

Figure 19. Switching Node Waveform

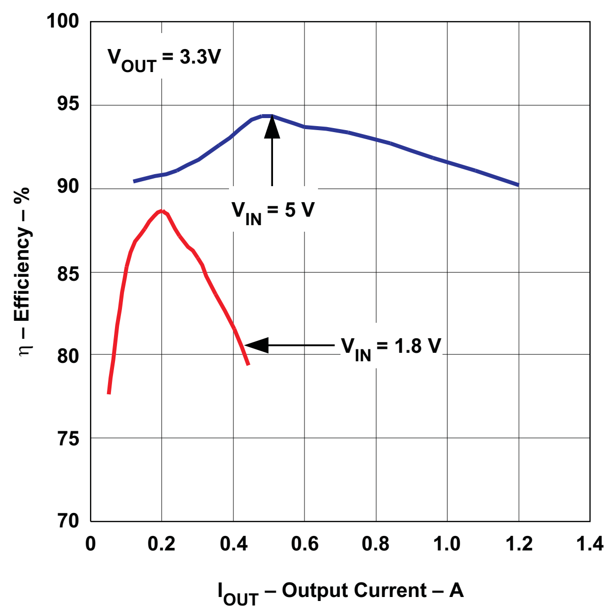

Figure 20. Efficiency vs Output Current

6 Inductor Selection

Table 8 lists several inductor series from different suppliers that have been used with TPS6303x converters. Table 9 lists several inductor series from different suppliers that have been used with TPS6300x converters.

Table 8. TPS6303x List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	LP3015
	EPL3010
Murata	LQH3NP
Taiyo Yuden	NR3015

Table 9. TPS6300x List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	LP3015
	LP4012
Murata	LQH3NP
Taiyo Yuden	NR3015
TDK	VLF3215
	VLF4012

For a more detailed description of how to configure the inductor based on the individual needs, refer to the related device data sheets.

7 Capacitor Selection

7.1 Input Capacitor

A minimum effective value of 4.7 μF for the input capacitor is recommended to improve transient behavior of the regulator and electromagnetic interference (EMI) behavior of the total power-supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the device is recommended.

*7.2 Bypass Capacitor **(TPS6303x only)***

To make sure that the internal control circuits are supplied with a stable, low-noise supply voltage, a capacitor can be connected between VIN_A and GND. Using a ceramic capacitor with a value of 0.1 μF is recommended. The value of this capacitor should not be higher than 0.22 μF.

7.3 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the device. If for any reason the application requires the use of large capacitors that cannot be placed close to the device, using a smaller ceramic capacitor in parallel to the larger one is recommended. This smaller capacitor should be placed as close as possible to the VOUT and PGND pins of the device.

To get an estimate of the recommended minimum output capacitance, use Equation 1.

$$C_{OUT} = 5 \times L \times \frac{\mu F}{\mu H} \tag{1}$$

A capacitor with a value in the range of the calculated minimum should be used. This capacitor is required to maintain control loop stability. There are no additional requirements regarding minimum equivalent series resistance (ESR). There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

8 General Layout Considerations

NOTE: The following guidelines are applicable to general power designs as such, and are not specific to the power solution outlined in this document.

As for all switching power supplies, the layout is an important step in the design. A proper function of the device demands careful attention to printed circuit board (PCB) layout. It is essential to take good care of the board layout to achieve specified performance. In case the layout is not well done, the regulator could show poor line and/or load regulation and stability issues, as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the primary current paths. The input capacitor, inductor, and output capacitor should be placed physically as close as possible to the device terminals. The most important reason (apart from keeping the noise at a low level) is the fail-safe operation of the solution. Any distance added between the components will increase the value of the parasitics, which could result in greater voltage levels within the device than the chip actually would be able to withstand. In other words, keeping the external components connected closely will prevent the device from failures through parasitics.

Connect the GND terminal of the device to the thermal pad land of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the thermal pad land (star point) underneath the device. Keep the common path to the GND terminal, which returns the small signal components and the high current of the output capacitors, as short as possible to avoid ground noise.

9 References

Table 10 lists several related documents.

Table 10. Related Documents

DEVICE NUMBER	TI LITERATURE NUMBER	DESCRIPTION
PRODUCT DATA SHEETS		
TPS63001	SLVS520	High Efficiency Single Inductor Buck-Boost Converter with 1.8-A Switch
TPS63031	SLVS696	High Efficiency Single Inductor Buck-Boost Converter with 1-A Switch
EVM USER GUIDES		
TPS63000EVM-148	SLVU156	Using the TPS63000EVM
TPS63030EVM-417	SLVU275	Using the TPS63030EVM

IMPORTANT NOTICE