Application Report
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Reduced Size, Double-Sided Layout for High-Current DC/DC Converters

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ABSTRACT

The use of a double-sided topology for a space optimized, *Clam Shell* layout for step-down DC/DC converters has previously been evaluated.(1) The results showed that this technique was successful for small, SOT23 regulators delivering up to 2.5-A output current. Using both sides of the PCB gives a space-efficient solution with no disadvantage in electrical or thermal performance. In this application report, this technique is investigated to see if it can be successfully employed for higher output current regulators such as the TPS56C215 device.

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Trademarks

1 Critical Steps in DC/DC Layout

A summary of the key layout steps, in order of priority is:

1. Place the input capacitors as close as possible to the IC with wide, short traces to the VIN and PGND pins. Every millimeter makes a difference! Minimize the area of the loop from CIN to VIN and PGND back to CIN.
2. Place the inductor, as close as possible to the SW pin of the device, keeping the switch-node area as small as possible.
3. Place output capacitors from the inductor, returning to the PGND close to the input capacitor. Again, minimize the area of the loop from the SW pin through the inductor to COUT and back to PGND.
4. As before, CIN, COUT and PGND are connected together to form a return path for the switching currents. This should be connected to the system GND at a single point.

For more details on optimization of DC/DC converter layout, see Tim Hegarty's three-part series on DC/DC layout published in EDN(2), and Chris Glaser's paper in the TI Analog Applications Journal.(3)

2 Double-Sided Layout

It is generally a good practice to avoid layer changes and hence vias in the power loops described in the previous steps. This is because vias add parasitic inductance and can lead to ringing and add to EMI. However, the parasitic inductance of vias is more or less critical at different places around the loops, as seen in Figure 1. For example vias directly in series with the inductor should add to the inductance and not cause parasitic issues. This suggests that, with care, the IC and other components might be placed on the opposite side to the PCB to the inductor. With the IC and capacitors directly under the inductor footprint, the total PCB area used by the DC/DC converter circuit is minimized.

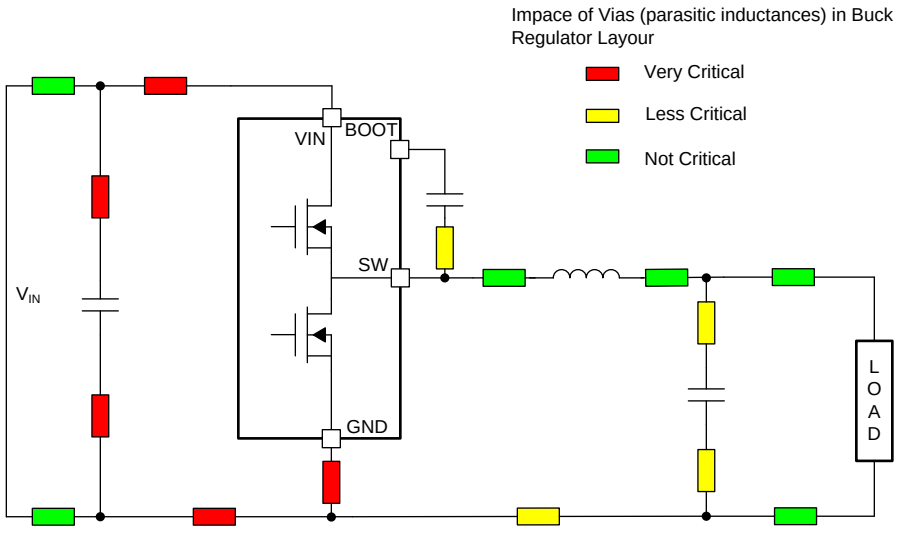

Figure 1. Effect of Parasitic Inductances at Different Locations in DC/DC Power Loops

3 Testing the Theory

In order to test the double-sided layout ideas, a board with three versions of an identical electrical circuit was created, with three different layouts. The circuit uses the TPS56C215RNNR 12-A buck regulator in a 3.5 mm × 3.5 mm VQFN package. The application converts from 12 V to 1.2 V at 8 A. Figure 2 illustrates the schematic.

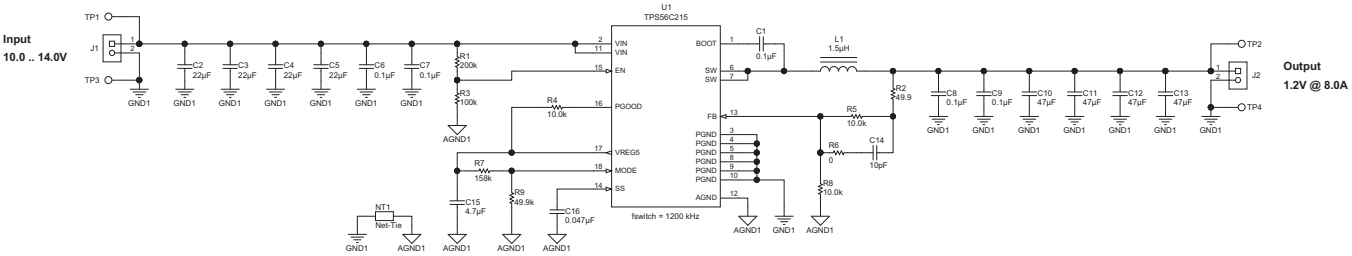

Figure 2. TPS56C215RNNR 12 V to 1.2 V at 8 A

- Input capacitors:
  - TDK C2012X5R1V226M125AC
  - CAP, CERM, 22 µF, 35 V, ±20%, X5R, 0805
  - Approximately 5 µF at 12 VDC (–80%)
- Output capacitors:
  - Murata GRM21BR61A476ME15
  - 47 µF, 10 V, ±20%, X5R, 0805
- Inductor:
  - Wurth Elektronik 744323150
  - Shielded Drum Core, 1.5 µH, 12 A, 6.6 mΩ

The three copies of the circuit were laid out on a four-layer PCB, with the internal layers used mainly for ground plane plus some tracking to connectors. The first layout (see Figure 3) uses an entirely single-sided layout and measures 23 mm × 23 mm, with an area of 529 mm^2. In the second layout (see Figure 4), the regulator IC and input capacitors are moved to the bottom of the board. The second layout measures 23 mm × 13 mm with an area of 299 mm^2. The third layout (see Figure 5) has the IC only moved to the bottom of the board, with inductor, input capacitors, and output capacitors on the top. This also measures 23 mm × 13 mm with an area of 299 mm^2. In both the double-sided layouts, the components on each side are directly above and below each other so the area used is the total area looking through the board.

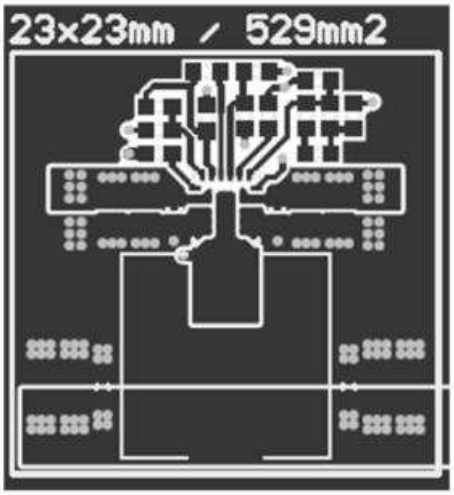

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Figure 3. Layout 1 - Single Sided

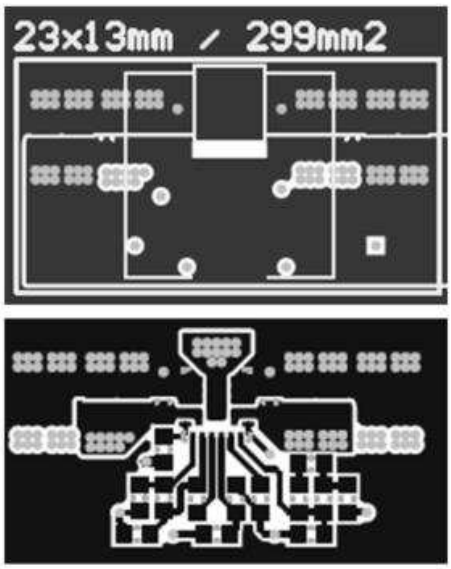

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Figure 4. Layout 2 - Inductor and Output Capacitors (Top), IC and Input Capacitors (Bottom)

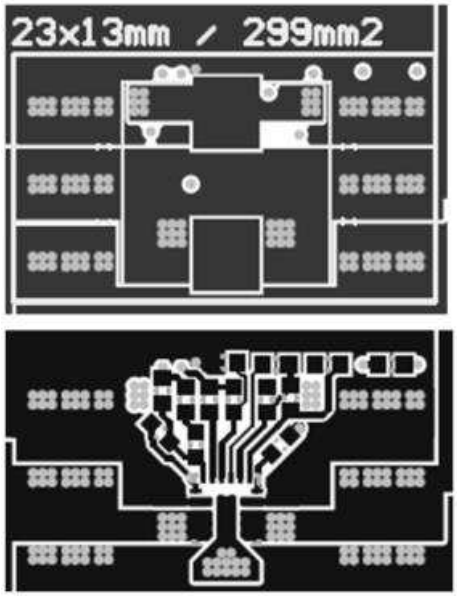

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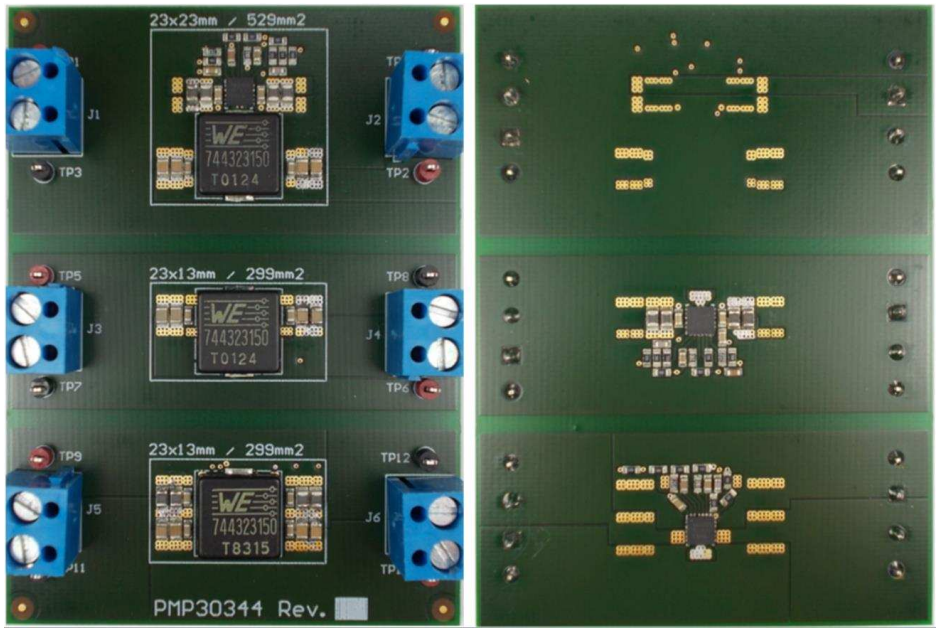
Figure 5. Layout 3 - Inductor, Output and Input Capacitors (Top), IC (Bottom)

Figure 6 shows the PCB used for testing the layouts.



Top Side Bottom Side

Figure 6. Test PCB

3.1 Results - Output Ripple

Figure 7, Figure 8, and Figure 9 show the output ripple measured directly across the output capacitors using a coaxial lead.(4)

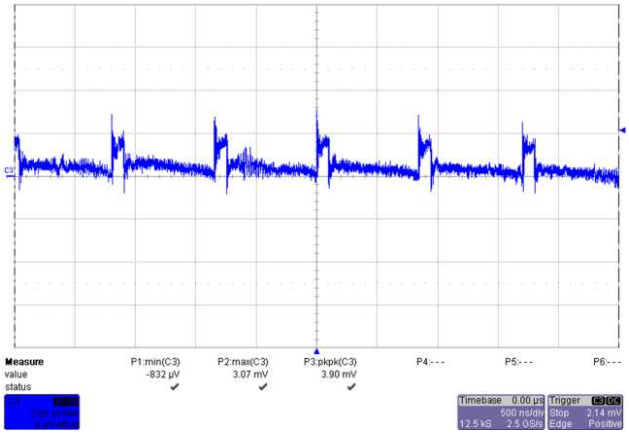


Figure 7. Layout 1 - Output Ripple, 2 mV/div, 12 V to 1.2 V at 8 A

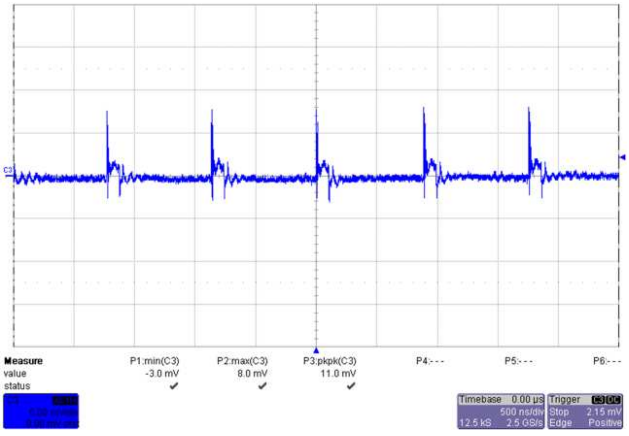


Figure 8. Layout 2 - Output Ripple, 5 mV/div, 12 V to 1.2 V at 8 A

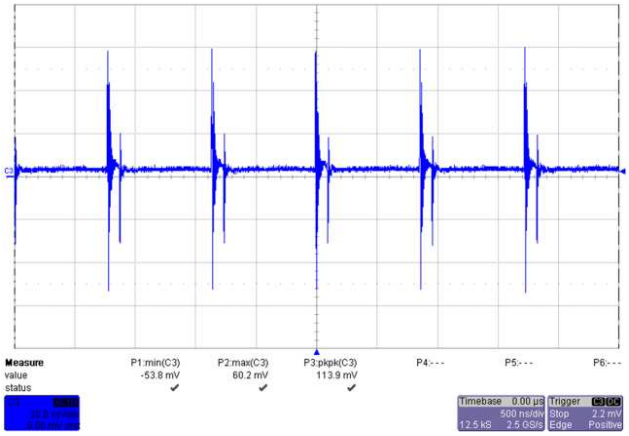


Figure 9. Layout 3 - Output Ripple, 20 mV/div, 12 V to 2.5 V at 8 A

Single-sided layout 1 has the best output ripple at only 4 mVpp. For Layout 2, the ripple increases slightly to 11 mVpp. This appears to be due to switching edge pick up. Layout 3 is the worst with > 100 mVpp made up of significant switching edge pick up with associated switch node ringing.

3.2 Results – Input Ripple

Figure 10, Figure 11, and Figure 12 show the input ripple as measured directly across the input capacitors of each circuit using the same coaxial method. The triangular waveform generated as the capacitor filters the input current is the same in each layout at approximately 100 mVpp. The differences between the three layouts are due to pick up of the switching edges. The single-sided layout 1 exhibits moderate switching edge pick up, leading to 234 mVpp ripple. In layout 2, there is less pick up and the ripple is reduced to 147 mVpp. Finally, layout 3 shows the worst ripple at approximately 500 mVpp with very significant pick up of the switching edge and associated ringing.

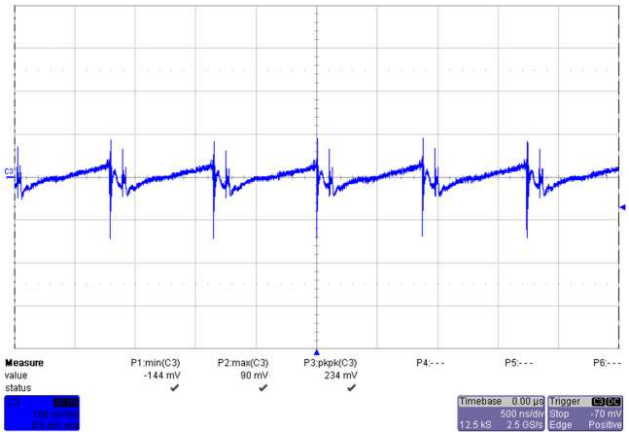


Figure 10. Layout 1 - Input Ripple, 100 mV/div, 12 V to 2.5 V at 8 A

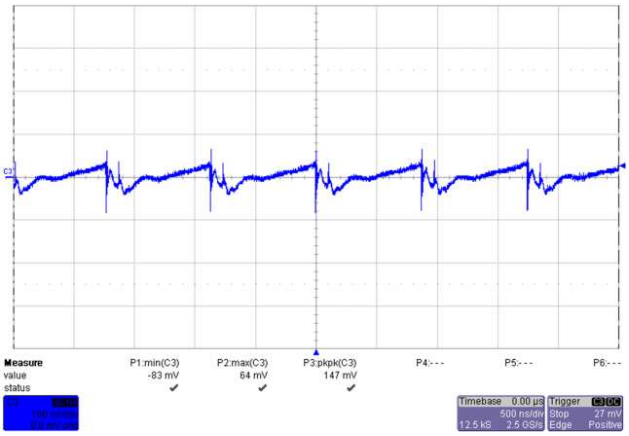


Figure 11. Layout 2 - Input Ripple, 100 mV/div, 12 V to 2.5 V at 8 A

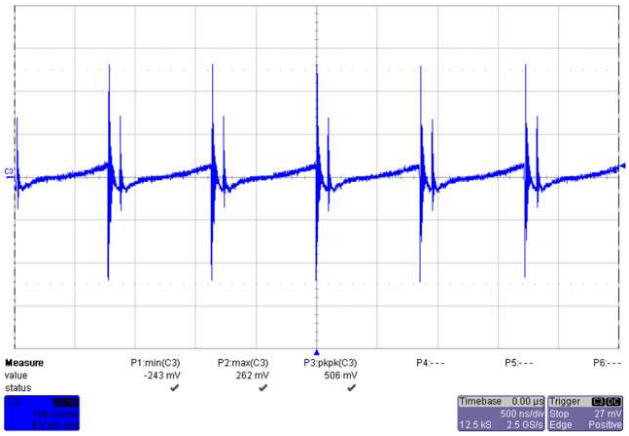


Figure 12. Layout 3 - Input Ripple, 100 mV/div, 12 V to 2.5 V at 8 A

3.3 Results – Switch Node

The switch node plots for layout 1 and layout 2 show very little or no overshoot and ringing, approximately 400 mV and approximately 1 V, respectively. However, the overshoot in layout 3 is approximately 5 V. Figure 9 and Figure 12 clearly show the results of this ringing coupling to the input and output waveforms.

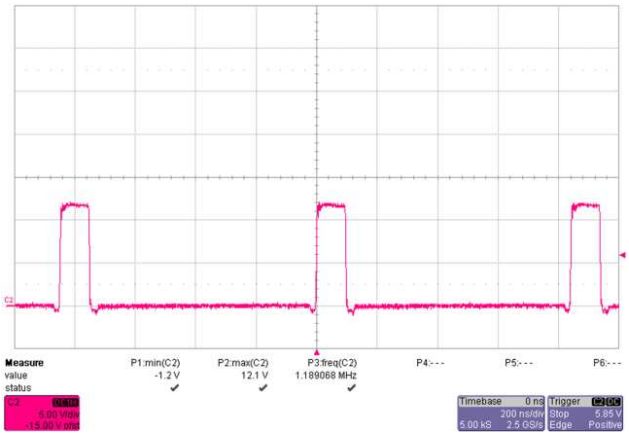


Figure 13. Switch Node Waveform, Layout 1

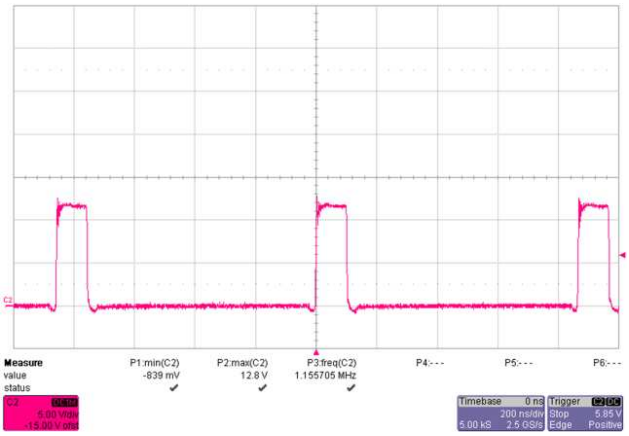


Figure 14. Switch Node Waveform, Layout 2

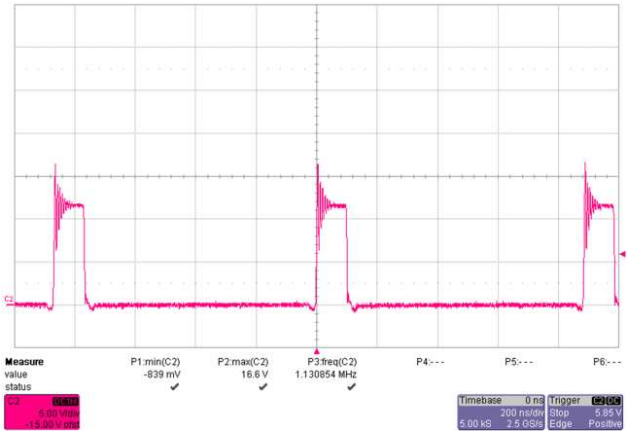


Figure 15. Switch Node Waveform, Layout 3

3.4 Results – Thermal Performance

Thermal images of each circuit were recorded with the converter running at 8-A continuous output, and left for a period of time to come to thermal equilibrium. The top-side plot was recorded from above while the bottom was recorded from below, looking up.

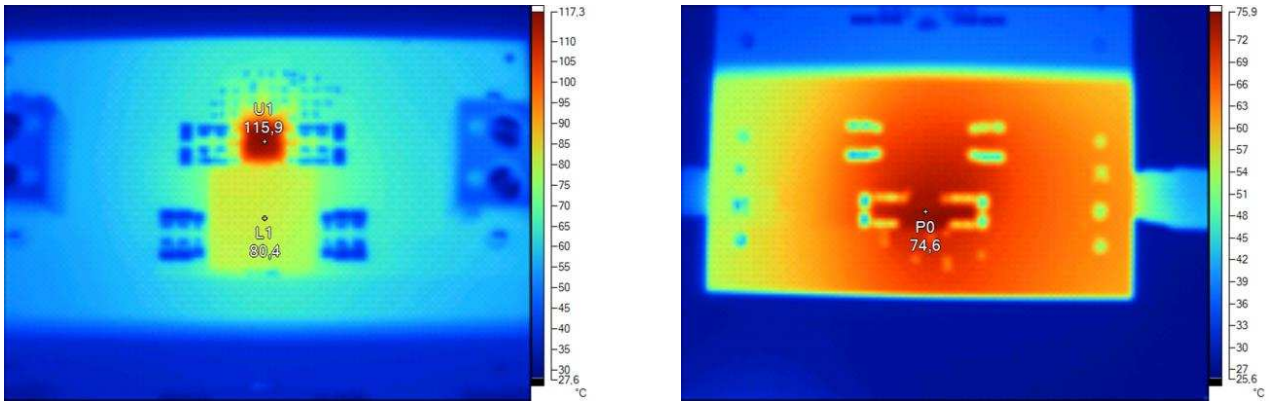


Figure 16. Layout 1 - Single Sided, All Components Top Side

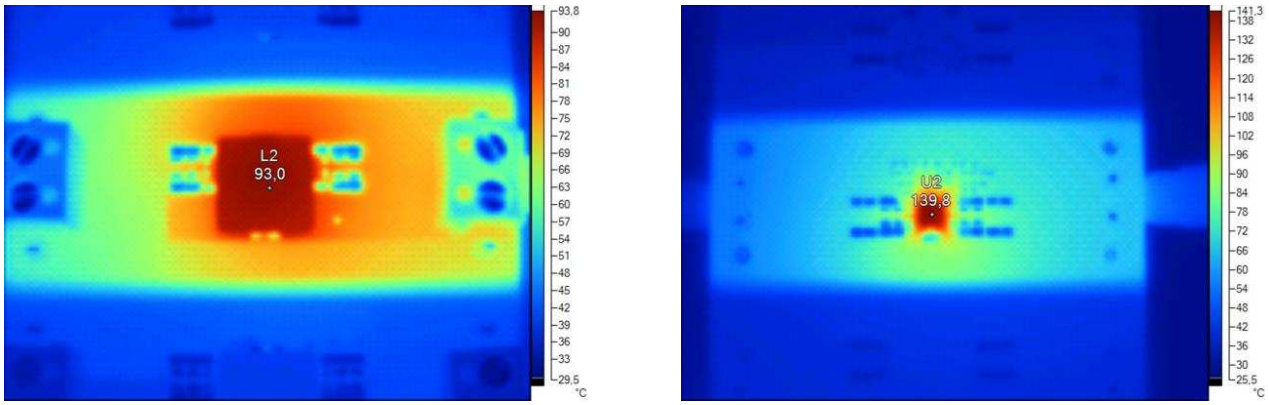


Figure 17. Layout 2 – Double Sided, Inductor Top Side, IC Bottom Side

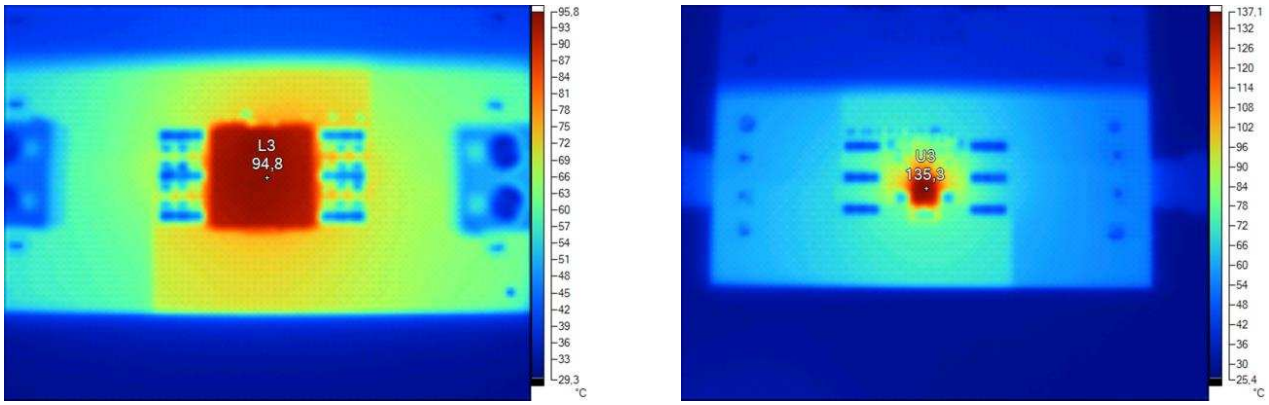


Figure 18. Layout 3 – Double Sided, Inductor Top Side, IC Bottom Side

The two double-sided layouts run somewhat hotter than the single-sided layout. This is almost certainly due to the hotspot created where the inductor sits directly over the IC. Using Ψ_{JT} junction-to-top characterization parameter of 0.4°C/W, it is estimated that the junction temperature is approximately 1°C higher than the case temperature, and still some way inside the 150°C maximum recommended operating junction temperature. It would be interesting to see the effect of inverting the double-sided layouts to see if convection from the regulator IC reduced the temperature.

4 Conclusions

Table 1 shows a summary of results for this investigation. Clearly an optimized, single-sided layout with all components on the top side gives the best electrical and thermal results. Where space is limited, a double-sided layout with the output capacitors and inductor on one side of the board and the IC and input capacitors on the other could be a good option, especially where the peak to average current ratio is higher, and the total heat generated less.

Table 1. Summary of Results

	Area	Output Ripple Peak to Peak	Input Ripple Peak to Peak	Switch Node Overshoot	IC Temperature, Inductor Temperature
Layout 1: Single-sided layout	529 mm^2	4 mV	234 mV	0.4 V	115.9°C, 74.6°C
Layout 2: Inductor and output capacitors on top side IC and input capacitors on bottom	299 mm^2	11 mV	147 mV	1.0 V	139.8°C, 93.0°C
Layout 3: Inductor, output and input capacitors on top side IC on bottom	299 mm^2	114 mV	506 mV	5.0 V	135.3°C, 94.8°C

Analyzing these three layouts and the position of the vias compared to Figure 1 gives the further insight into the results achieved. Figure 19 shows no critical vias. Figure 20 shows that the vias in the ground return from the output capacitors are not ideal though not very critical. Figure 21 shows that there are multiple critical vias around both the input and output capacitors on layout 3.

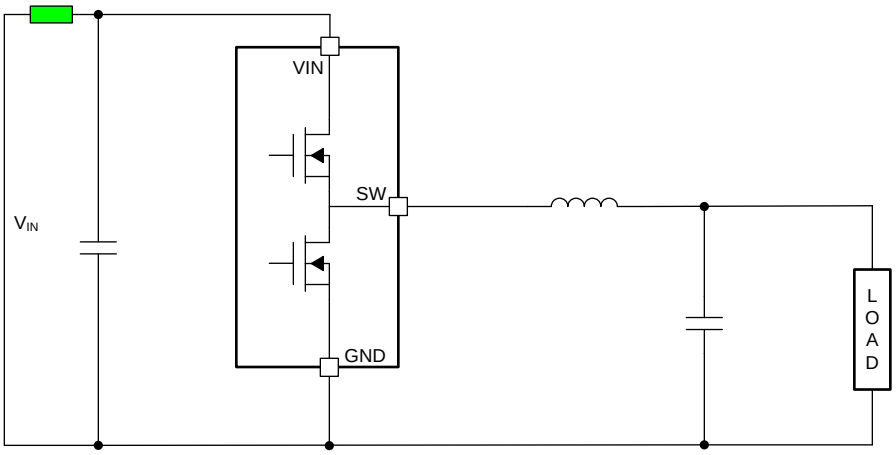


Figure 19. Layout 1 - no Critical Vias

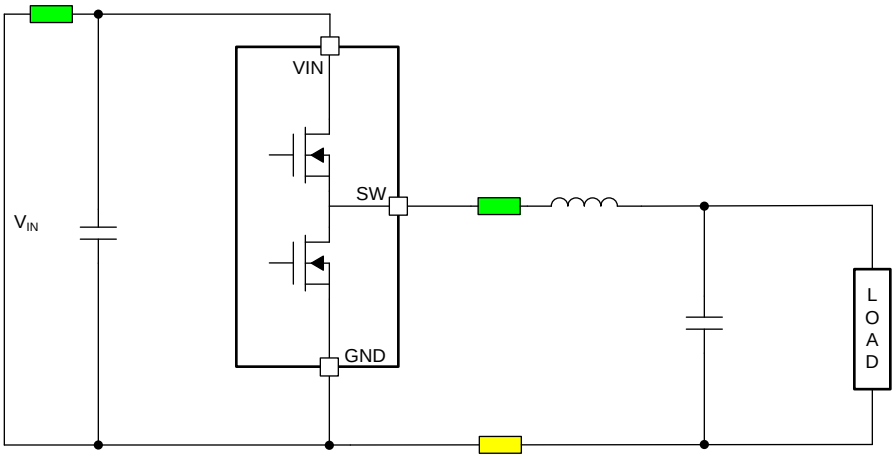


Figure 20. Layout 2 – Critical Vias in Ground Return From Output Capacitors

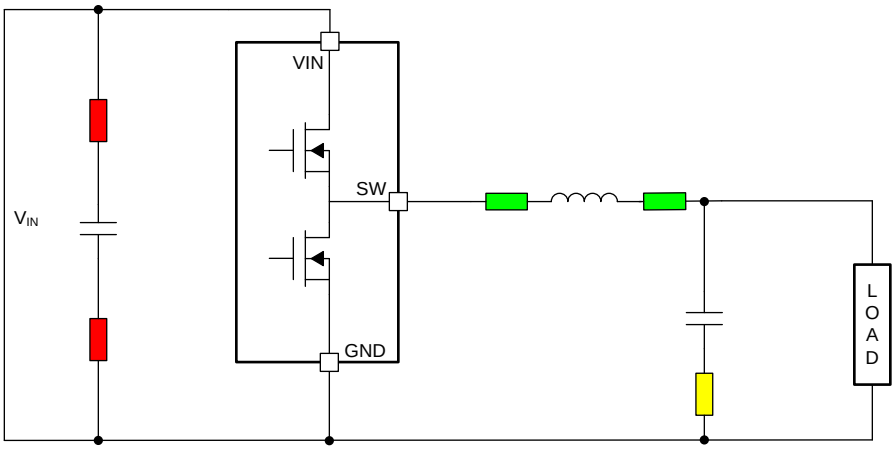


Figure 21. Layout 3 – Critical Vias on Both Input and Output Capacitor Connections

This analysis suggests that a double-sided layout with the inductor on the top side and the IC, input and output capacitors on the bottom might be a better solution as Figure 22 shows.

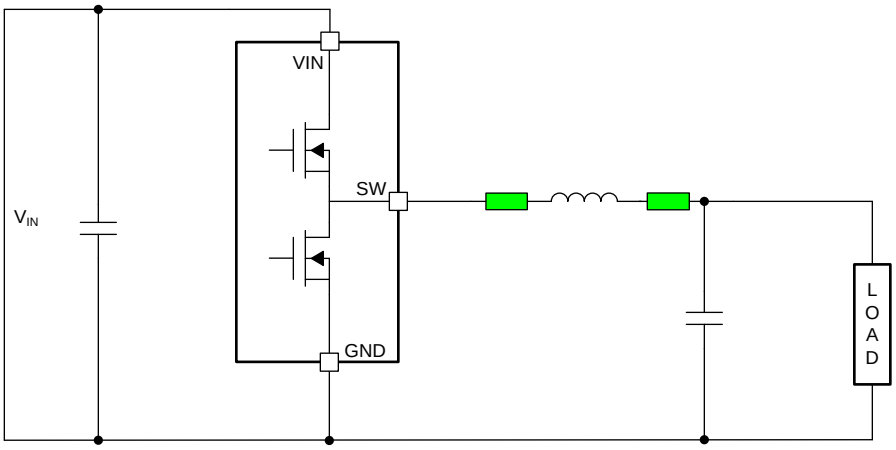


Figure 22. Possible Improved Layout With Vias to Inductor Only

The parasitic inductances in the power loops are not the only factors to consider. High current, large voltage swings can couple to other parts of the circuit close by and also between layers. As the layouts become smaller and denser, the switch node and inductor connection can be very close to the input or output capacitors (or both), and couple noise across. This may go some way to explain the larger spikes on the input ripple waveform for the single-sided layout 1 compared to the double-sided layout 2. In layout 1, the input voltage track an input capacitors are in close proximity to the switch node and inductor, whereas on layout 2 they are on the opposite side of the board. Again this may suggest that suggests that a double-sided layout with the inductor on the top side and the IC, input and output capacitors on the bottom might be a better solution as Figure 22 shows.

5 References

1. Texas Instruments, *Space Optimized, "Clam Shell" Layout for Step-Down DC/DC Converters Application Report*
2. *DC/DC converter PCB layout*, Part 1,2&3. Timothy Hegarty -June 15, 2015.
3. Texas Instruments, *Five steps to a great PCB layout for a step-down converter Application Report*
4. Texas Instruments, *How You Measure Ripple Can Make You or Break You* TI Powerhouse Blog

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