Application Brief

TPS25981 - Making Power Dense

Mahavir Jain, Kunal Goel

Introduction

With the ever-increasing power demand in server applications, power designers need to squeeze more functionality into the design to differentiate it. Some of the limiting factors to this are Board area, components power capability and height. Using components that can deliver higher power levels in small form factors, helps in achieving higher power density. As package size shrinks, die size shrinks and overall power density deteriorates, the expected thermal performance degrades rapidly, unless package innovations are prioritized to improve thermal performance (getting the heat out faster) and reducing power losses (generating less heat).

Server power systems operate at wide ambient temperature range up to 70C. Components such as hot-swap controllers or eFuses experience high ambient temperature like 70C. Therefore, power design engineers get concerned about the thermal performance of these devices, when high currents are packed in the small packages.

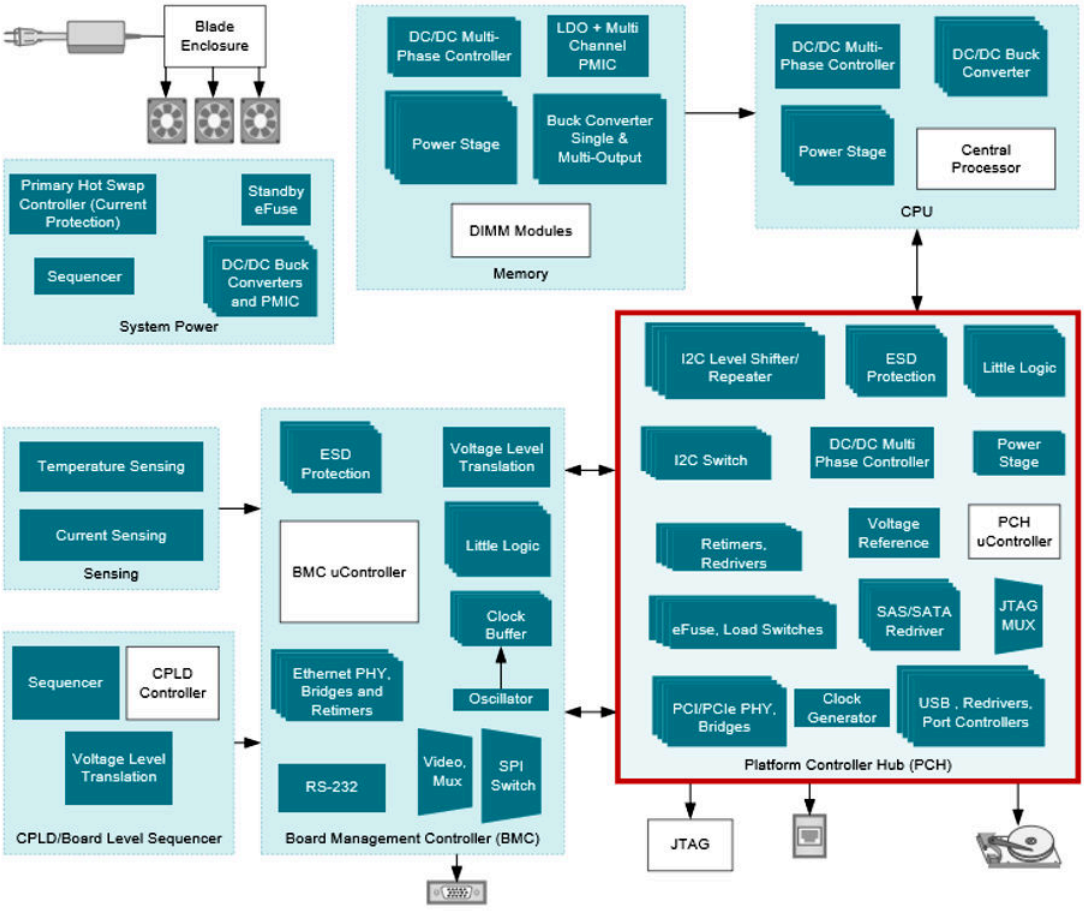

Figure 1. Enterprise Server

TPS25981

TPS25981 comes in unique Hotrod QFN package. A regular wire-bond QFN with an exposed power/thermal pad is a popular package from power-density point of view. They usually have high electrical resistance and hence higher heat generation.

In TI's TPS25981 HotRod interconnect, with silicon die flipped directly on a lead frame, it can dramatically reduce the interconnect parasitic and lower the dissipated power. While HotRod technology can lower power dissipation, it can result in less optimal exposed lead frame patterns when compared to a bond-wire QFN with a large exposed pad.

To address this, in TPS25981 multiple Cu pillars are placed on IN and OUT traces such that, the highest power dissipating pins are converted into long trace lines. This provides larger area for heat dissipation on both IN and OUT pins and placing multiple vias on PCB, directly under the IN and OUT trace can help dissipate the heat through bottom of the board.

Figure 2. TPS2595 in Standard QFN with Bond-wires to Electrically Connect to the Die

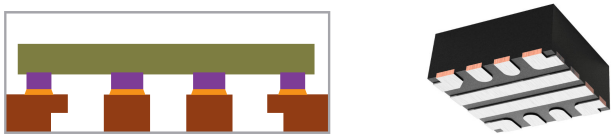

Figure 3. TPS25981 in HotRod Package with Copper Pillars and Flip-chip Interconnect Between the Leadframe and Die

TPS2595 was the first generation 4A eFuse device from TI which provided power path protection in very small WSON 2mm x 2mm package. The evolution of packaging technology from TPS2595 allows for fitting a bigger die in the same package size allowing TPS25981 to support up to 10A without compromising on thermal performance. TPS25981 offers all protection features present in TPS2595 in same package size with an increased continuous current rating of 10A.

Benchmarking TPS25981 with Competition

For comparison, a best in class power density device in 2mm x 2mm package from competition is considered. At room temperature both TPS25981 and competitor device were operated at 12V, 10A on their respective EVMs. Competition is a 13.5V load switch with typical RDSON of 12.8 mΩ at VIN=12V in DFN 8 pin 2mm x 2mm package.

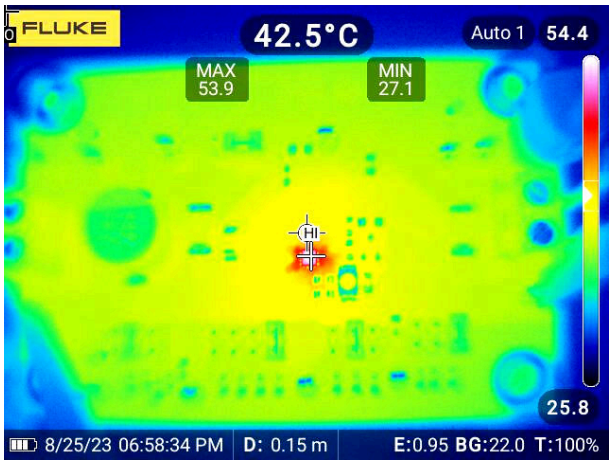

Figure 4. TPS25981EVM, VIN=12 V, IOUT=10 A

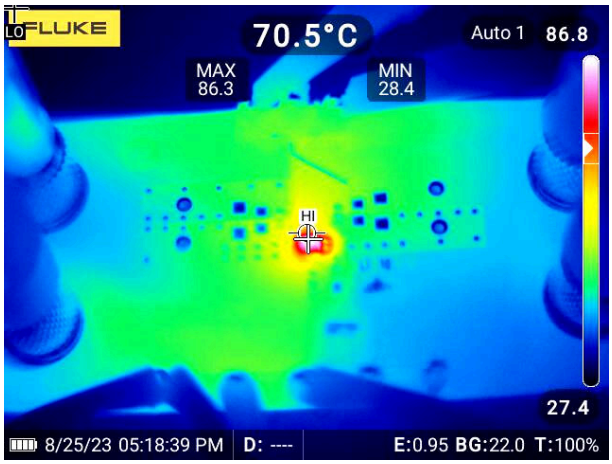

Figure 5. Competition Device EVM, VIN=12 V, IOUT=10 A

It is found that competitor device case temperature rises 30C more than the TPS25981 device. As junction temperature is proportional to case temperature that means competitor device FET junction temperature is higher than TPS25981 device. This proves that TPS25981 thermal performance is superior as compared to competitor device. Though TPS25981 supports higher voltage up to 16V, reduced typical RDSON of 6mohm compared to competition helps in improved thermal performance.

As TPS25981 device is designed for server applications operating at high ambient temperatures, the previous test was repeated but with ambient of 70C by keeping EVMs inside thermal chamber. It is found that competitor device is not able to support 10A current at 70C. It is getting shut down due to thermal protection inside device meaning internal FET is reaching SOA limits. TPS25981 device is able to support 10A at 70C.

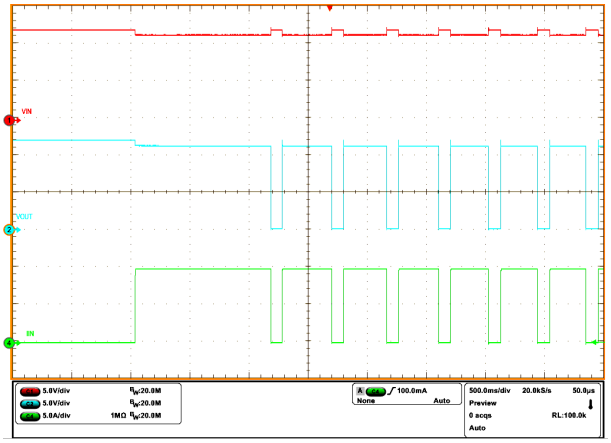

Figure 6. Competition Device Shutting Down at 10 A, 70 C

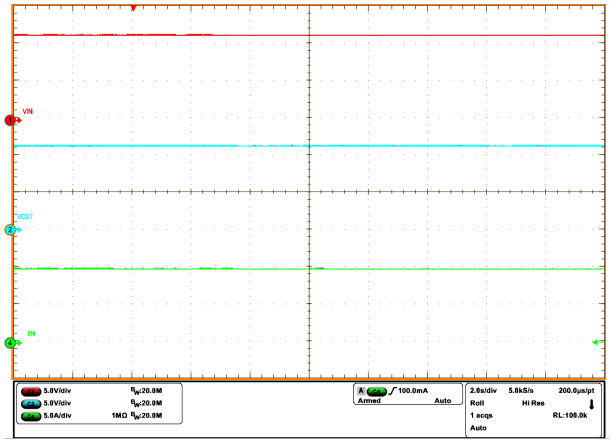

Figure 7. TPS25981 Running Continuously at 10 A, 70 C

Conclusion

TPS25981 by the virtue of package innovation is able to achieve best in class power density. It solves the challenges and is well adapted for the high current and low RDSON trends in end-equipment like enterprise servers, dense optical port protection and industrial PCs. Table 1 highlight key differences between TPS25981, TPS2595 and competition device from power density perspective.

Table 1. Differences Between TPS25981,TPS2595, and Competition Device

	TPS2595	TPS25981	Competition Device
Input voltage	2.7 V - 18 V	2.7 V - 16 V	0.5V - 13.5 V
Maximum current at 70C	4 A	10 A	9.5 A
RDSON at 12V(typ)	34 mΩ	6 mΩ	12.8 mΩ
Max Current/Area at 70C	1 A/mm^2	2.5 A/mm^2	2.37 A/mm^2
Package	QFN, 2mm x 2mm	QFN-HR, 2mm x 2mm	DFN, 2mm x 2mm

References

- Understanding the Trade-offs and Technologies to Increase Power Density
- How eFuse Ensures Integrated FET Operation in Safe Operating Area
- TPS25981x 2.7 V – 16 V, 10-A, 6-mΩ eFuse with Transient Overcurrent Blanking Timer
- TPS2595xx 2.7 V to 18 V, 4-A, 34-mΩ eFuse With Fast Overvoltage Protection
- How to Achieve Higher Power Density and Better Thermal Performance in PSUs

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265