*Application Note*

# *D-CAP2™ and D-CAP3™ Loop Analysis With Hybrid Output Capacitors*

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**ABSTRACT**

D-CAP2™ and D-CAP3™ converters achieve low ESR ceramic output capacitors through ripple injection circuit. But many designers still prefer to use an electrolytic capacitor or polymer to obtain high capacitance for better ripple and transient performance. This application note discusses the loop stability of the D-CAP2 and D-CAP3 converter using different types of capacitors, especially electrolytic capacitors or polymers. This application note introduces the calculation of the zero and pole with a hybrid output capacitor network based on D-CAP2 and D-CAP3 stage small signal model. The theoretical calculation results are verified by bench loop test. An analysis of the loop stability for the D-CAP2 and D-CAP3 converter with a hybrid output capacitors network is provided. This application note also provides two application design examples based on TPS51386EVM, a 4.5-V to 24-V input, 8-A synchronous buck converter with adaptive on-time D-CAP3 control mode.

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## Trademarks



## 1 Introduction

In general, MLCCs have low capacitance and small ESR, and electrolytic capacitors have high capacitance but large ESR. Many designers use MLCCs and electrolytic capacitors in parallel to obtain high capacitance for better ripple and transient performance. However, the electrolytic capacitors have a large ESR, and in DC/DC converter small-signal model, the hybrid output capacitors introduce additional zeros and poles in the loop. And when the ESR of electrolytic capacitors is too large, the zeros and poles are pushed into the bandwidth and have a direct effect on the stability of the loop. This application note calculates the zero and pole of hybrid output capacitor and analyzes the loop stability.

## 2 Zcap Calculation of Hybrid Capacitors

Two different types of capacitors in parallel are common in application designs, so two types of capacitors in parallel are the main focus of discussion here. The simplified equivalent circuit of hybrid output capacitors is shown in Figure 2-1. C1 is the MLCC with small ESR and the C2 is the capacitors with a high capacitance and large ESR, such as electrolytic capacitor or polymer capacitors.

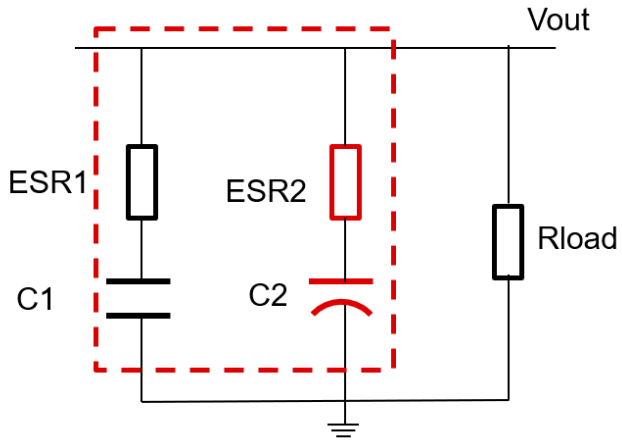


**Figure 2-1. The Simplified Equivalent Circuit of Hybrid Output Capacitors**

The impedance of a hybrid output capacitor network can be given by Equation 1.

$$Z_{cap}(s) = \left(r_1 + \frac{1}{sC_2}\right) // \left(r_1 + \frac{1}{sC_2}\right) = \frac{(1 + sC_1r_1)(1 + sC_2r_2)}{s(C_1 + C_2)\left[1 + s(r_1 + r_2)\frac{C_1C_2}{C_1 + C_2}\right]} \quad (1)$$

Where, r1 is the ESR of C1; r2 is the ESR of C2

The results show that the hybrid capacitor network introduces an additional zero $\omega_{z\_C2}$ and pole $\omega_{p\_C2}$ compared to just one type of MLCC capacitor network.

$$\omega_{z\_C2} = \frac{1}{C_2r_2} \quad \omega_{p\_C2} = \frac{1}{(r_1 + r_2)\frac{C_1C_2}{C_1 + C_2}} \quad (2)$$

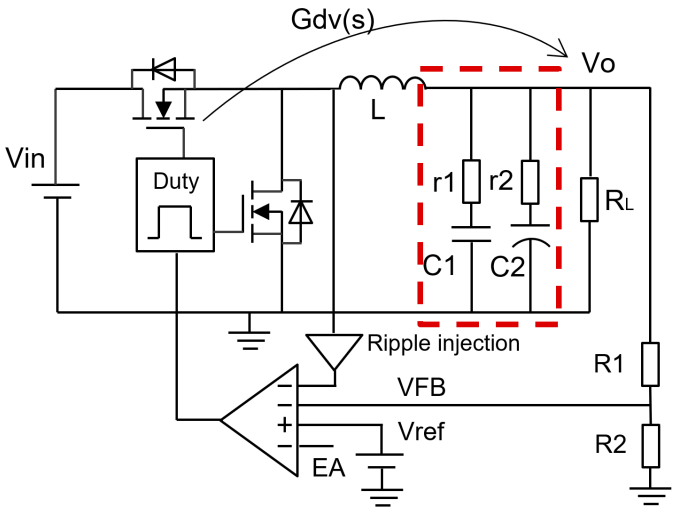


**Figure 2-2. D-CAP3™ Functional Block Diagram With Hybrid Capacitor Network**

The only difference between the D-CAP2 and D-CAP3 converter is that the D-CAP3 has an error amplifier (EA) to eliminate static errors of output voltage, while the D-CAP2 converter does not have an EA block. Since the EA does not affect the loop analysis with the hybrid capacitor network, the D-CAP3 is used as an example in the next analysis. Figure 2-2 shows a simplified DCAP3 functional block diagram with hybrid capacitor network. The *D-CAP2™ Frequency Response Model based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection* application note, builds on the D-CAP2/3 small-signal model and provides the transfer function from duty to Vout with an MLCC capacitor network. Using a hybrid capacitor network for output in combination with Equation 1 yields the Gdv(s) in Equation 3.

$$\mathrm{Gdv(s)} = \frac{\mathrm{Vin} \times \left(1 + \frac{S}{\omega_{z\_C1}}\right)\left(1 + \frac{S}{\omega_{z\_C2}}\right)}{\left[1 + 2\sigma\frac{S}{\omega_0} + \left(\frac{S}{\omega_0}\right)^2\right]\left(1 + \frac{S}{\omega_{p\_C2}}\right)} \tag{3}$$

where

$$\sigma = \frac{\sqrt{L / C_0} + R_L(r_L + r_c)\sqrt{L / C_0}}{2R_L\sqrt{1 + r_L / R_L}} \tag{4}$$

$C_0$ is total output capacitance

$\omega_0$ is the double pole:

$$\omega_0 = \sqrt{\frac{1}{L(C_1 + C_2)}} \tag{5}$$

$\omega_{z\_C1}$ is the zero generated by C1:

$$\omega_{z\_C1} = \frac{1}{C_1 r_1} \tag{6}$$

$\omega_{z\_C2}$ is the zero generated by C2:

$$\omega_{z\_C2} = \frac{1}{C_2 r_2} \tag{7}$$

$\omega_{p\_C2}$ is the pole generated by the hybrid capacitors network:

$$\omega_{p\_C2} = \frac{1}{(r_1 + r_2)\frac{C_1 C_2}{C_1 + C_2}} \tag{8}$$

## 3 Experimental Verification

To verify the calculation results in the previous section, the TPS51386EVM is used as an example to perform bench loop test and the Bode plot is used for loop analysis. The TPS51386 is a 4.5-V to 24-V input, 8-A synchronous buck converter with adaptive on-time D-CAP3 control mode.

The experimental conditions are: $V_{in}$= 20 V, $V_o$= 3.3 V, $I_{out}$= 8 A, $f_{sw}$= 600 kHz, L= 1.5 µH, C1= 22 µF×4, total effective capacitance of ≅59 µF, with total 0.5-mΩ ESR and C2= 220 µF, with 20-mΩ ESR. The zero of internal ripple injection of TPS51386 $\omega_{RI}$ is approximately 45 kHz.

Equation 5 through Equation 8 are used to calculated the zero and pole, the result is $\omega_0$= 7.8 kHz, $\omega_{z\_C1}$= 5.40 MHz, $\omega_{z\_C2}$= 36.2 kHz, and $\omega_{p\_C2}$= 167 kHz.

Figure 3-1 shows the Bode plot test results of the EVM board with the position of turning frequency marked. The result of the amplitude gain curve shows that the conversion frequency corresponds to the calculated frequency of zero and pole. This plot also verifies that the previous calculation is accurate.

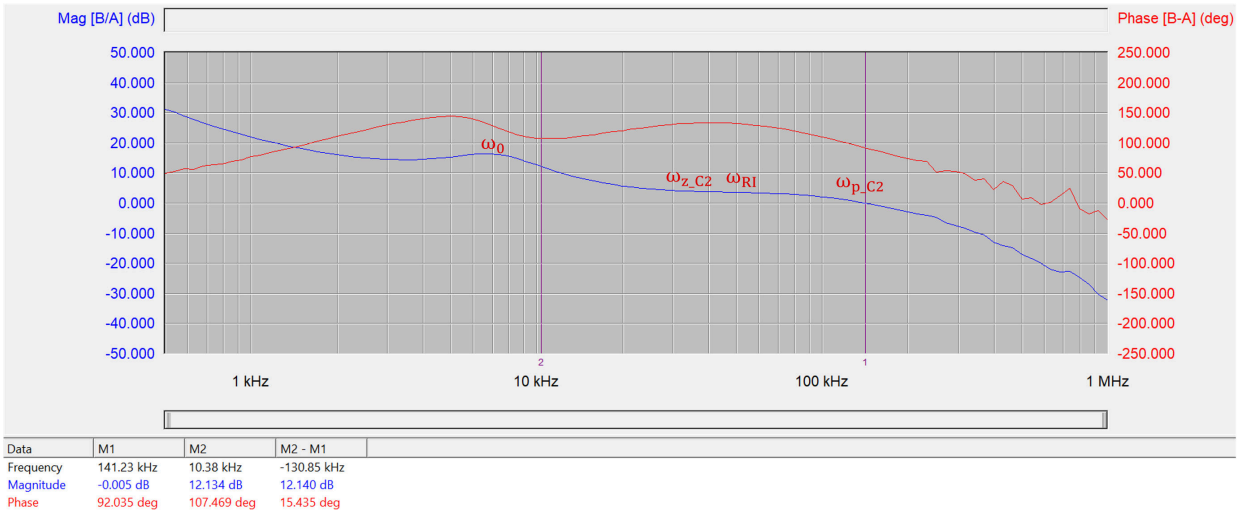


**Figure 3-1. The Bode Plot Results of Bench Loop Test**

## 4 Loop Stability Analysis With Hybrid Output Capacitor Network

The loop of the D-CAP3 converter is stable with the MLCC output capacitors network and the bandwidth is less than 1/3 switching frequency to make sure the loop is stable. When the hybrid output capacitor network is used, the loop stability is discussed in more detail.

Equation 9 shows the zero frequency minus the pole frequency, C1<C2, r1<r2, the result is less than 0. So the zero frequency is always less than the pole frequency, which can simplify the subsequent analysis and calculations. Since the ESR and capacitance of the MLCC is low, the zero $\omega_{z\_C1}$ is typically located at a very high frequency and does not affect loop stability. The discussion focuses on the zero $\omega_{z\_C2}$ and pole $\omega_{p\_C2,}$, which is divided into two cases.

$$\omega_{z\_C2} - \omega_{p\_C2} = \frac{1}{C_2 r_2} - \frac{1}{(r_1 + r_2)\frac{C_1 C_2}{C_1 + C_2}} = \frac{C_1 r_1 - C_2 r_2}{(r_1 + r_2) C_1 C_2 r_2} < 0 \quad (9)$$

**Case 1:** When the ESR and capacitance of C2 is not large enough, and the zero $\omega_{z\_C2}$ produced by the C2 is greater than $\omega_{cross}$ and outside the bandwidth as shown in Figure 4-1. The $\omega_{z\_C2}$ and $\omega_{p\_C2}$ have little effect on the bandwidth and the bandwidth is less than 1/3×fsw.

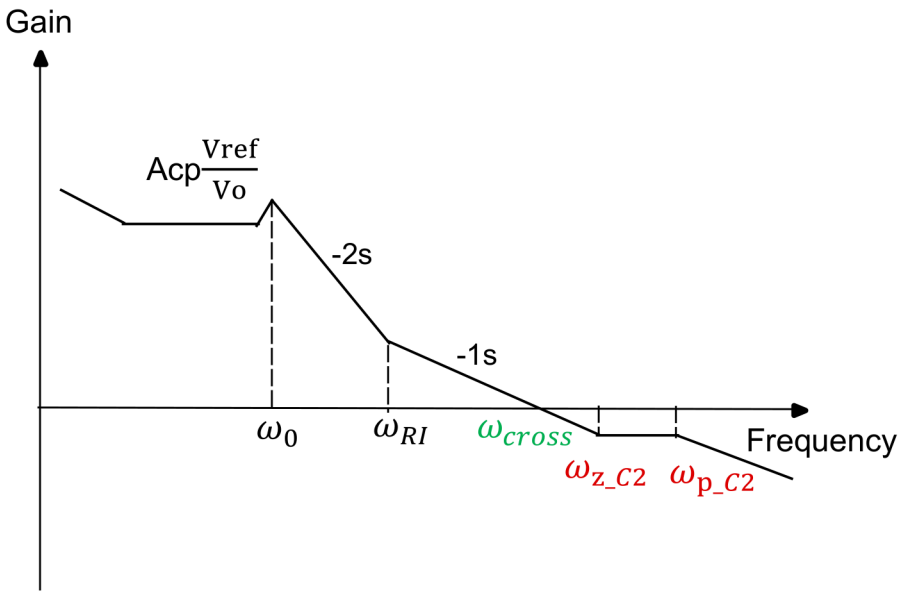


**Figure 4-1. Loop Gain of a D-CAP3 Converter With $\omega_{z\_C2} > \omega_{cross}$**

The loop stable condition is $\omega_{z\_C2} > \omega_{cross}$, the crossover frequency can be calculated by:

$$\frac{20\lg\left(\mathrm{Acp}\frac{\mathrm{Vref}}{\mathrm{V_0}}\right) - 20\lg(\mathrm{G_{RI}})}{\lg(\omega_0) - \lg(\omega_{\mathrm{RI}})} = -40\ \mathrm{dB/decade}$$
$$\frac{20\lg(\mathrm{G_{RI}}) - 0}{\lg(\omega_{\mathrm{RI}}) - \lg(\omega_{\mathrm{cross}})} = -20\ \mathrm{dB/decade} \quad (10)$$

The $\omega_{cross}$ can be given by:

$$\omega_{\mathrm{cross}} = \frac{\mathrm{Acp\ Vref}\ \omega_0^2}{\mathrm{V_0}\omega_{\mathrm{RI}}} \quad (11)$$

At the same time, the introduced C2 makes the double pole frequency $\omega_0$ become small and causes the crossing frequency to decrease as well. If the $\omega_{cross} \le \omega_{RI,}$ the loop gain crosses 0 dB with -40-dB/decade slope, which results in the loop becoming unstable without enough phase margin. So, the loop stable condition is $\omega_{z\_C2} > \omega_{cross}$ and $\omega_{cross} > \omega_{RI,}$ which can be given by:

$$C_2 r_2 < \frac{\mathrm{V_0}\omega_{\mathrm{RI}}}{\mathrm{Acp Vref}\omega_0^2} \quad (12)$$

and

$$C_2 < \frac{\mathrm{Acp Vref}\omega_0^2}{LV_0\omega_{\mathrm{RI}}} - C_1 \quad (13)$$

**Case 2:** when the ESR and capacitance is large enough, and $\omega_{z\_C2}$ is pushed into the bandwidth as shown in Figure 4-2, $\omega_{z\_C2} < \omega_{cross}$. Since the gain curve passes through the zero $\omega_{z\_C2}$, the slope of the gain curve becomes 0, which changes to -20dB/decade only when the slope encounters the pole $\omega_{p\_C2}$. So, when the zero $\omega_{z\_C2}$ enters within the bandwidth, the poles $\omega_{p\_C2}$ must be inside the bandwidth, and the crossing frequency occurs after the $\omega_{p\_C2}$. The zero and pole inside crossover frequency increases the bandwidth and can cause the loop to become unstable when the crossover frequency exceeds 1/3×fsw. To provide loop stabilization, the conditions that $\omega_{cross} < 1/3\times fsw$ and $\omega_{z\_C2} < \omega_{cross}$ need to be met.

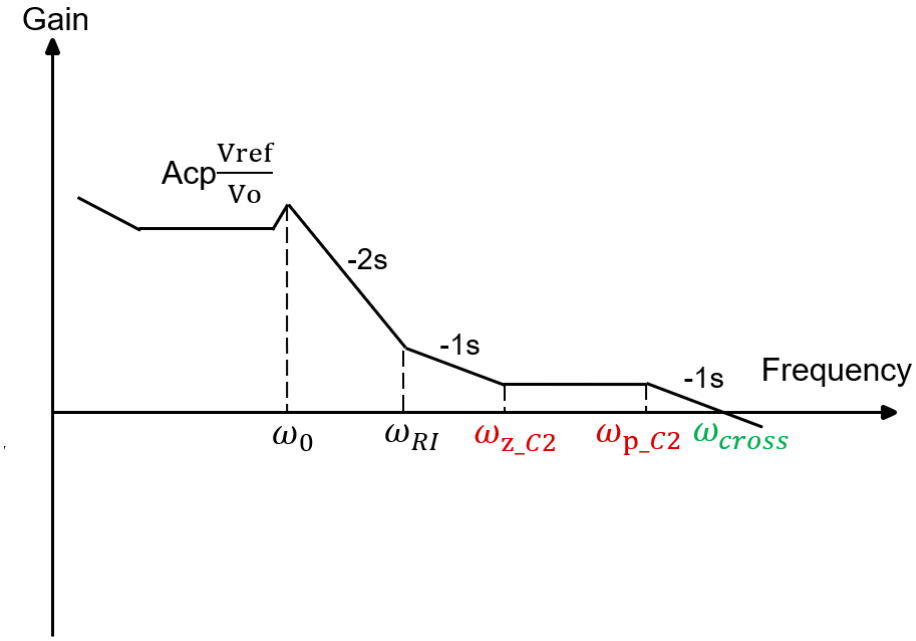


**Figure 4-2. Loop Gain of a D-CAP3™ Converter With $\omega_{z\_C2} < \omega_{cross}$**

The crossover frequency can be calculated by:

$$\frac{20\lg\left(\mathrm{Acp}\frac{\mathrm{Vref}}{V_0}\right) - 20\lg(G_{RI})}{\lg(\omega_0) - \lg(\omega_{RI})} = -40\ \mathrm{dB/decade}$$
$$\frac{20\lg(G_{RI}) - 20\lg\left(G_{z\_C2}\right)}{\lg(\omega_{RI}) - \lg\left(\omega_{z\_C2}\right)} = -20\ \mathrm{dB/decade} \quad (14)$$
$$\frac{20\lg\left(G_{p\_C2}\right) - 0}{\lg\left(\omega_{p\_C2}\right) - \lg(\omega_{cross})} = -20\ \mathrm{dB/decade}$$
$$\lg\left(G_{p\_C2}\right) = \lg\left(G_{z\_C2}\right)$$

The $\omega_{cross}$ can be given by:

$$\omega_{cross} = \frac{\mathrm{Acp}\ \mathrm{Vref}\ \omega_0^2\ \omega_{p\_C2}}{V_0\omega_{RI}\ \omega_{z\_C2}} \quad (15)$$

Summarizing the two previous conditions, the loop stable conditions can be given by:

$$\omega_{z\_C2} > \frac{\mathrm{Acp}\ \mathrm{Vref}\ \omega_0^2}{V_0\omega_{RI}} \quad (16)$$

or

$$\frac{\mathrm{Acp}\ \mathrm{Vref}\ \omega_0^2\ \omega_{p\_C2}}{V_0\omega_{RI}\ \omega_{z\_C2}} < \frac{1}{3}\mathrm{fsw} \quad (17)$$

If the ESR and capacitance of C2 is too large and the $\omega_{z\_C2}$ is less than $\omega_{RI}$ or $\omega_0$, the bandwidth increases more than case 2. This situation rarely occurs in the application design and the calculation of crossing frequency is more complex. Getting the crossover frequency through bench test is recommended because this method is simple and accurate. The $\omega_{cross}$ calculation is not discussed more in-depth in this section. The calculation results are ideal and have deviation with the bench test results. Verifying the loops stability of the hybrid output

capacitor network is recommended with the help of the bench loop test or simulation model. The suitable C2 can be selected based on the above principles and analysis method.

## 5 Application Design Example of D-CAP3™ Converter With a Hybrid Output Capacitors Network

This section introduces the loop performance for large ESR and small ESR with the same output capacitance value. The TPS51386EVM board is used to perform the loop test and the Bode plot for loop analysis. The setups are $V_{in}$= 20 V, $V_o$= 1.8 V, $I_{out}$= 8 A, $f_{sw}$= 600 kHz, L= 1 µH, and C1= 22 µF (effective value) with 2-mΩ ESR.

**Test 1**: C2= 150 µF with 5-mΩ ESR.

Equation 5 through Equation 8 are used to calculate the zero and pole, which can be given by $\omega_0$= 12.1 kHz, $\omega_{z\_C1}$= 3.62 MHz, $\omega_{z\_C2}$= 212.3 kHz, and $\omega_{p\_C2}$= 1.19 MHz.

Figure 5-1 shows the loop test results, that the crossover frequency is 59.03 kHz, and that the phase margin is 41.98 degrees. The crossover frequency is less than the 1/3×fsw and the loop is stable.

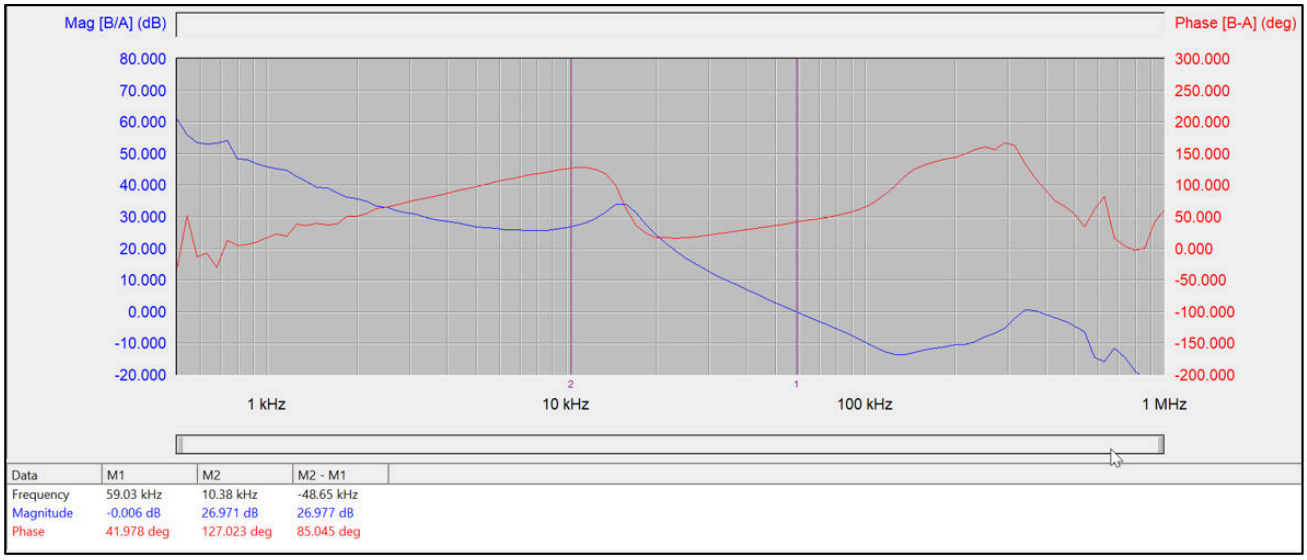


**Figure 5-1. Experimental Result With C2= 150 µF, 5-mΩ ESR**

**Test 2:** C2= 150 µF with 70-mΩ ESR.

Equation 5 through Equation 8 are used to calculate the zero and pole, which can be given by $\omega_0$= 12.1 kHz, $\omega_{z\_C1}$= 3.62 MHz, $\omega_{z\_C2}$= 15.2 kHz, $\omega_{p\_C2}$= 115.3 kHz.

Figure 5-2 shows the loop test results that the crossover frequency is 202.83 kHz and the phase margin is at 82.18 degrees. The crossover frequency is greater than the 1/3×fsw, which can cause the loop to be unstable.

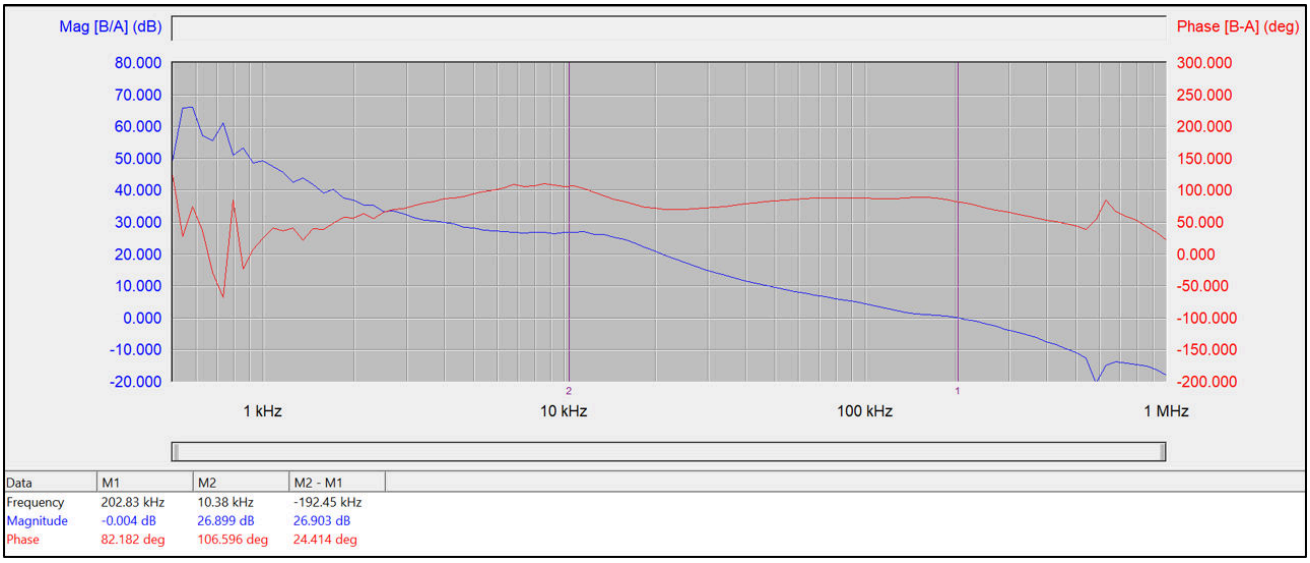


**Figure 5-2. Experimental Result With C2= 150 µF, 70-mΩ ESR**

## 6 Summary

A zero and pole calculation and loop stability method with hybrid capacitor network forD-CAP2™ and D-CAP3™ converters is proposed in this application note. When the ESR of the output capacitor is too large, an additional pair of poles and zeros is introduced and can be pushed into the bandwidth. This method increases the bandwidth and can cause loop instability when the bandwidth is greater than 1/3×fsw.

## 7 References

1. Texas Instruments, *D-CAP2TM Frequency Response Model based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection*, application note.
2. Texas Instruments, *How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors*, application note.
3. Texas Instruments, *Stability Analysis and Design of D-CAP2 and D-CAP3 Converter - Part 1: How to Select Output Capacitor*, application note.
4. Texas Instruments, *TPS51386 4.5-V to 24-V Input, 8-A Synchronous Buck Converter With Latched OVP/ UVP, Adjustable Soft Start, and PSM/OOA Modes*, data sheet.

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