

TPS715AxxEVM

This User's Guide describes the characteristics, operation, and use of the TPS715AxxEVM evaluation module (EVM). The EVM is designed to help the user easily evaluate and test the operation and functionality of the TPS715Axx. The User's Guide includes setup instructions for the hardware, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the EVM.

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1 Related Documentation From Texas Instruments

TPS715Axx data sheet ([SBVS047](#))

2 Introduction

The Texas Instruments TPS715AxxDRB is a low dropout regulator (LDO) in a 3x3-mm QFN package that provides output currents up to 80 mA. Both fixed and adjustable output voltage units are available.

2.1 Background

The TPS715AxxEVM uses the TPS715A01 and the TPS715A33 in a 3x3-mm QFN package to provide 3.3 V and 5 V at up to 80 mA. The EVM operates with full-rated performance with an input voltage between 3.5 V and 24 V.

2.2 Performance Specification

[Table 1](#) provides a summary of the TPS715AxxEVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input voltage		3		24	V
Output voltage U1	I _{out} = 10 mA to 100 mA	3.133	3.3	3.465	V
Output voltage U2	I _{out} = 10 mA to 100 mA	4.9	5	5.1	V
Output current		0		80	mA

2.3 Modifications

The PWB for this EVM is designed to accommodate both the fixed (U2) and adjustable (U1) versions of this IC.

2.3.1 Fixed Output IC U2 Operation

U2 is configured for operation of the fixed output version. No resistor adjustment is provided.

2.3.2 Adjustable Output IC U1 Operation

U1 is configured for evaluation of the adjustable output version. Resistors R1 and R2 are used to set the output voltage between 1.2 V and 15 V. This unit is configured for 5 V. See the data sheet for more information.

3 Setup

This section describes how to properly set up the TPS715AxxEVM.

3.1 Input/Output Connector Descriptions

J1–VIN Positive input connection from the input supply for U1.

J2–GND Return connection from the input supply for U1. Common with J4.

J3–VOUT Output voltage from U1.

J4–GND Output return connection for U1. Common with J2.

J5–VIN Positive input connection from the input supply for U2.

J6–GND Return connection from the input supply for U2. Common with J8.

J7–VOUT Output voltage from U2.

J8–GND Output return connection for U2. Common with J6.

3.2 Operation

To operate the EVM, connect an input supply to the appropriate pins, and connect a load to the appropriate pins.

4 Board Layout

This section provides the TPS715AxxEVM board layout and illustrations.

4.1 Layout

Figure 1, Figure 2, and Figure 3 show the board layout for the TPS715AxxEVM PWB.

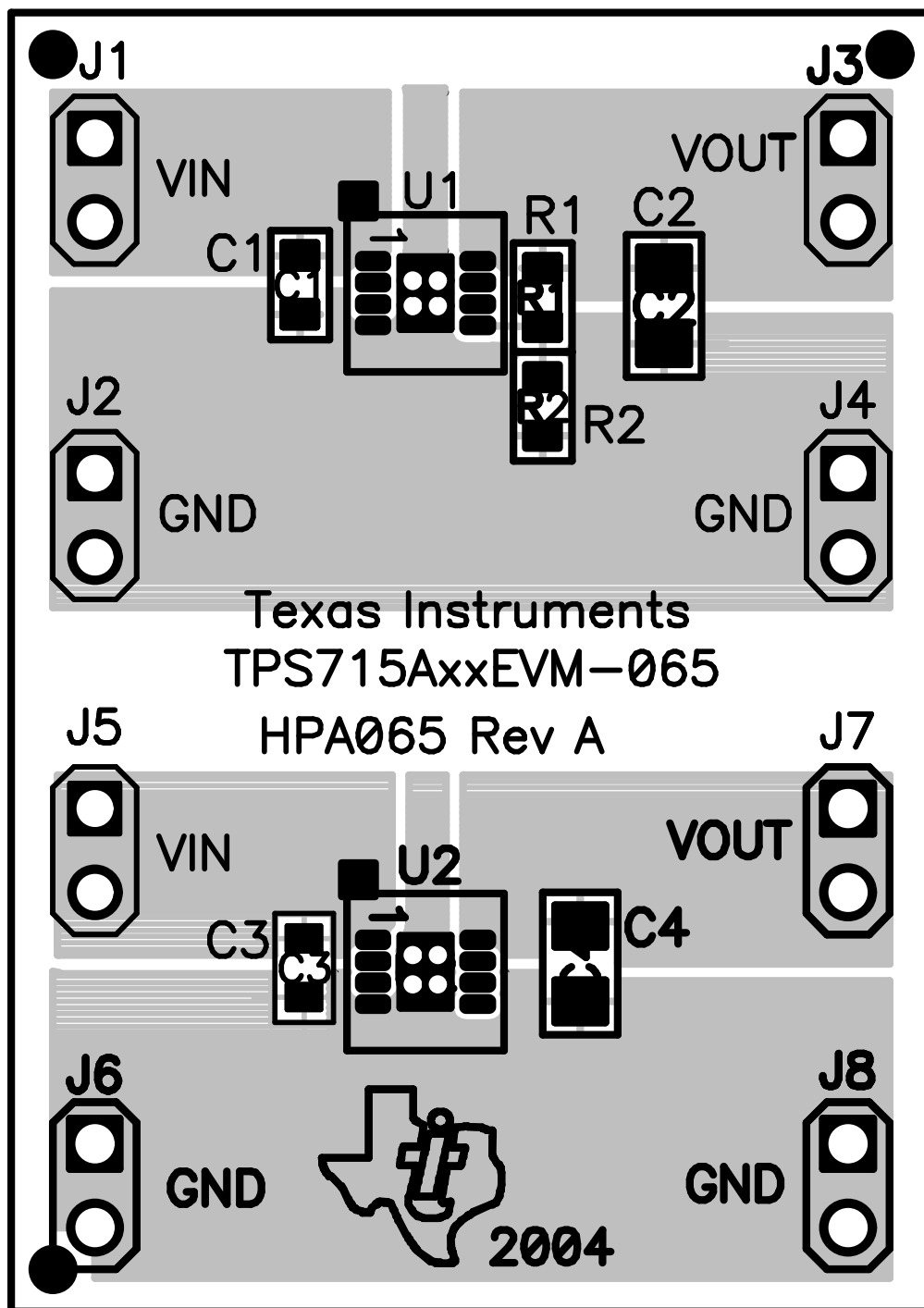


Figure 1. Assembly Layer

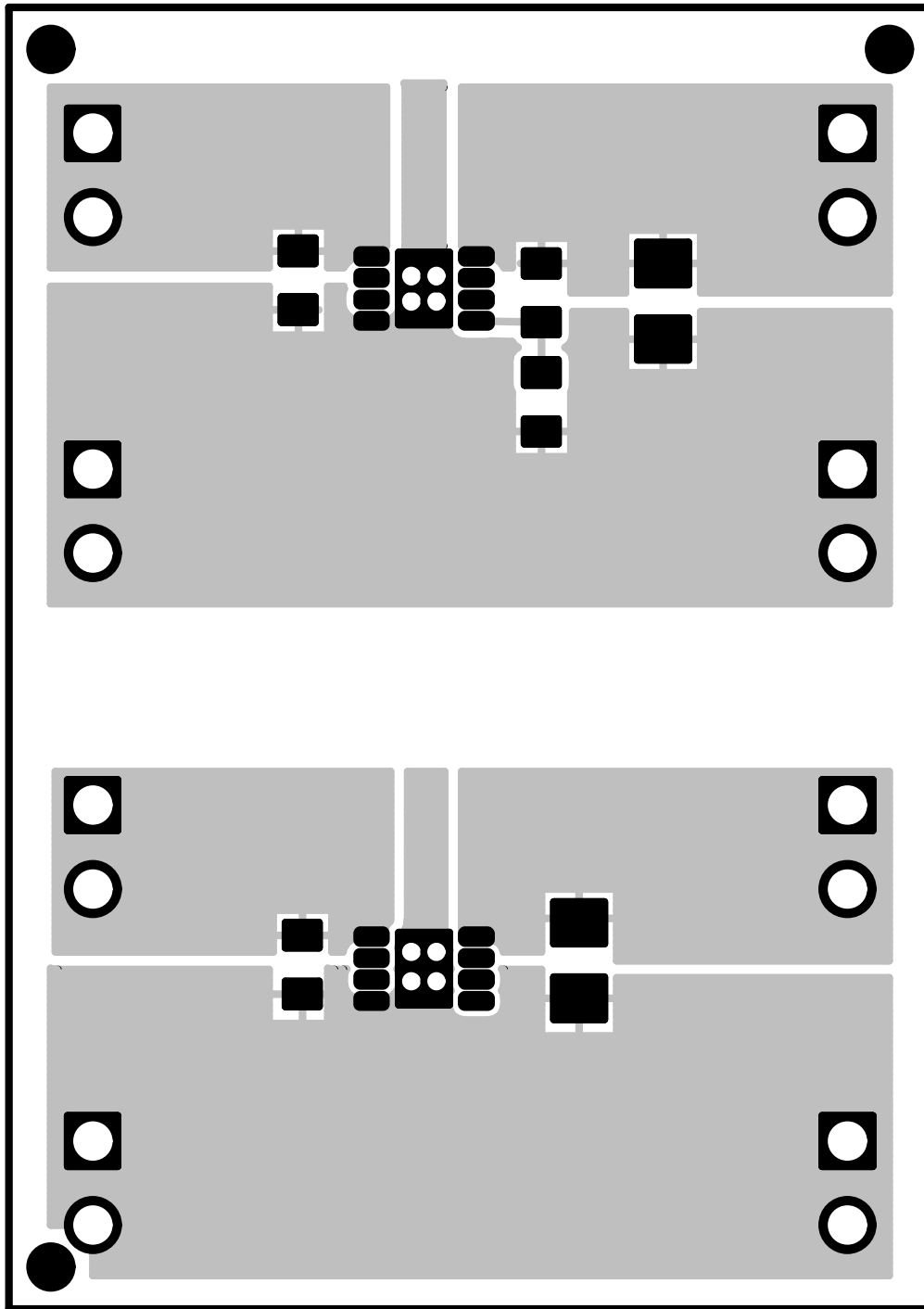


Figure 2. Top Layer Routing

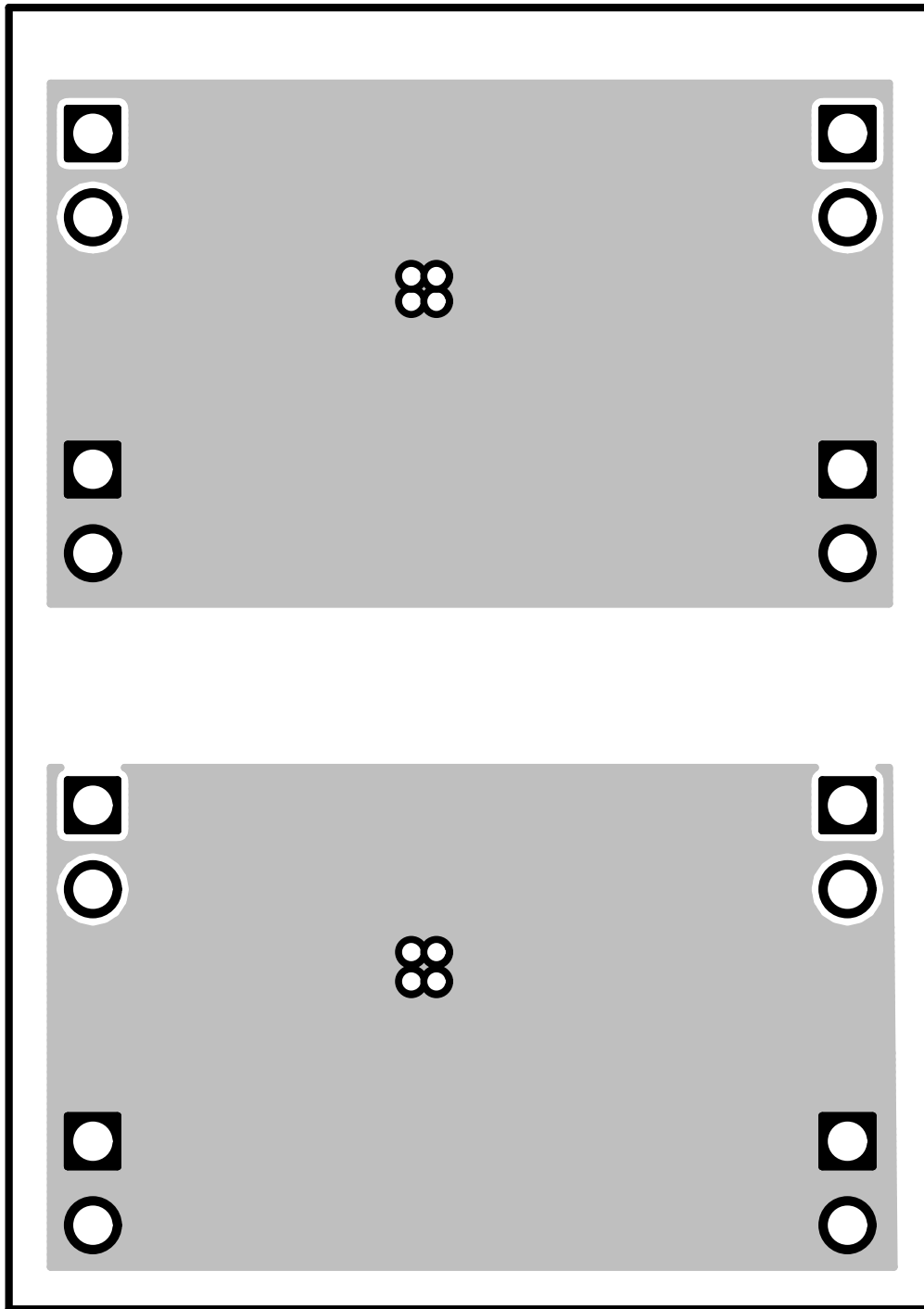


Figure 3. Bottom Layer Routing

5 Schematic and Bill of Materials

This chapter provides the TPS715AxxEVM schematic and bill of materials.

5.1 Schematic

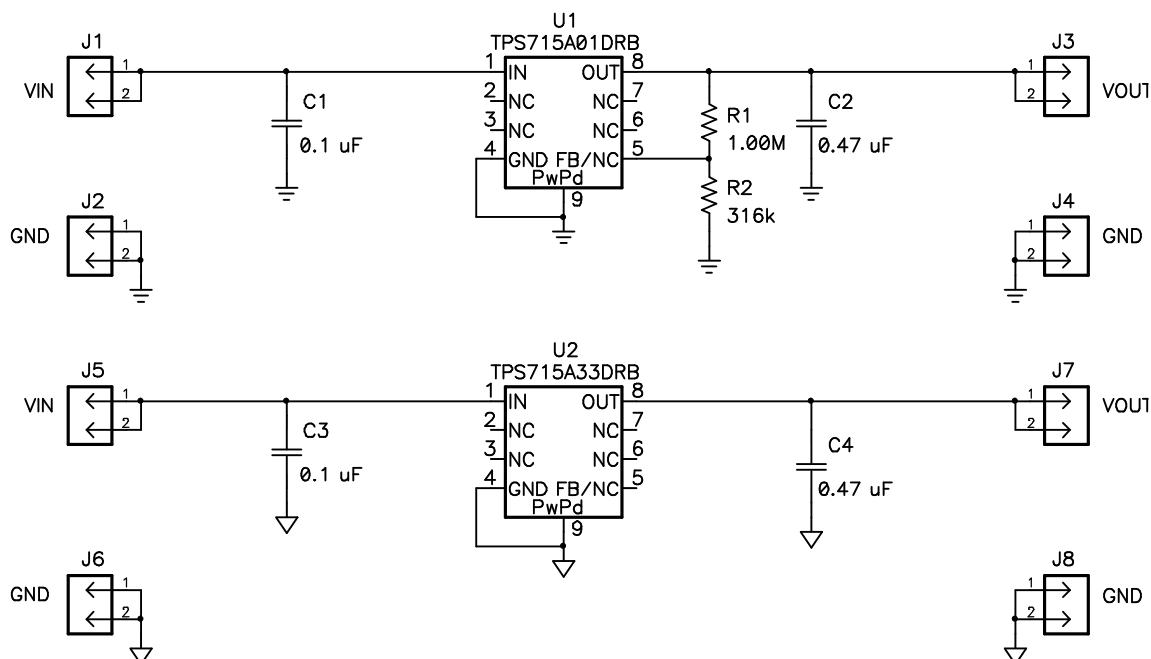


Figure 4. TPS715AxxEVM Schematic

5.2 Bill of Materials

Table 2. TPS715AxxEVM Bill of Materials

Count	Ref Des	Description	Size	Part Number	MFR
2	C1, C3	Capacitor, ceramic, 0.1- μ F, 25-V, X7R, 10%	0603	C1608X7R1E104K	TDK
2	C2, C4	Capacitor, ceramic, 0.47- μ F, 16-V, X5R, 10%	0805	C2012X7R1C474K	TDK
8	J1–J8	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 \times 2	PTC36SAAN	Sullins
1	R1	Resistor, chip, 1.00 M Ω , 1/16-W, 1%	0603	Std	Std
1	R2	Resistor, chip, 316 k Ω , 1/16-W, 1%	0603	Std	Std
1	U1	IC, high input voltage, micropower, 3.2 μ A at 80 mA LDO, Adj-V	QFN-8	TPS715A01DRB	TI
1	U2	IC, high input voltage, micropower, 3.2 μ A at 80 mA LDO, 3.3-V	QFN-8	TPS715A33DRB	TI
1	—	PCB, 1.55 In \times 1.1 In \times 0.062 In		HPA065	Any

FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.5 V to 24 V and the output voltage range of 3.3 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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