TPS2384 Eight Port EVM

This User's Guide describes the TPS2384 Eight Port EVM (HPA152). This guide contains the EVM schematic, bill of materials and assembly drawings.

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1 Introduction

This User's Guide describes the setup and operation of the TPS2384 Eight Port EVM (HPA152). Information and instruction presented throughout this document assumes user familiarity with the MSP430, the TPS2384 and with the IEEE 802.3af Specification for Power Over Ethernet.

2 Hardware Overview

The HPA152 EVM features the TPS2384 made by Texas Instruments, Inc. The EVM has been designed to be configured as both an Endpoint PSE or a Midspan PSE using two TPS2384 devices to create eight IEEE 802.3af Ethernet ports.

Each TPS2384 controls four ports. The HPA152 EVM uses an MSP430 and custom firmware written by TI to operate in Power Management Mode (PMM). However, if necessary, the MSP430 can be bypassed and both TPS2384 devices can be configured to operate in Auto Mode (AM).

3 EVM Operation

3.1 Power Management Mode Operation

The HPA152 is configured at the factory for Power Management Mode. It also has firmware loaded into the MSP430 that can be exercised using the GUI available from the TI website. An external 48 volt power supply connected to J43 pin 1 (positive) and J43 pin 3 (negative) is required. This power supply provides the bias for the TPS2384 devices and is also used as the voltage source sent down the Ethernet cable. An external 3.3 volt power supply connected to J2 pin 2 (positive) and J2 pin 4 (negative) is also needed. The 3.3 volt power supply is used to bias the MSP430 and all the port LEDs.

The following jumpers are installed in the factory. For jumper function information, see section 3.3.

J3, J9–J14, J31–J34, J45, J46, J50–J52, J54–J56, J74–J77, J87, J88	Jumper installed
J15–J18, J27–J30,	Jumper installed between pin 1 and pin 2
J47–J49	Jumper installed between pin 2 and pin 3
J58–J61, J70–J73	Jumper installed between pin 1 and pin 2

Switch S1 and S2 are used to simulate power rail status inputs to the MSP430. Both must be set to a logic high (switch S1 is set towards R19 and switch S2 is set towards R20 on PCB).

Depressing the RESET button will generate a logic low signal to the RST* input of the MSP430 which will in turn generate a logic low signal to the PORB input of the TPS2384 which will reset all internal state machines and registers.

The firmware has been designed to control both TPS2384 devices on the HPA152 EVM. Each TPS2384 has an associated I2C Address Bus. This Address is set by S3 and S5. S3 sets the I2C Address for U8 to ‘01’ and S5 sets the I2C Address for U13 to ‘02’.

I2C Address Settings:	
S3 switch 6	Open
S3 switch 5	Open
S3 switch 4	Open
S3 switch 3	Open
S3 switch 2	Open
S3 switch 1	Closed
S5 switch 6	Open
S5 switch 5	Open
S5 switch 4	Open
S5 switch 3	Open
S5 switch 2	Closed
S5 switch 1	Open

3.2 Connectors

J1	RS232 communications connector
J2	3.3V power input connector
J6	Host I2C interface connector
J7	MSP430 JTAG input connector
J43	48V power input connector
J86	Expansion connector

3.3 Jumpers

J3	Allows the MSP430 to control the Mode Select input to the TPS2384s via an opto-coupler.
J4	If the MSP430 control of the Mode Select is not used, this jumper can be used to set the state of the Mode Select input to the TPS2384 devices. Setting the jumper between MS and 3.3V sets the board in Power Management Mode. Setting the jumper between MS and GND will place the module in Auto Mode.
J5	Can be used to monitor the RS232 communications between the host PC and the MSP430.
J8	Allows the user to manually pull-up or connect to ground the PORB signal going to the TPS2384 devices. If PORB is under MSP430 control, this jumper must be left open. If Auto Mode of the TPS2384 devices is desired, this jumper can be installed between PORB and 3.3V to keep the board reset input inactive.
J9	Allows the MSP430 to control the PORB input to the TPS2384 devices. If Auto Mode is desired, this jumper should be removed.
J10	Connects the MSP430 P6.3 GPIO to the clock input (CLK-1) of the LED Control Circuit.
J11	Connects the MSP430 P1.3 GPIO to the I2C Serial Clock lines on the TPS2384 devices.
J12	Connects the MSP430 P6.4 GPIO to the data input (DATA-1) of the LED Control Circuit.
J13	Connects the MSP430 P1.2 GPIO to the I2C Serial Data lines on the TPS2384 devices.
J14	Connects the MSP430 P6.5 GPIO to the latch input (LATCH-1) of the LED Control Circuit.
J31	Places D25 in the circuit to indicate that Port 0 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load generated by this circuit will keep the port from powering off after the PD has been removed.
J32	Places D27 in the circuit to indicate that Port 1 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load created by this circuit will keep the port from powering off after the PD has been removed.
J33	Places D29 in the circuit to indicate that Port 2 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load generated by this circuit will keep the port from powering off after the PD has been removed.
J34	Places D31 in the circuit to indicate that Port 3 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load created by this circuit will keep the port from powering off after the PD has been removed.
J44	Can be used to ground the CT input of U8. See the TPS2384 datasheet for details.
J45	Makes the SCL1 connection between the opto-coupler and the TPS2384 devices.
J46	Makes the SDA_IN connection between the opto-coupler and the TPS2384 devices.
J47	Allows AltA/B of the TPS2384 devices to be set to a logic high or a logic low. See the TPS2384 datasheet for details.
J48	Allows MS of the TPS2384 devices to be set to a logic high or a logic low. See the TPS2384 datasheet for details. If used to set MS, J53 must be removed to prevent the opto-coupler from trying to drive this signal.
J49	Allows WDIS of the TPS2384 devices to be set to a logic high or a logic low. See the TPS2384 datasheet for details.
J50	When used with J51, allows the S4 reset switch to be placed in the circuit. J50 and J51 should only be installed if J52 is not installed.
J51	Provides an external pull-up to the POR inputs of the TPS2384 devices. This jumper should only be installed if J52 is not installed.
J52	Makes the PORB1 connection between the opto-coupler and the TPS2384 devices.
J53	Makes the MS1 connection between the opto-coupler and the TPS2384 devices.
J54	When installed, allows U8 to receive 48 volts.
J55	Allows the TPS2384 3.3V output to supply power to the opto-couplers. If an external 3.3V supply is used to power the opto-couplers, this jumper must be removed.
J56	Makes the SDA_OUT connection between the TPS2384 devices and the opto-coupler.
J57	Allows the TPS2384 port outputs (ports 0 thru 3) to be monitored or connected elsewhere.
J74	Places D62 in the circuit to indicate that Port 4 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load generated by this circuit will keep the port from powering off after the PD has been removed.
J75	Places D64 in the circuit to indicate that Port 5 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load created by this circuit will keep the port from powering off after the PD has been removed.
J76	Places D66 in the circuit to indicate that Port 6 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load generated by this circuit will keep the port from powering off after the PD has been removed.
J77	Places D68 in the circuit to indicate that Port 7 is powered. This jumper should not be installed if operating in AC Disconnect mode. The additional load created by this circuit will keep the port from powering off after the PD has been removed.
J87	Allows the SYN output of U8 to control the SYN input of U13.
J88	When installed, allows U13 to receive 48 volts.
J89	Allows the TPS2384 port outputs (ports 4 thru 7) to be monitored or connected elsewhere.

3.4 Port Power Configuration

In *Power Management Mode*, the HPA152 can be commanded via the GUI to discover, classify and power up IEEE 802.3af compliant Powered Devices (PDs). Power will be applied to the Ethernet port on either the spare pairs or on the data lines of the RJ-45 connector. The HPA152 EVM is designed with jumper blocks which allow the user to configure the method in which power is applied to the PD. The following tables can be used to help the user set the appropriate jumpers depending on the desired power delivery configuration. Even though the tables show all ports being configured the same way, each port can be configured independently of all other ports.

The following configuration inserts 48 volts on the spare pins of the RJ-45 connectors (positive on pins 4 and 5 and negative on pins 7 and 8).				
Port 0 Configuration:				
	Jumper Block	1	2	3
	J16	X	X	
	J27	X	X	
	J36			
	J35			
Port 1 Configuration:				
	Jumper Block	1	2	3
	J17	X	X	
	J30	X	X	
	J38			
	J37			
Port 2 Configuration:				
	Jumper Block	1	2	3
	J15	X	X	
	J28	X	X	
	J40			
	J39			
Port 3 Configuration:				
	Jumper Block	1	2	3
	J18	X	X	
	J29	X	X	
	J42			
	J41			
Port 4 Configuration:				
	Jumper Block	1	2	3
	J58	X	X	
	J70	X	X	
	J79			
	J78			
Port 5 Configuration:				
	Jumper Block	1	2	3
	J59	X	X	
	J71	X	X	
	J81			
	J80			
Port 6 Configuration:				
	Jumper Block	1	2	3
	J60	X	X	

The following configuration inserts 48 volts on the spare pins of the RJ-45 connectors (positive on pins 4 and 5 and negative on pins 7 and 8).				
	J72	X	X	
	J83			
	J82			
Port 7 Configuration:				
	Jumper Block	1	2	3
	J61	X	X	
	J73	X	X	
	J85			
	J84			

The following configuration inserts 48 volts on the spare pins of the RJ-45 connectors (positive on pins 7 and 8 and negative on pins 4 and 5).				
Port 0 Configuration:				
	Jumper Block	1	2	3
	J16		X	X
	J27		X	X
	J36			
	J35			
Port 1 Configuration:				
	Jumper Block	1	2	3
	J17		X	X
	J30		X	X
	J38			
	J37			
Port 2 Configuration:				
	Jumper Block	1	2	3
	J15		X	X
	J28		X	X
	J40			
	J39			
Port 3 Configuration:				
	Jumper Block	1	2	3
	J18		X	X
	J29		X	X
	J42			
	J41			
Port 4 Configuration:				
	Jumper Block	1	2	3
	J58		X	X
	J70		X	X
	J79			
	J78			
Port 5 Configuration:				
	Jumper Block	1	2	3
	J59		X	X
	J71		X	X
	J81			
	J80			

The following configuration inserts 48 volts on the spare pins of the RJ-45 connectors (positive on pins 7 and 8 and negative on pins 4 and 5).				
Port 6 Configuration:				
	Jumper Block	1	2	3
	J60		X	X
	J72		X	X
	J83			
	J82			
Port 7 Configuration:				
	Jumper Block	1	2	3
	J61		X	X
	J73		X	X
	J85			
	J84			

The following configuration inserts 48 volts on the data pair pins of the RJ-45 connectors (positive on pins 1 and 2 and negative on pins 3 and 6).				
Port 0 Configuration:				
	Jumper Block	1	2	3
	J16			
	J27			
	J36	X	X	
	J35	X	X	
Port 1 Configuration:				
	Jumper Block	1	2	3
	J17			
	J30			
	J38	X	X	
	J37	X	X	
Port 2 Configuration:				
	Jumper Block	1	2	3
	J15			
	J28			
	J40	X	X	
	J39	X	X	
Port 3 Configuration:				
	Jumper Block	1	2	3
	J18			
	J29			
	J42	X	X	
	J41	X	X	
Port 4 Configuration:				
	Jumper Block	1	2	3
	J58			
	J70			
	J79	X	X	
	J78	X	X	
Port 5 Configuration:				
	Jumper Block	1	2	3
	J59			

The following configuration inserts 48 volts on the data pair pins of the RJ-45 connectors (positive on pins 1 and 2 and negative on pins 3 and 6).				
	J71			
	J81	X	X	
	J80	X	X	
Port 6 Configuration:				
	Jumper Block	1	2	3
	J60			
	J72			
	J83	X	X	
	J82	X	X	
Port 7 Configuration:				
	Jumper Block	1	2	3
	J61			
	J73			
	J85	X	X	
	J84	X	X	

The following configuration inserts 48 volts on the data pair pins of the RJ-45 connectors (positive on pins 3 and 6 and negative on pins 1 and 2).				
Port 0 Configuration:				
	Jumper Block	1	2	3
	J16			
	J27			
	J36		X	X
	J35		X	X
Port 1 Configuration:				
	Jumper Block	1	2	3
	J17			
	J30			
	J38		X	X
	J37		X	X
Port 2 Configuration:				
	Jumper Block	1	2	3
	J15			
	J28			
	J40		X	X
	J39		X	X
Port 3 Configuration:				
	Jumper Block	1	2	3
	J18			
	J29			
	J42		X	X
	J41		X	X
Port 4 Configuration:				
	Jumper Block	1	2	3
	J58			
	J70			
	J79		X	X
	J78		X	X

The following configuration inserts 48 volts on the data pair pins of the RJ-45 connectors (positive on pins 3 and 6 and negative on pins 1 and 2).				
Port 5 Configuration:				
	Jumper Block	1	2	3
	J59			
	J71			
	J81		X	X
	J80		X	X
Port 6 Configuration:				
	Jumper Block	1	2	3
	J60			
	J72			
	J83		X	X
	J82		X	X
Port 7 Configuration:				
	Jumper Block	1	2	3
	J61			
	J73			
	J85		X	X
	J84		X	X

3.5 Test Points

The HPA152 EVM has been design with numerous test points. When making measurements, the user needs to be aware of which side of the isolation barrier is needed for referencing test equipment. Also, all eight Integration capacitor test points require special equipment (see table below for more information).

Test Points	Description
TP1	Ground Reference Point for MSP430 side of isolation barrier.
TP2	Ground Reference Point for MSP430 side of isolation barrier.
TP3	Ground Reference Point for MSP430 side of isolation barrier.
TP4	Test point for monitoring the 48V_AC voltage source.
TP5	Test point for monitoring the 48V_SW voltage source.
TP6	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 3. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP7	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 2. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP8	Test point for monitoring AC_HI on U8
TP9	Test point for monitoring AC_LO on U8
TP10	Test point for monitoring SYN.
TP11	Test point for monitoring Ct.
TP12	Test point for monitoring the 2.5V internal bias source.
TP13	Test point for monitoring SDA.
TP14	Test point for monitoring SDA-I.
TP15	Test point for monitoring SCL.
TP16	Test point for monitoring the 3.3V voltage source.
TP17	Ground Reference point for TPS2384 side of isolation barrier.
TP18	Test point for monitoring the 10V internal bias source.
TP19	Test point for monitoring the 6.3V internal bias source.
TP20	Test point for monitoring WD_DIS.

Test Points	Description
TP21	Ground Reference point for TPS2384 side of isolation barrier.
TP22	Test point for monitoring INT.
TP23	Test point for monitoring POR
TP24	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 0. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP25	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 1. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP26–TP29	Ground Reference point for TPS2384 side of isolation barrier.
TP30	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 6. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP31	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 7. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP32	Test point for monitoring AC_HI on U13
TP33	Test point for monitoring AC_LO on U13
TP34	Test point for monitoring SYN.
TP35	Test point for monitoring Ct.
TP36	Test point for monitoring the 2.5V internal bias source.
TP37	Test point for monitoring SDA.
TP38	Test point for monitoring SDA-I.
TP39	Test point for monitoring SCL.
TP40	Test point for monitoring the 3.3V voltage source.
TP41	Ground Reference point for TPS2384 side of isolation barrier.
TP42	Test point for monitoring the 10V internal bias source.
TP43	Test point for monitoring the 6.3V internal bias source.
TP44	Test point for monitoring WD_DIS.
TP45	Ground Reference point for TPS2384 side of isolation barrier.
TP46	Test point for monitoring INT.
TP47	Test point for monitoring POR
TP48	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 5. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP49	Test point for monitoring the voltage ramp on the A/D integration capacitor for port 4. This is a high impedance input and performance may be affected by any additional impedance. It is recommended that a low capacitance/FET input buffer be used when monitoring this test point.
TP50–TP53	Ground Reference point for TPS2384 side of isolation barrier.

3.6 Auto Mode Operation

The HPA152 EVM can be placed in Auto Mode by moving the jumper on J4 between MS and GND. The PORB jumper (J9) must be removed and used to pull-up the PORB input to the module by placing the jumper between PORB and 3.3V on J8.

In Auto Mode operation, the LEDs on either side of the RJ45 connectors will not operate. These LEDs are only available during Power Management Mode. However, in order to determine whether a port is powered or not, each port has a separate LED (D25, D27, D29, D31, D62, D64, D66 and D68) which turns on after the port has been classified and power is being sent to the PD. In order for these LEDs to operate, their respective jumpers need to be inserted (J31, J32, J33, J34, J74, J75, J76 and J77).

4 Bill of Materials

Table 1. HPA152 Bill of Materials

Count	RefDes	Value	Size	MFR	Part Number	Description
27	C1– C10, C35–C40, C43– C45, C48–C50, C73, C74, C76, C77, C80	0.1 µF	1260	Std	Std	Capacitor, Ceramic, 0.1 µF,100V, X7R
16	C11–C14, C20, C22, C24, C26, C51–C54, C60, C62, C64, C66	0.1 µF	0805	Std	Std	Capacitor, Ceramic, 0.1 µF,100V, X7R, 20%
16	C15–C19, C21, C23, C25, C55, C56–C59, C61, C63, C65	1000 pF	1808	TDK	C4520X7R3D102K	Capacitor, Ceramic, 1000-pF, 2000-V, X7R
8	C27–C30, C67–C70	220 nF	1210	TDK	C3225X7R2A224K	Capacitor, Ceramic, 220 nF, 100V, X7R, 10%
1	C31	68 µF	0.670 × 0.750	Panasonic	EEV-FK2A680Q	Capacitor, Aluminum, SM, 68 µF, 100-V,
1	C32	220 µF	18 × 16,5 mm	Panasonic	EEVFK2A221M	Capacitor, Aluminum, 220 µF, 100V, 20%
8	C33, C34, C46, C47, C71, C72, C78, C79	0.027 µF	0.126 × 0.098	Panasonic	ECHU1H273GX5	Capacitor, Film Chip,0.027-µF, 50V, 2%
1	C41	1 µF	0805	Vishay	Std	Capacitor, Ceramic, 1-µF, 25V, X7R, 10%
1	C42	220 pF	0805	Kemet	C0805C221FGAC7800	Capacitor, Ceramic, 220pF, 100V, C0G, 1%
0	C75	220 pF	0805	Kemet	C0805C221FGAC7800	Capacitor, Ceramic, 220pF, 100V, C0G, 1%
18	D1, D3, D5, D7, D9, D11, D13, D15, D25, D27, D29, D31, D51, D53, D62, D64, D66, D68	LN1371G	SMD	Panasonic	LN1371G	Diode, LED, Green, 20-mA, 0.9-mcd
16	D17–D24, D54–D61		SOD-323	Protek Devices	GBLC03C	Diode, TVS, 19 Clamping Voltage V, 350W
8	D2, D4, D6, D8, D10, D12, D14, D16		0.114 × 0.049 in	Panasonic	LN1471Y	Diode, LED, Amber, 20-mA, -.4-mcd
8	D26, D28, D30, D32, D63, D65, D67, D69			ON Semiconductor	1SMB5932BT3	Zener Diode, 20V, 3W
8	D33–D36, D70–D73		SMA	ST	EB2BA	Diode, Schottky, 2A, 100V
16	D37, D38, D40, D42–D45, D47, D74–D77, D82–D85		SMA	St	STPS1H100A	Diode, Schottky, 1A, 100V
8	D39, D41, D46, D48, D78–D81		SMA	Littelfuse	SMAJ10A	Diiode, Transient Voltage Supressor, 400W, 10V
1	D49		SMA	Diodes Inc.	SMAJ12A	Diode, Zener, 12-V, 1W
1	D50		SMA	Diodes	SMAJ58A	Diode, SMT TVS 400W, 58V
1	D52		SMA	Diodes Inc.	1SMA5919BT3	Diode, Zener
1	D86		SMA	Diodes Inc.	S2B-13	Diodes Rectifier, 1.5A 100V

Table 1. HPA152 Bill of Materials (continued)

Count	RefDes	Value	Size	MFR	Part Number	Description
8	F1–F8		TH	Raychem	RXE090	Polyswitch, 0.47 Ω Max, 40 A Max, 72 V Max
1	J1		TH	Norcomp	182-009-212-171	Connector, 9-pin D, Right Angle, Female
8	J19, J21, J23, J25, J62, J64, J66, J68	RJ-45	TH	AMP	556416	Connector, Jack, Modular, 8 POS
8	J20, J22, J24, J26, J63, J65, J67, J69	RJ-45	TH	AMP	520252-4	Connector, Jack, Modular, Rt, Angle, 8 POS
2	J6, J43		TH	Weidmüller	1793830000	Header, 6-pin, 150mil spacing
2	J6, J43, Socket		Socket	Weidmüller	1798890000	Header, 6-pin, Socket 150mil spacing
1	J2			Weidmüller	1793810000	Header, 4-pin, 150mil spacing
1	J2, Socket			Weidmüller	1798870000	Header, 4-pin, Socket 150mil spacing
27	J3, J9–J14, J31–J34, J44–J46, J50–J56, J74–J77, J87, J88		0.100 × 2	Sullins	PTC36SAAN	Header, 2-pin, 100 mil spacing
38	J4, J5, J8, J15–J18, J27–J30, J35–J42, J47–J49, J58–J61, J70–J73, J78–J85		0.100 × 3	Sullins	PTC36SAAN	Header, 3-pin, 100 mil spacing
2	J57, J89		0.100 × 8 in	Sullins	PTC36SAAN	Header, 8-pin, 100 mil spacing
2	J7, J86		0.100 × 2X7	3M	2514-6002UB	Connector, Straight 2x7 pin, 100 mil spacing
8	L1–L8		0.320 × 0.198	Coilcraft	TTDLF2500	Inductor, 2 Lines, 0.500A, 5 µH
1	Q1		D2PAK	IR	IRF540NS	Transistor, NFET, 100V, 33A, 44 mΩ
1	Q2		SOT23		BSS119E6327	MOSFET, N-ch, 100-V, 0.17-A, zz-mΩ
1	Q3		SOT23	Fairchild	FDV301N	MOSFET, N-ch, 25-V, 220-mA, 5 Ω
17	R1—R3, R5–R7, R10, R11, R13, R18, R21–R26, R80	330	0805	Vishay	Std	Resistor, Chip, 330-Ω, 1/10W, 5%
4	R12, R14, R66, R67	2K	0805	Vishay	Std	Resistor, Chip, 2-kΩ, 1/10W, 5%
1	R16	68.1K	0805	Std	Std	Resistor, Chip, 68.1-kΩ, 1/10W, 5%
32	R28–R35, R40–R47, R81–R88, R93–R100	85	0603	Std	Std	Resistor, Chip, 75 Ω, 1/10W, 5%
9	R36–R39, R68, R89–R92	10K	0805	Std	Std	Resistor, Chip, 10 kΩ, 1/10W, 5%
8	R48–R51, R101–R104	7.5K	0805	Std	Std	Resistor, Chip, 7.5 Ω, 1/10W, 5%
1	R52	100 Ω	0805	Std	Std	Resistor, Chip, 100 Ω, 1/10W, 5%
1	R53	0.01	2512	IRC	LCR-LRF2512-01-RO10-F	Resistor, Metal Strip, 0.01 Ω, 2W, 1%
1	R55	187K	0805	Std	Std	Resistor, Chip, 187 kΩ, 1/10W, 5%
1	R56	69.8K	0805	Std	Std	Resistor, Chip, 69.8 kΩ, 1/10W, 1%
4	R57–R60	3.3K	0805	Std	Std	Resistor, Chip, 3.3 kΩ, 1/10W, 5%

Table 1. HPA152 Bill of Materials (continued)

Count	RefDes	Value	Size	MFR	Part Number	Description
16	R4, R15, R17, R19, R20, R54, R61–R65, R106–R110	100K	0805	Std	Std	Resistor, Chip, 100 kΩ, 1/10W, 5%
2	R59, R71	200	0805	Std	Std	Resistor, Chip, 200 kΩ, 1/10W, 5%
2	R70, R77	1K	0805	Std	Std	Resistor, Chip, 1 kΩ, 1/10W, 5%
2	R72, R111	124K	0805	Std	Std	Resistor, Chip, 124 kΩ, 1/10W, 0.1%
2	R73, R76	300	0805	Std	Std	Resistor, Chip, 300 Ω, 1/10W, 5%
2	R74, R75	3.9K	0805	Std	Std	Resistor, Chip, 3.9 kΩ, 1/10W, 5%
1	R78	7.15K	0805	Std	Std	Resistor, Chip, 7.5 kΩ, 1/10W, 5%
5	R8, R9, R27, R79, R105	0 Ω	0805	Std	Std	Resistor, Chip, 0 Ω, 1/10W, 1%
2	S1, S2		0.46 × 0.16	E_Switch	EG1218	Switch, 1P2T, Slide, PC-mount, 200-mA
2	S3, S5		0.60 × 0.40 in	Grayhill	76SB06S	Switch, 6-pole DIP, Raised Rocker
2	S4, S6		0.245 × 0.251	C & K	KT11P2JM	Switch, SPST, PB Momentary, Sealed Washable
8	T1–T8		0.500 × 0.370	Pulse	H2019	Xfmr, Center-tapped, Voice Over Ip
45	TP1–TP25, TP30–TP49		TH	Keystone	5012	Test Point, White, 0.062 Hole
8	TP26–TP29, TP50–TP53		SM	Keystone	5016	Test Point, SM, 0.150 × 0.090 in
1	U1		SSOP-16	Maxim	MAX3221ECAE	IC, RS-232 Transceivers with AutoShutdown
1	U10		SO-8	NEC	PS8802-2-A	IC, Optocoupler, Dual Open Collector Output
1	U11		SO14	TI	SN74LVC06A	IC, High-Speed CMOS Logic Hex Inverting Schmitt Trigger
1	U12		SO-8	NEC	PS9821-1-A	IC, Optocoupler, Single Open Collector Output
1	U2		QFP-64	TI	MSP430F169PM	IC, Mixed Signal Microcontroller
2	U3, U5		TVSOP-20	TI	SN74ALVCH373DGVR	IC, Octal Transparent D-Type Latch/3-State Outputs
2	U4, U6		TSSOP-14	TI	SN74HC164PW	IC, 8-Bit Parallel-Out Serial Shift Registers
1	U7		DGS10	TI	TPS2490DGS	IC, TPS2490DGS
2	U8, U113		PWFQ-64	TI	TPS2384PAP	IC, Quad Ethernet Power Sourcing
1	U9		SO-8	NEC	PS8821-2-A	IC, Optocouper, Dual Open Collector Output
1	X1	6–8 MHz	0.394 × 0.197	ECS	ZTT8.00MT	Crystal, 8.00 MHz
1				Any	HPA152	PCB, 7.250 in × 12.25 in × 0.062 in
35				Sullins	STC02SYAN	Shunts
12				SPC Technology	2563	Rubber Bumpers

Notes:

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFR's components.
5. Add 12 rubber bumpers to the bottom side of the board; 4 from left to right top, 4 from left to right bottom, and 4 from left to right middle

4.1 Related Documentation From Texas Instruments

1. TPS2384 Power Over Ethernet Quad PSE, data sheet, SLUS634
2. MSP430 data sheet, SLAS368

5 EVM Board Layout and Schematic

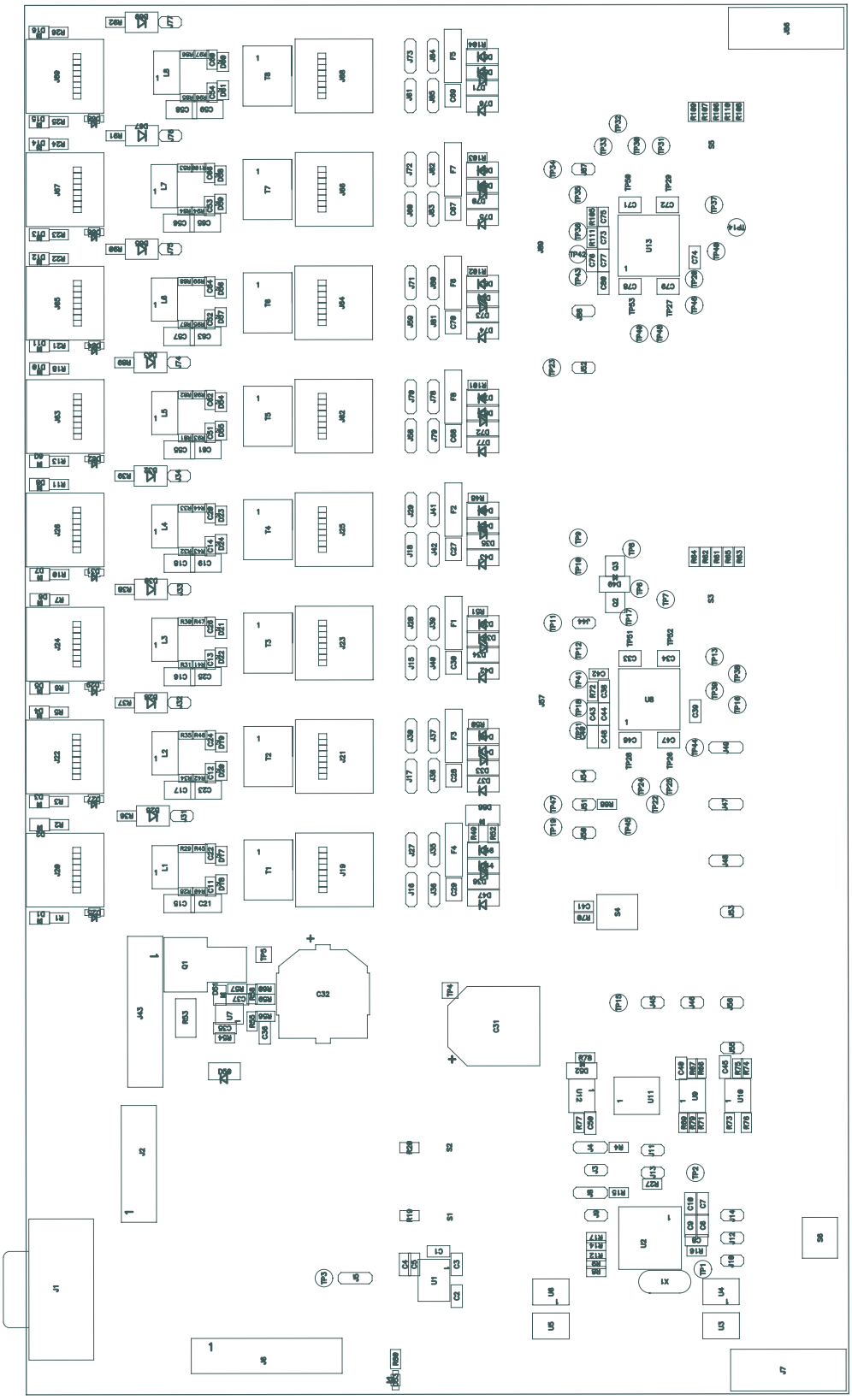

Figure 1. EVM Board Top Layer

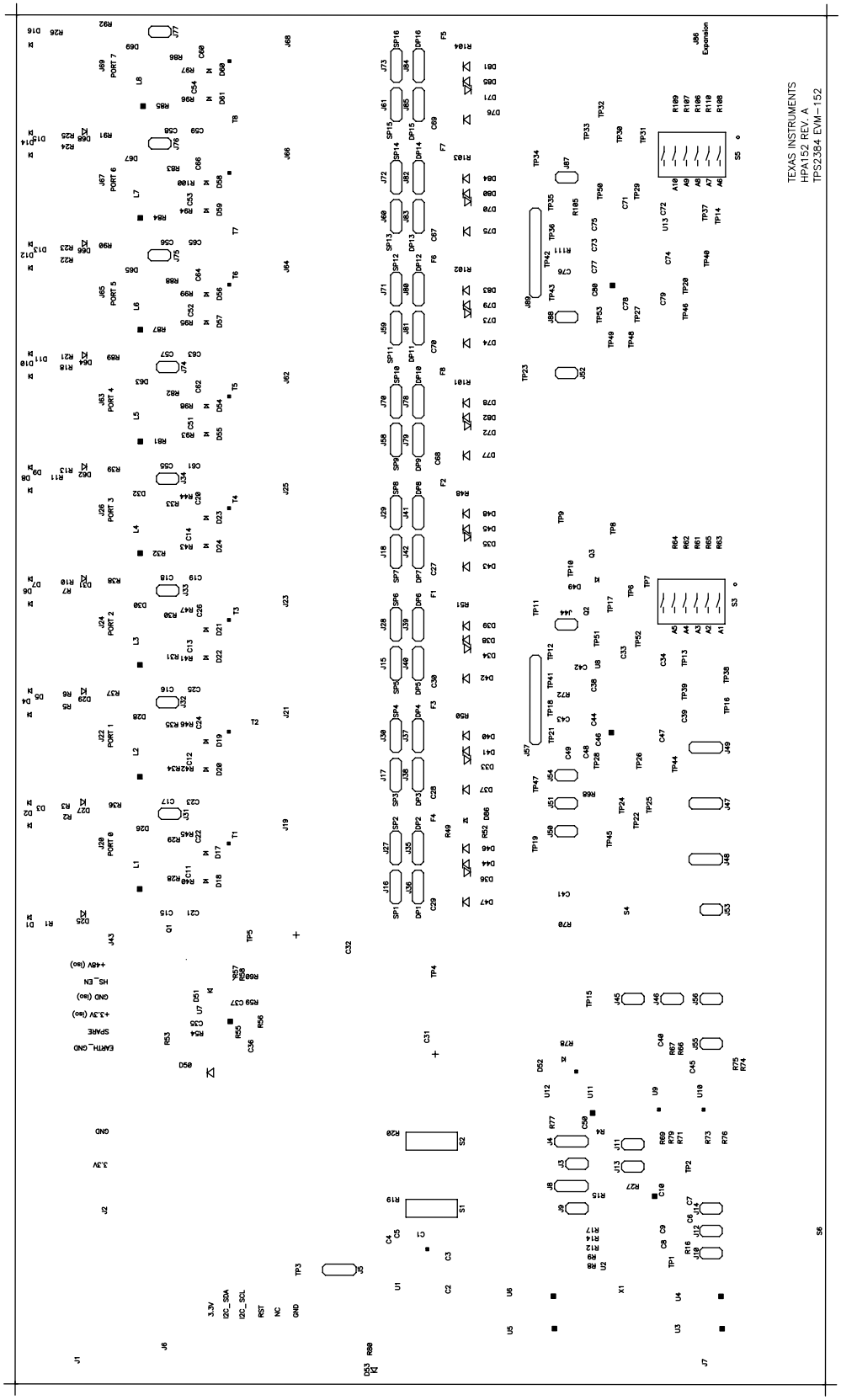

Figure 2. EVM Board Silkscreen

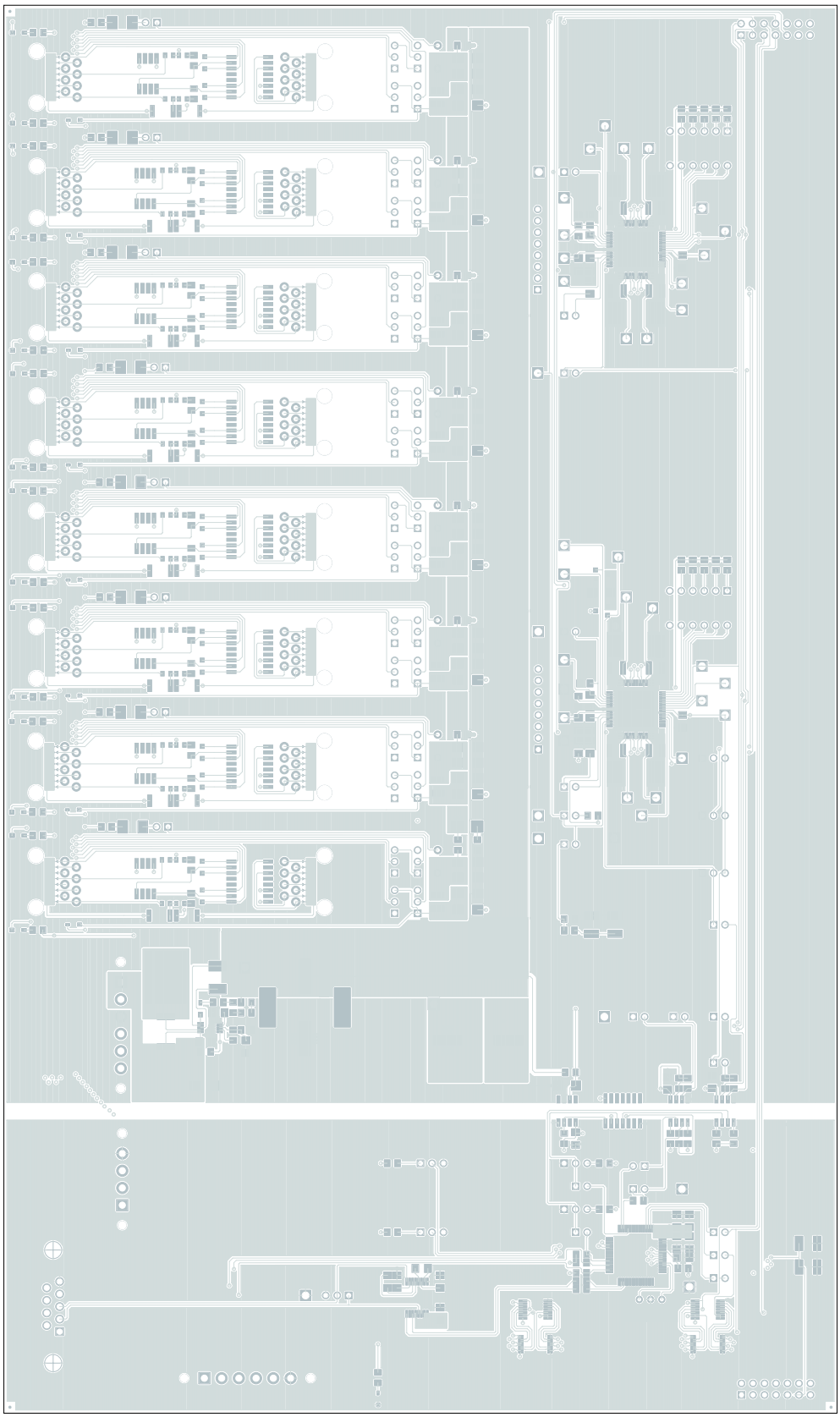

Figure 3. EVM Board Layout 2

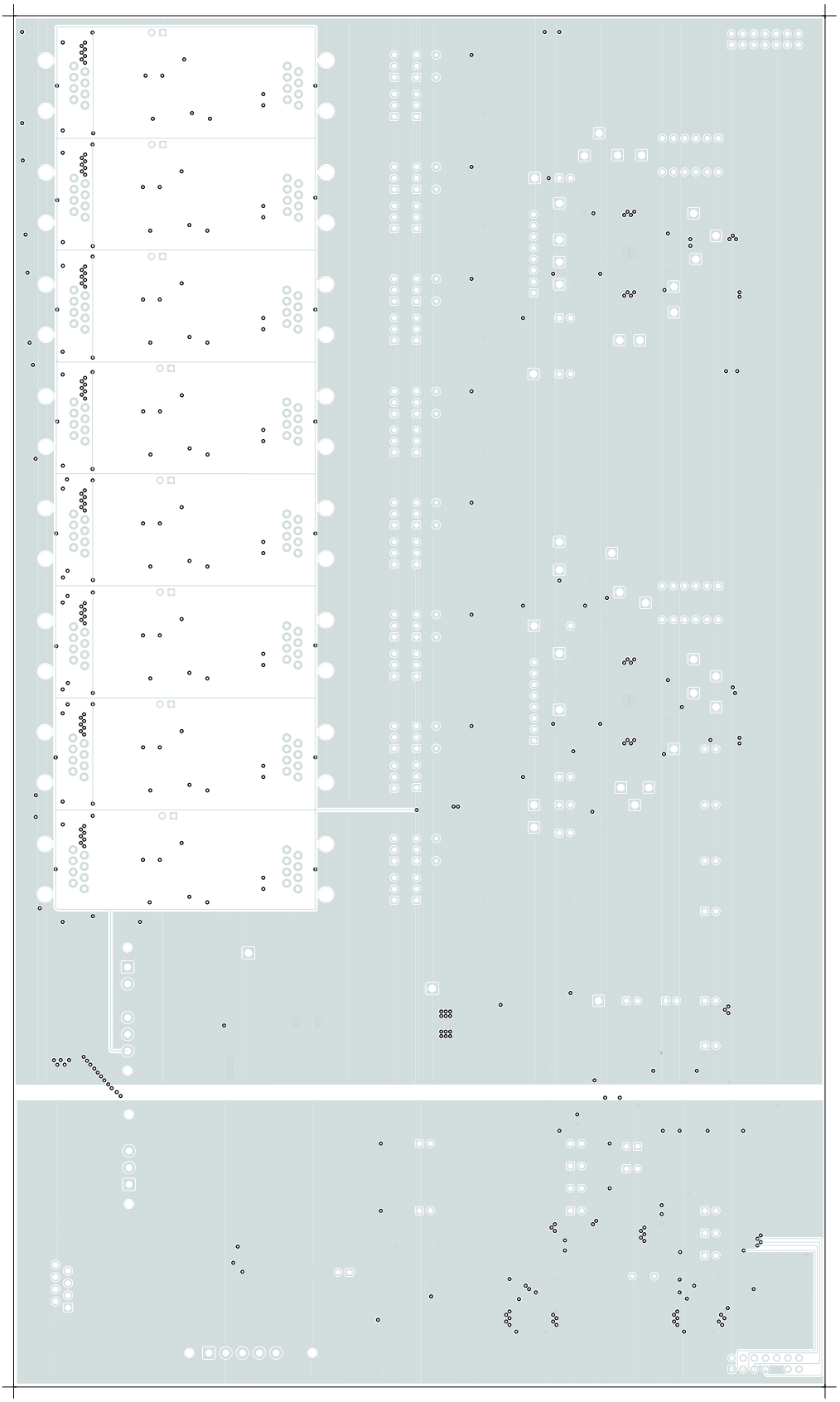

Figure 4. EVM Board Layout 3

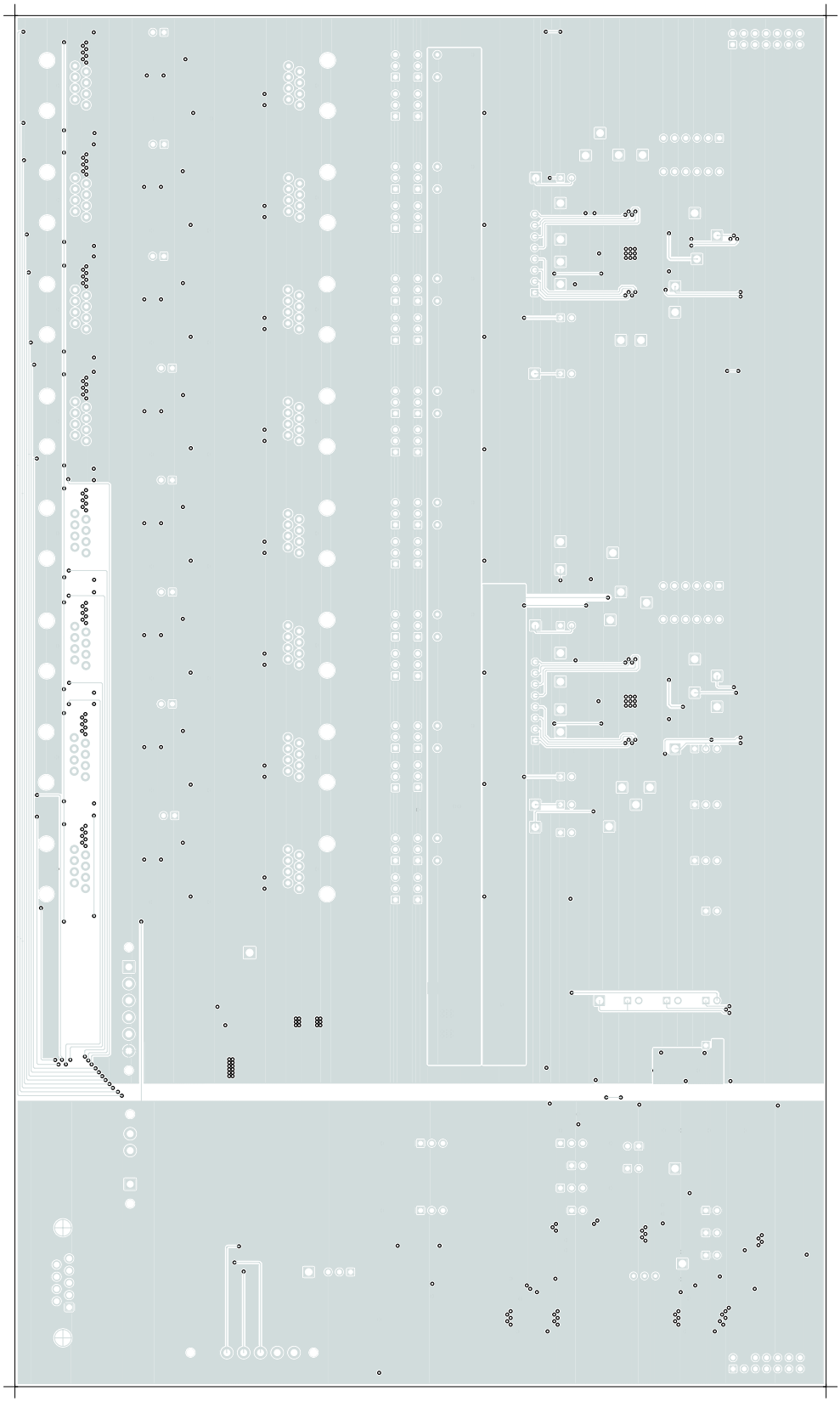

Figure 5. EVM Board Layout 4

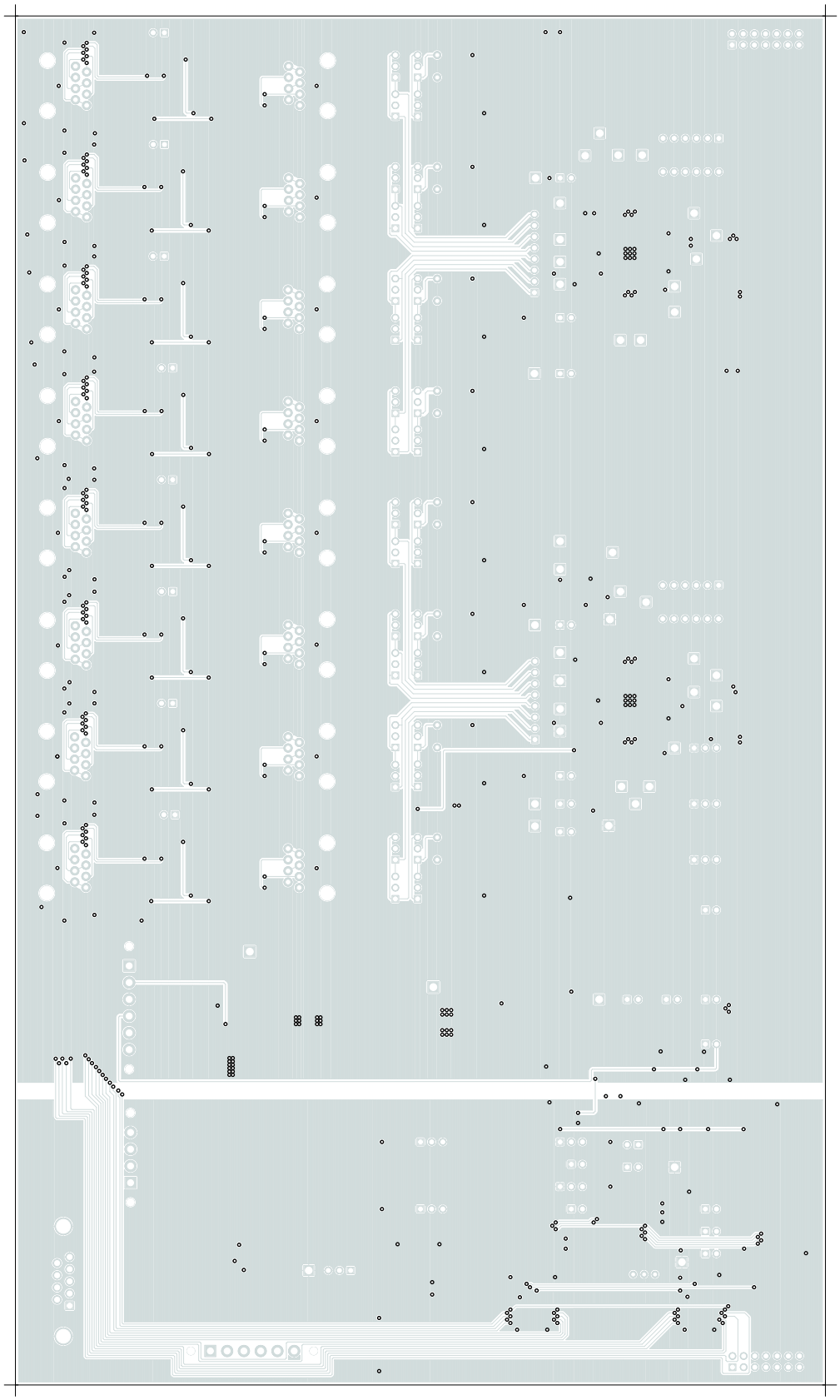

Figure 6. EVM Board Layout 5

FCC Warnings

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During normal operation, some circuit components may have case temperatures greater than 50°C . The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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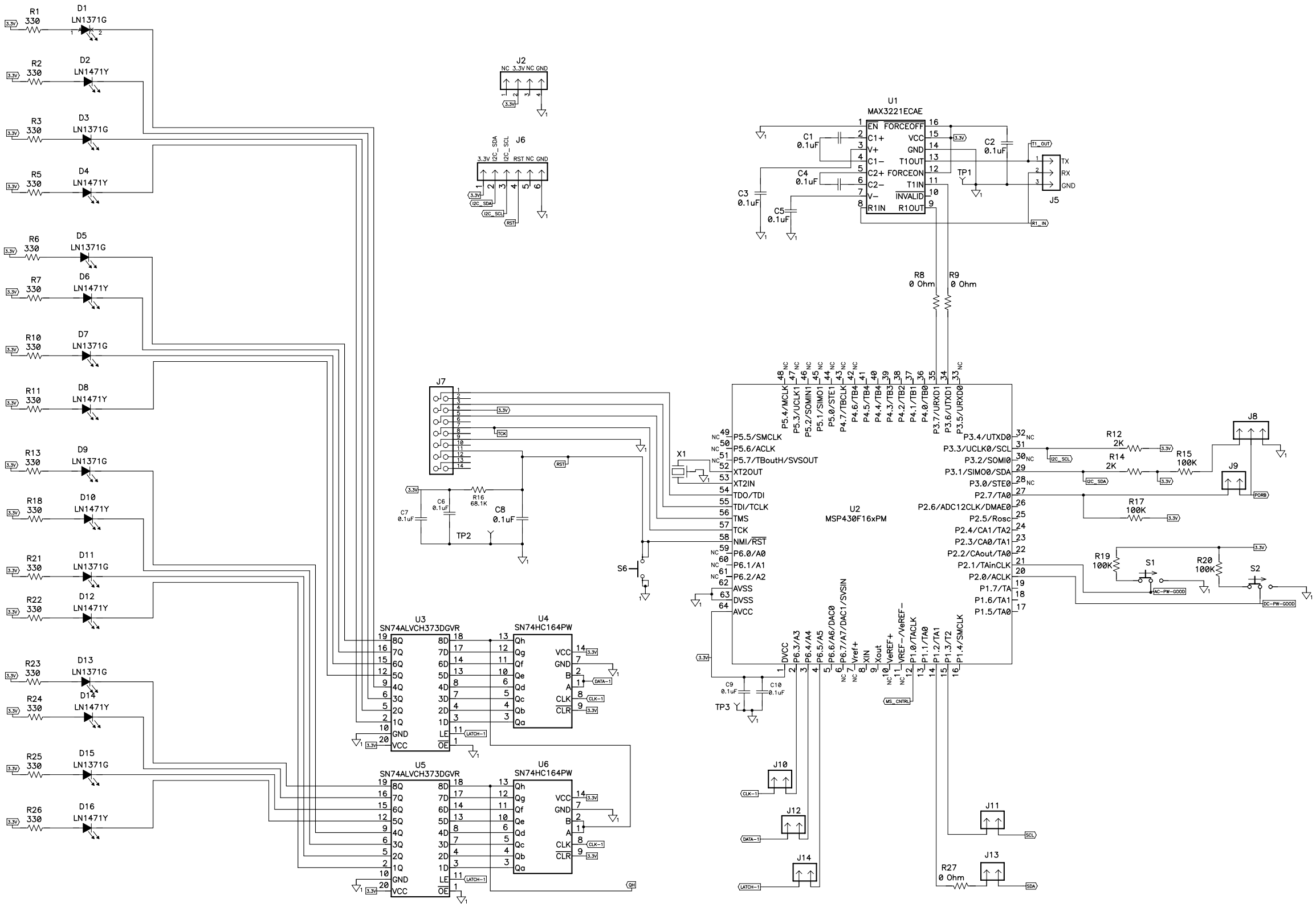

⚠ NOT USED

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Date	Wed Nov 30, 2005	Drawn by {Drawn By}	
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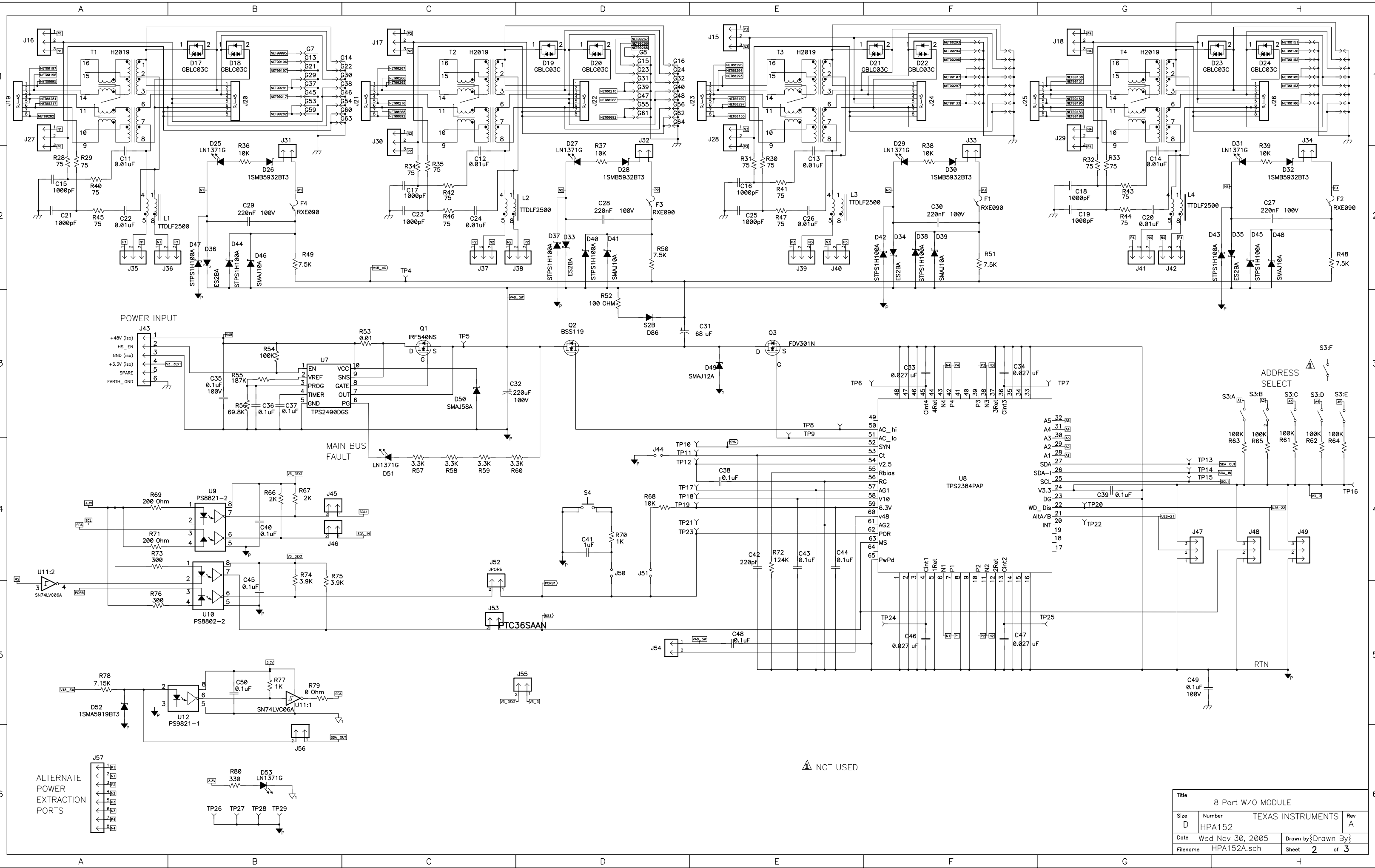

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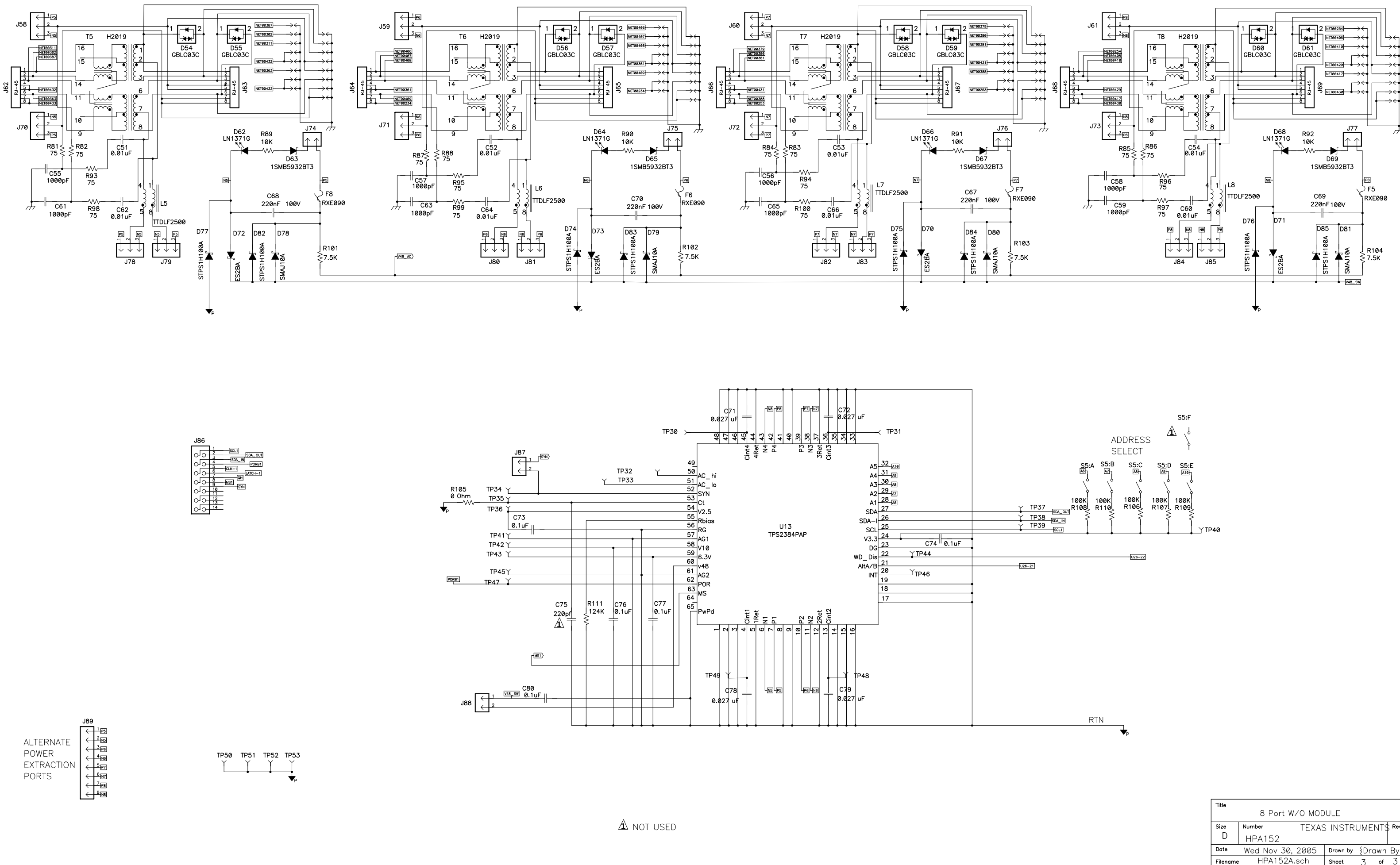

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Rev	A
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Filename	HPA152A.sch
Sheet	3 of 3

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