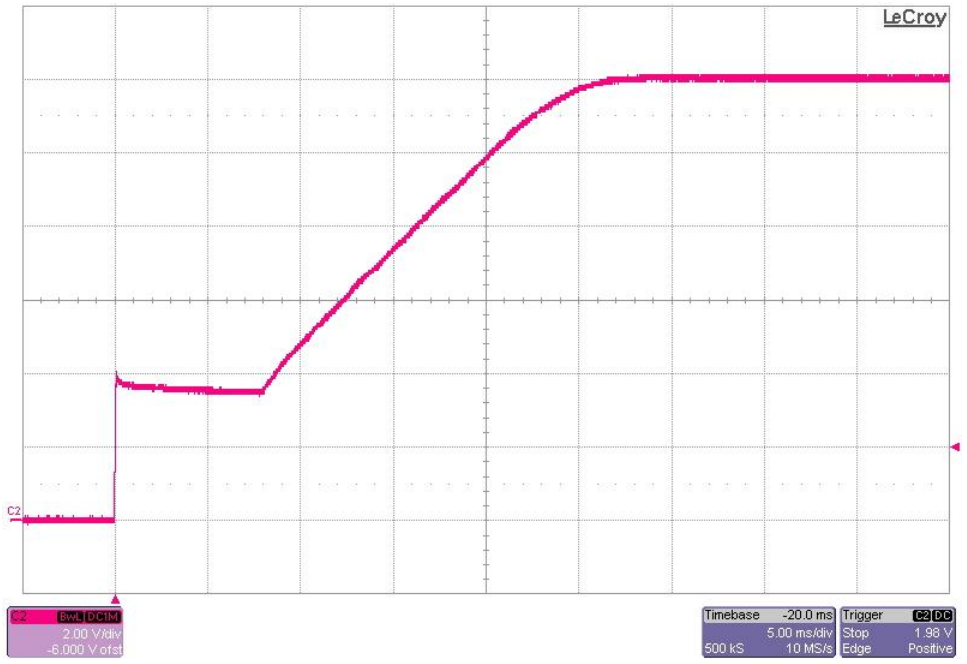
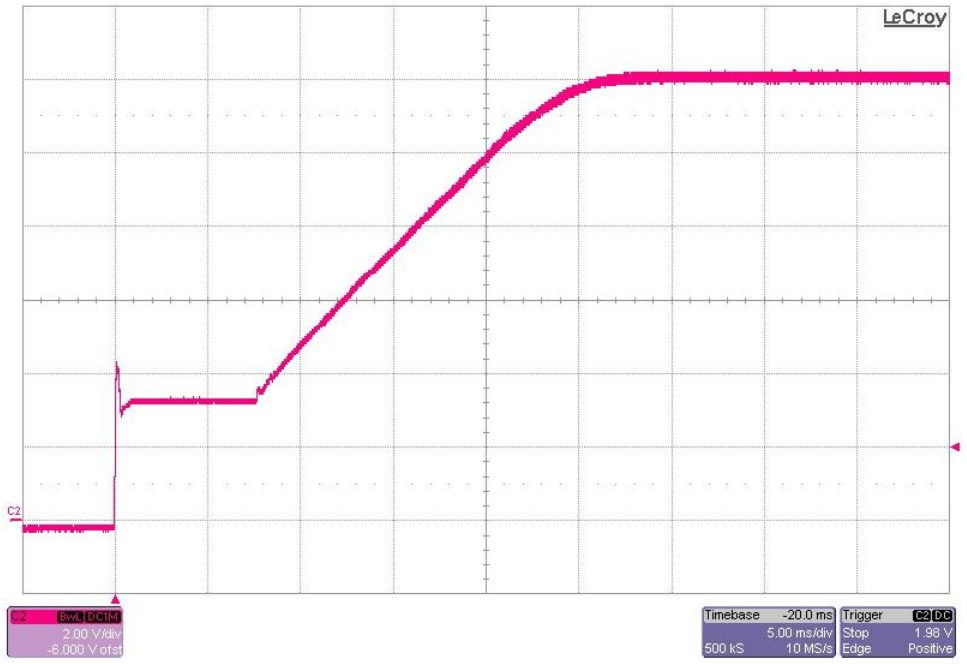
1 Startup

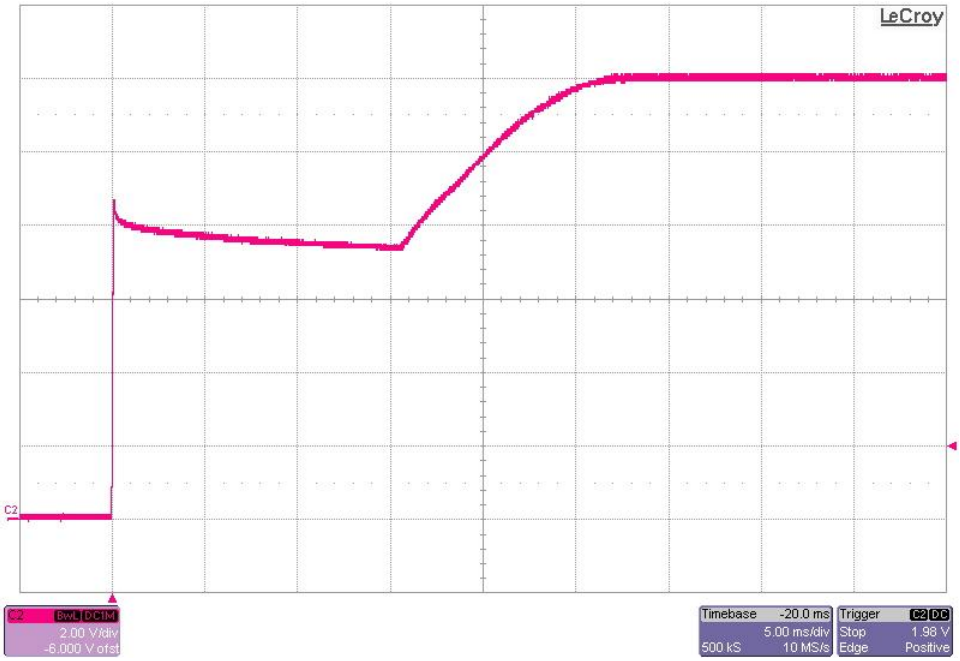
The photo below shows the output voltage startup waveform after the application of 3.8V in. The 12V output was loaded to 0A. (2V/DIV, 5mS/DIV)



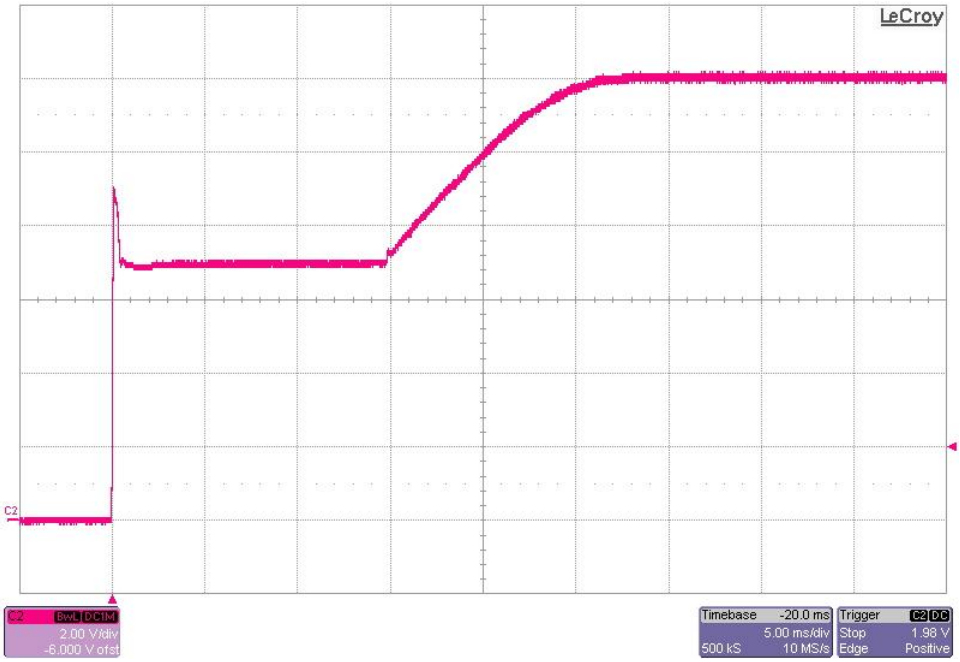
The photo below shows the output voltage startup waveform after the application of 3.8V in. The 12V output was loaded to 4A. (2V/DIV, 5mS/DIV)



The photo below shows the output voltage startup waveform after the application of 7.6V in. The 12V output was loaded to 0A. (2V/DIV, 5mS/DIV)

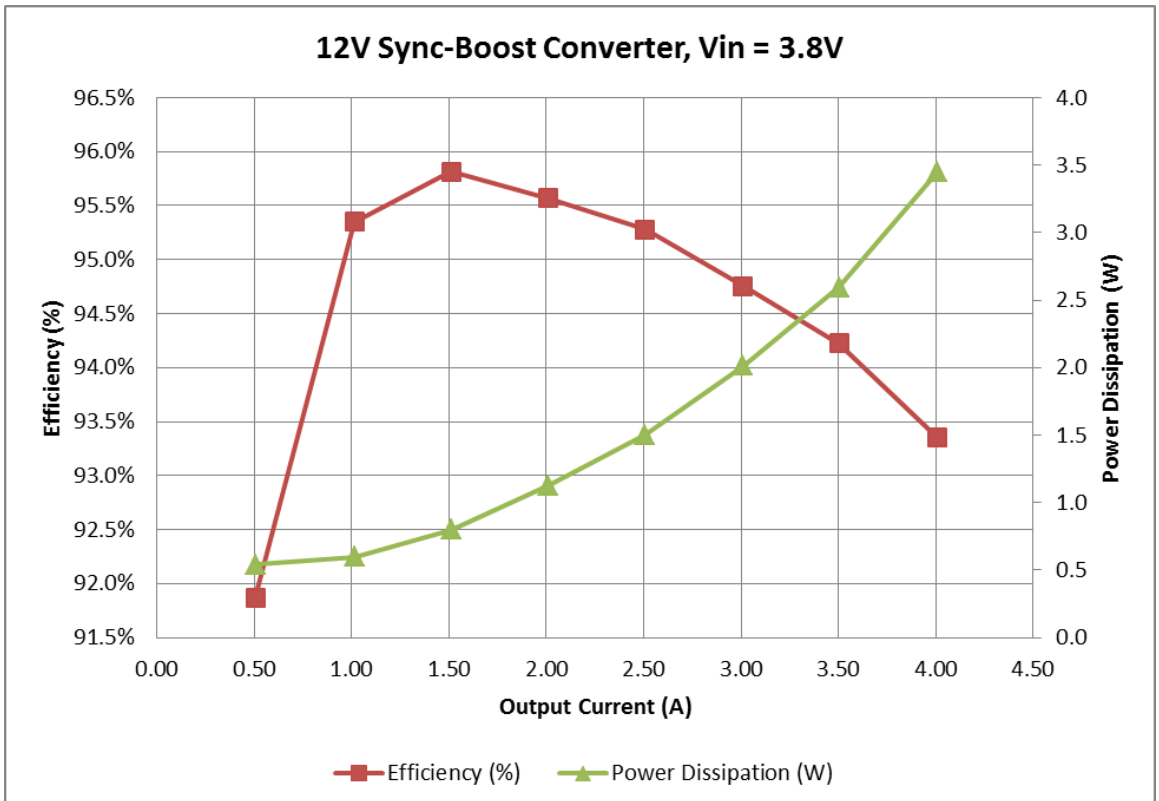


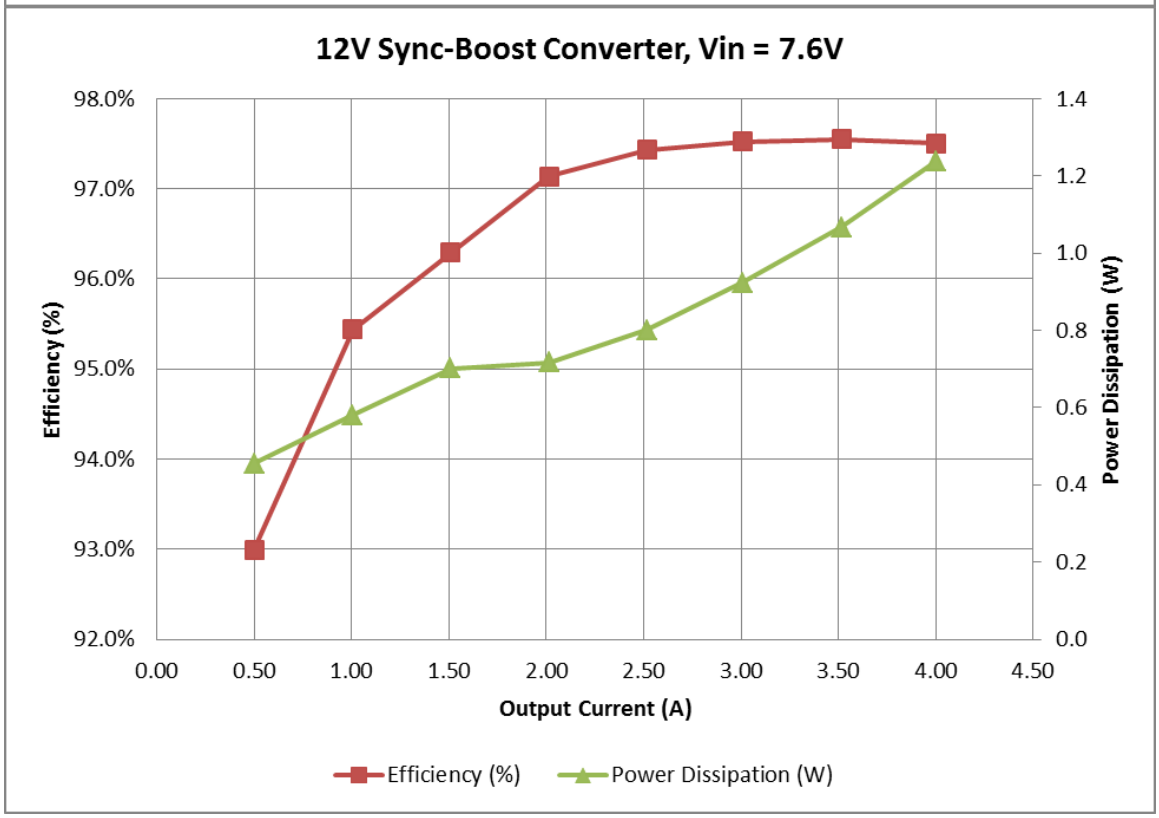
The photo below shows the output voltage startup waveform after the application of 7.6V in. The 12V output was loaded to 4A. (2V/DIV, 5mS/DIV)



2 Efficiency

The 12V sync boost converter efficiency is shown below.

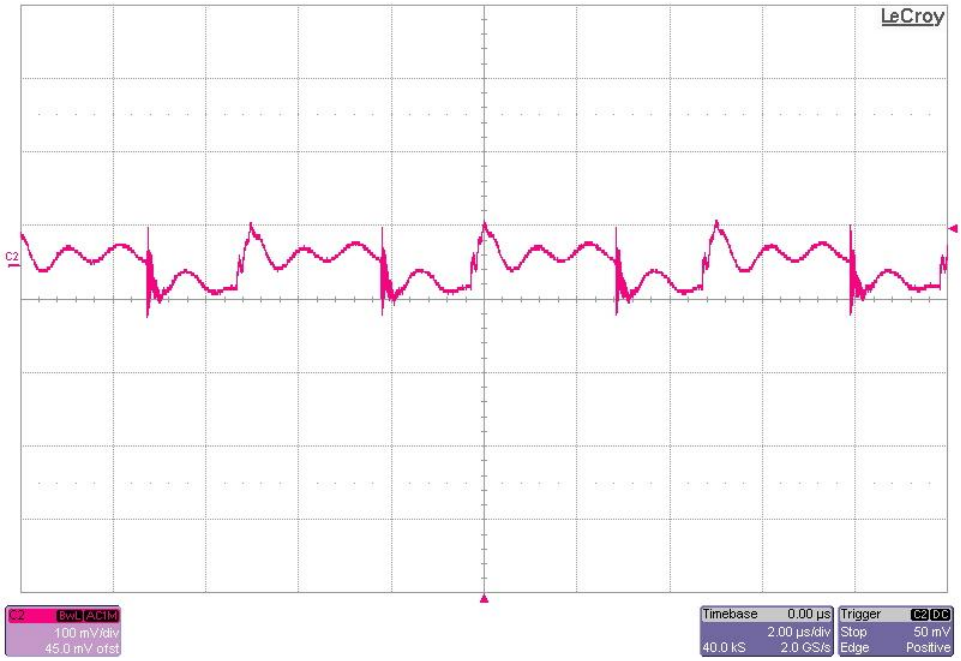




3 Output Ripple Voltage

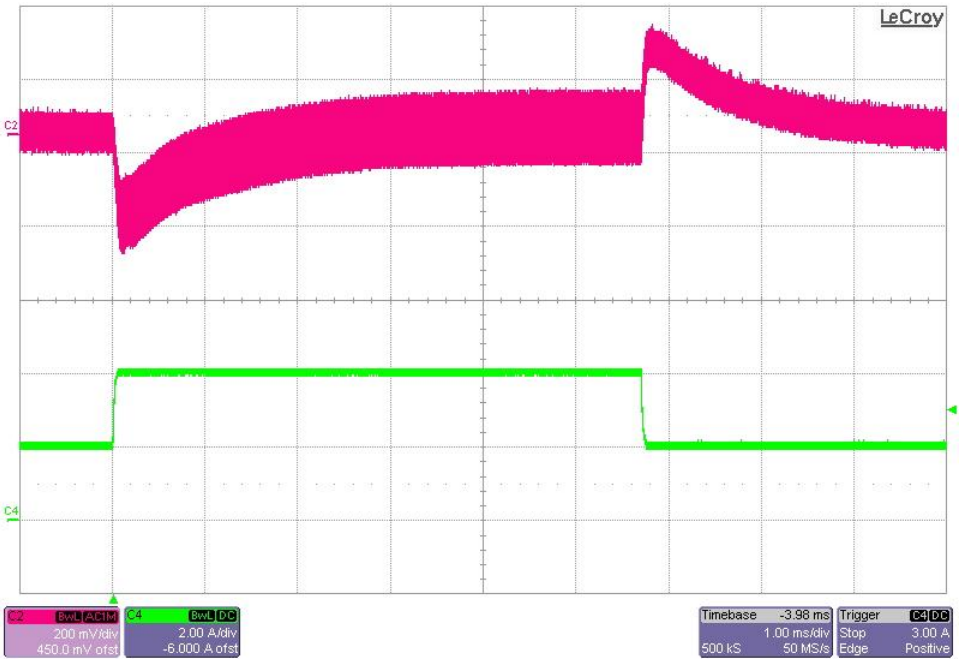
The 12V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 4A. The input voltage is set to 3.8V. (100mV/DIV, 2uS/DIV)

The 12V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 4A. The input voltage is set to 7.6V. (100mV/DIV, 2uS/DIV)

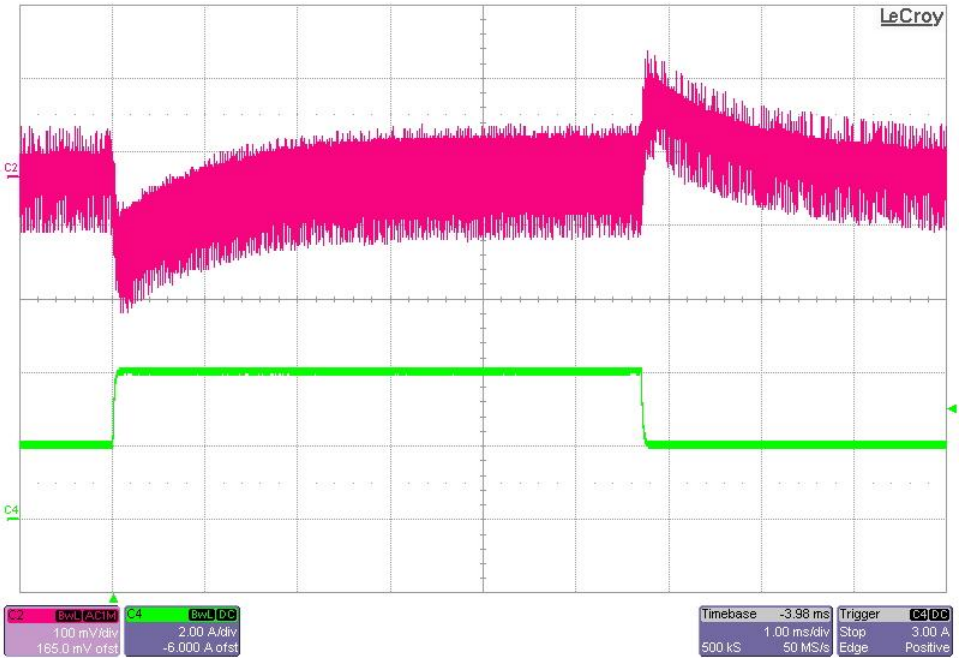


4 Load Transients

The photo below shows the output voltage (ac coupled) when the load current is stepped between 2A and 4A. Vin = 3.8V. (200mV/DIV, 2A/DIV, 1mS/DIV)

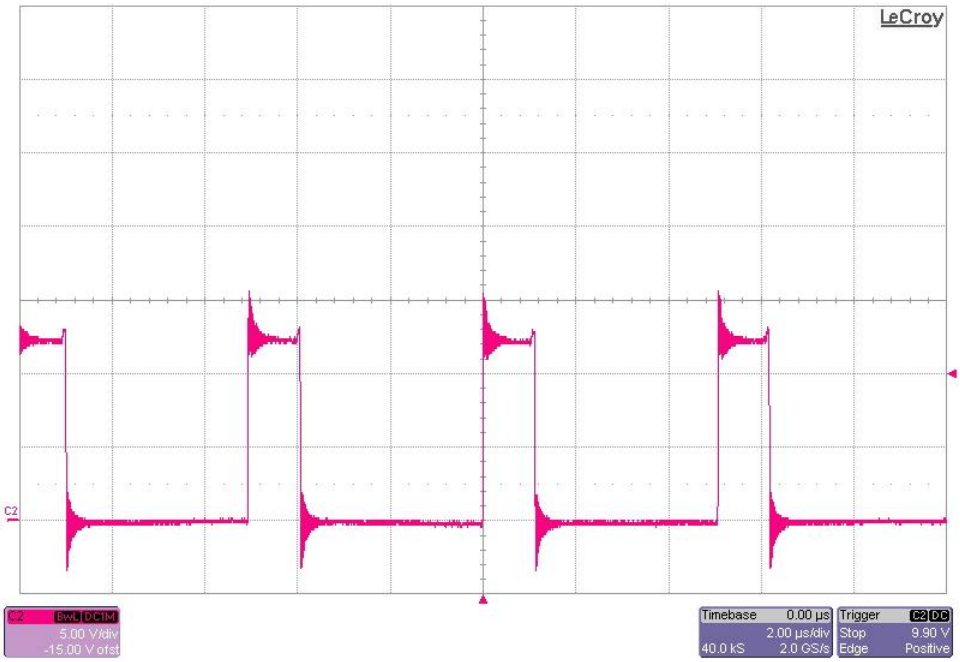


The photo below shows the output voltage (ac coupled) when the load current is stepped between 2A and 4A. Vin = 7.6V. (100mV/DIV, 2A/DIV, 1mS/DIV)

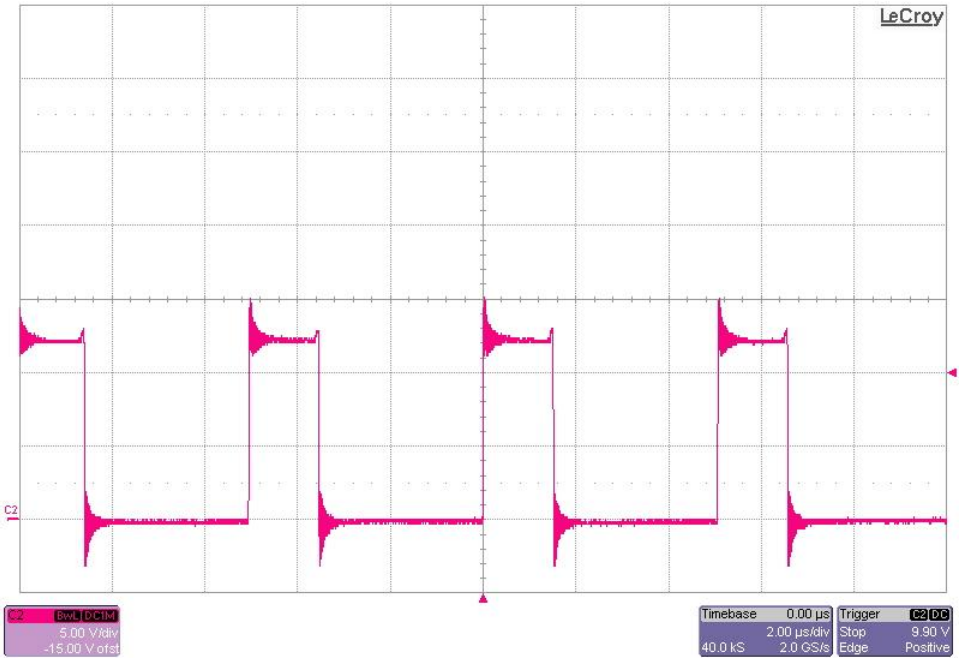


5 Switch Node Waveforms

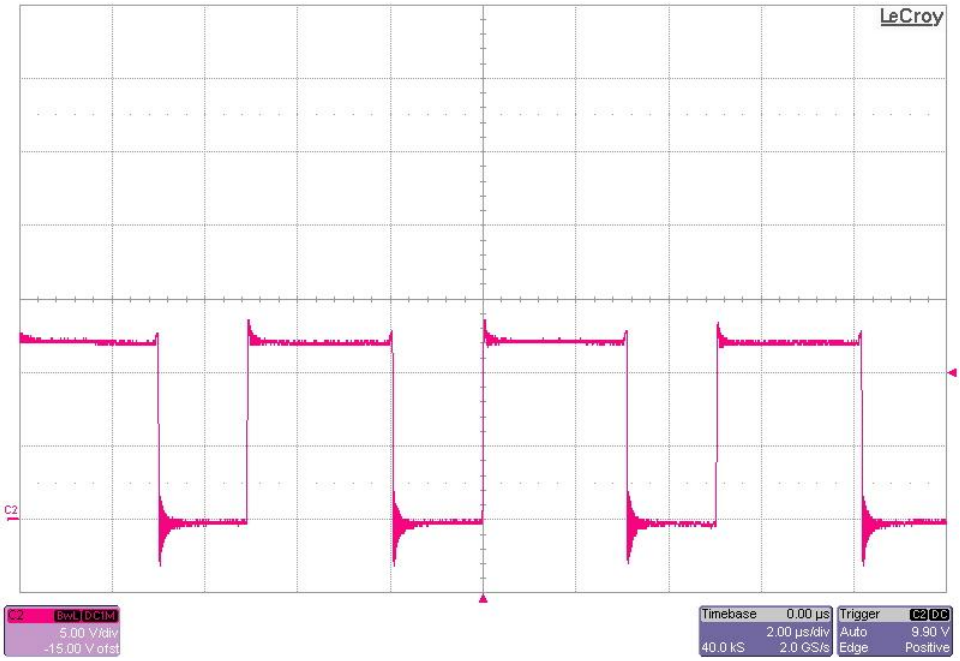
The photo below shows the FET switching voltage. The input voltage is 3.0V and the output is loaded to 4A. (5V/DIV, 2uS/DIV)



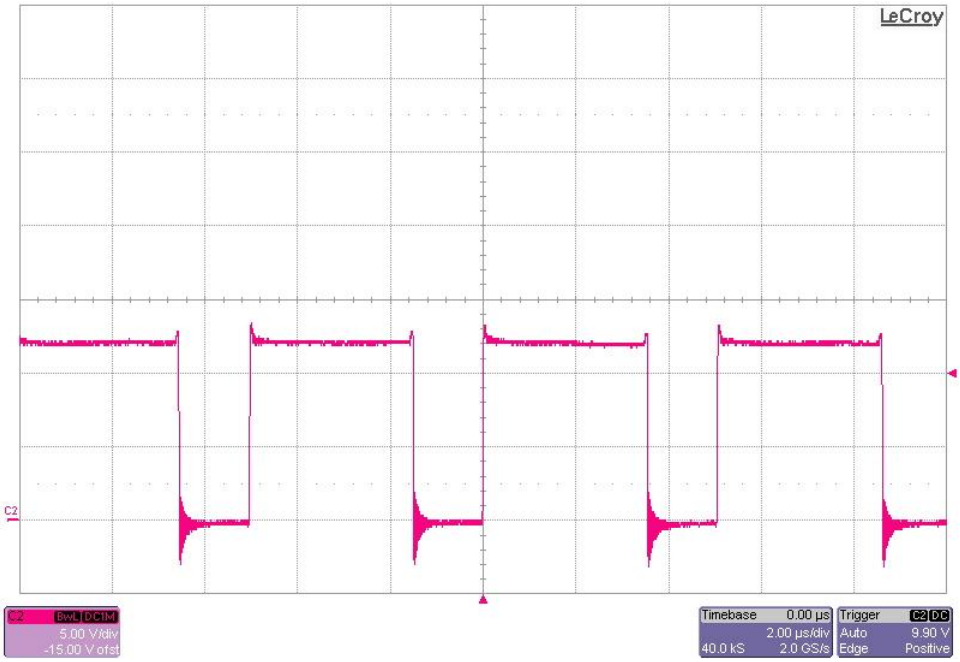
The photo below shows the FET switching voltage. The input voltage is 3.8V and the output is loaded to 4A. (5V/DIV, 2uS/DIV)



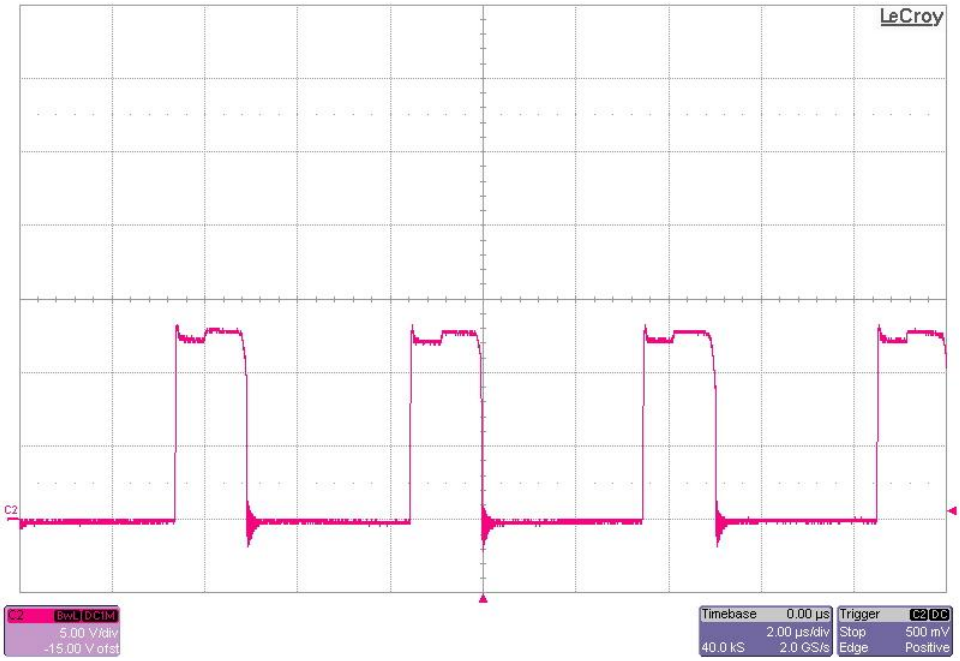
The photo below shows the FET switching voltage. The input voltage is 7.6V and the output is loaded to 4A. (5V/DIV, 2uS/DIV)



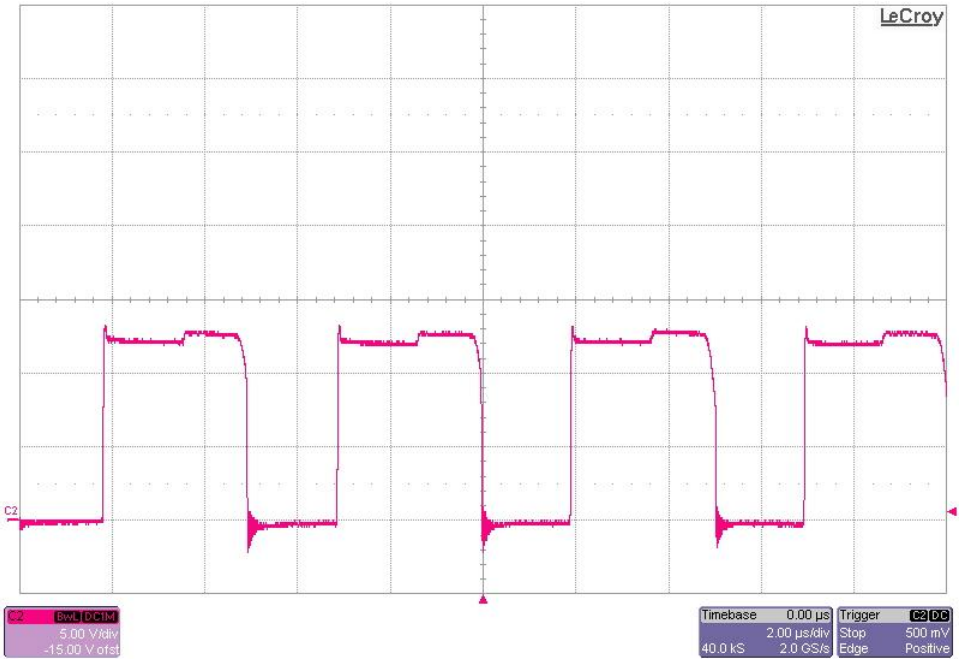
The photo below shows the FET switching voltage. The input voltage is 8.6V and the output is loaded to 4A. (5V/DIV, 2uS/DIV)



The photo below shows the FET switching voltage. The input voltage is 3.8V and the output is loaded to 0.4A. The boost converter is starting discontinuous mode operation. (5V/DIV, 2uS/DIV)



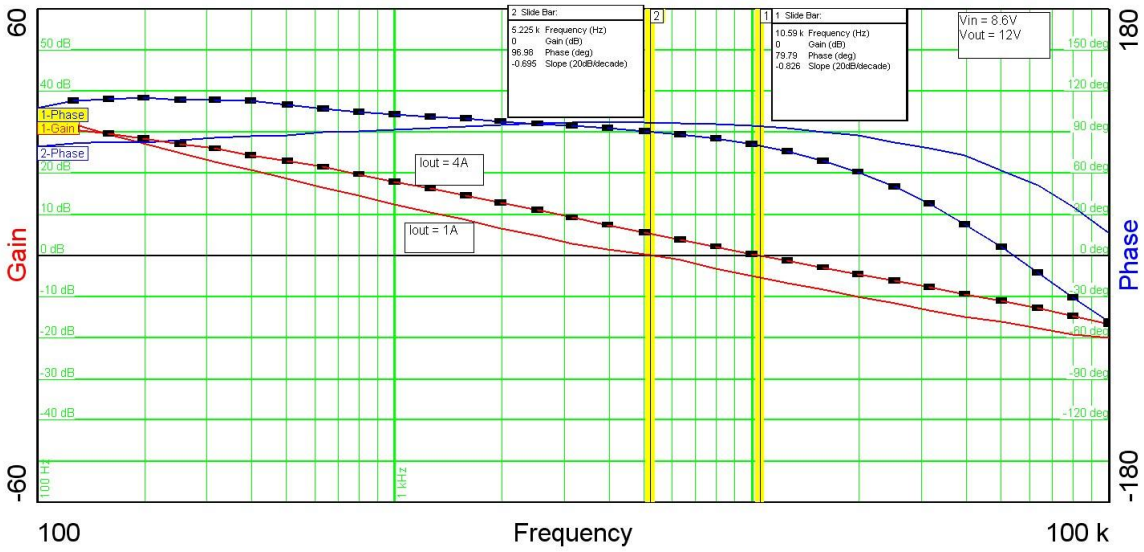
The photo below shows the FET switching voltage. The input voltage is 7.6V and the output is loaded to 1A. The boost converter is starting discontinuous mode operation. (5V/DIV, 2uS/DIV)



6 Control Loop Gain / Stability

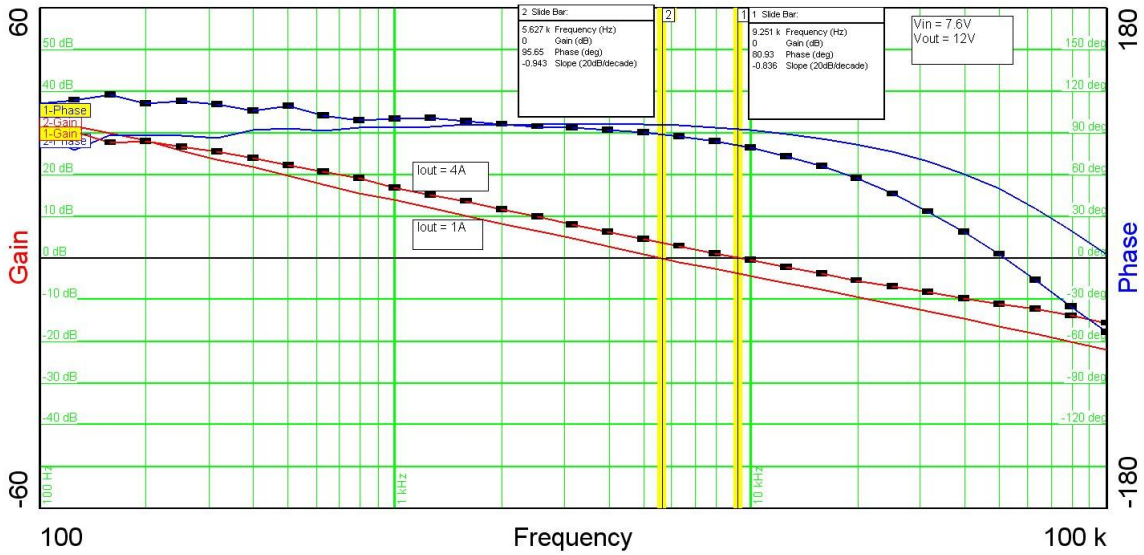
The plot below shows the loop gain and phase margin with the output loaded to 1A and 4A. The input voltage was set to 8.6V.

Band Width = 5.23KHz, Phase Margin = 97 degrees (12V@1A)
Band Width = 10.59KHz, Phase Margin = 80 degrees (12V@4A)



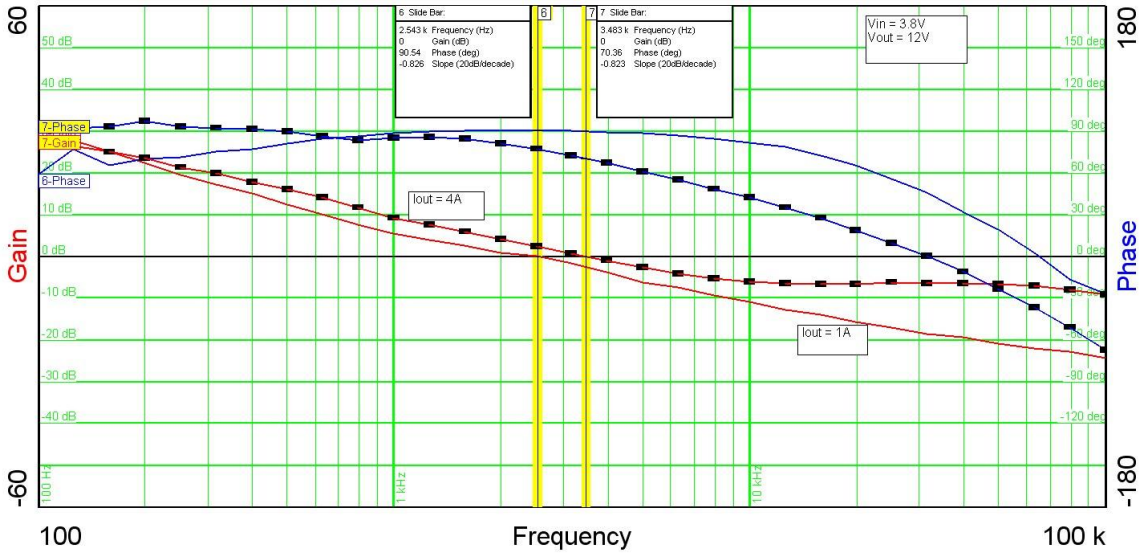
The plot below shows the loop gain and phase margin with the output loaded to 1A and 4A. The input voltage was set to 7.6V.

Band Width = 5.63KHz, Phase Margin = 96 degrees (12V@1A)
Band Width = 9.25KHz, Phase Margin = 81 degrees (12V@4A)



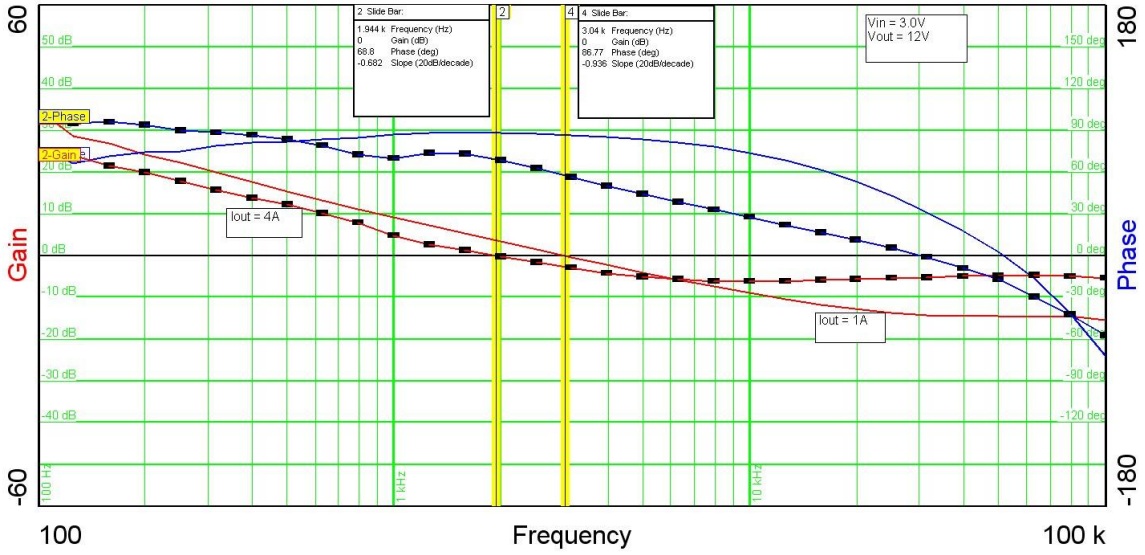
The plot below shows the loop gain and phase margin with the output loaded to 1A and 4A. The input voltage was set to 3.8V.

Band Width = 2.54KHz, Phase Margin = 91 degrees (12V@1A)
Band Width = 3.48KHz, Phase Margin = 70 degrees (12V@4A)



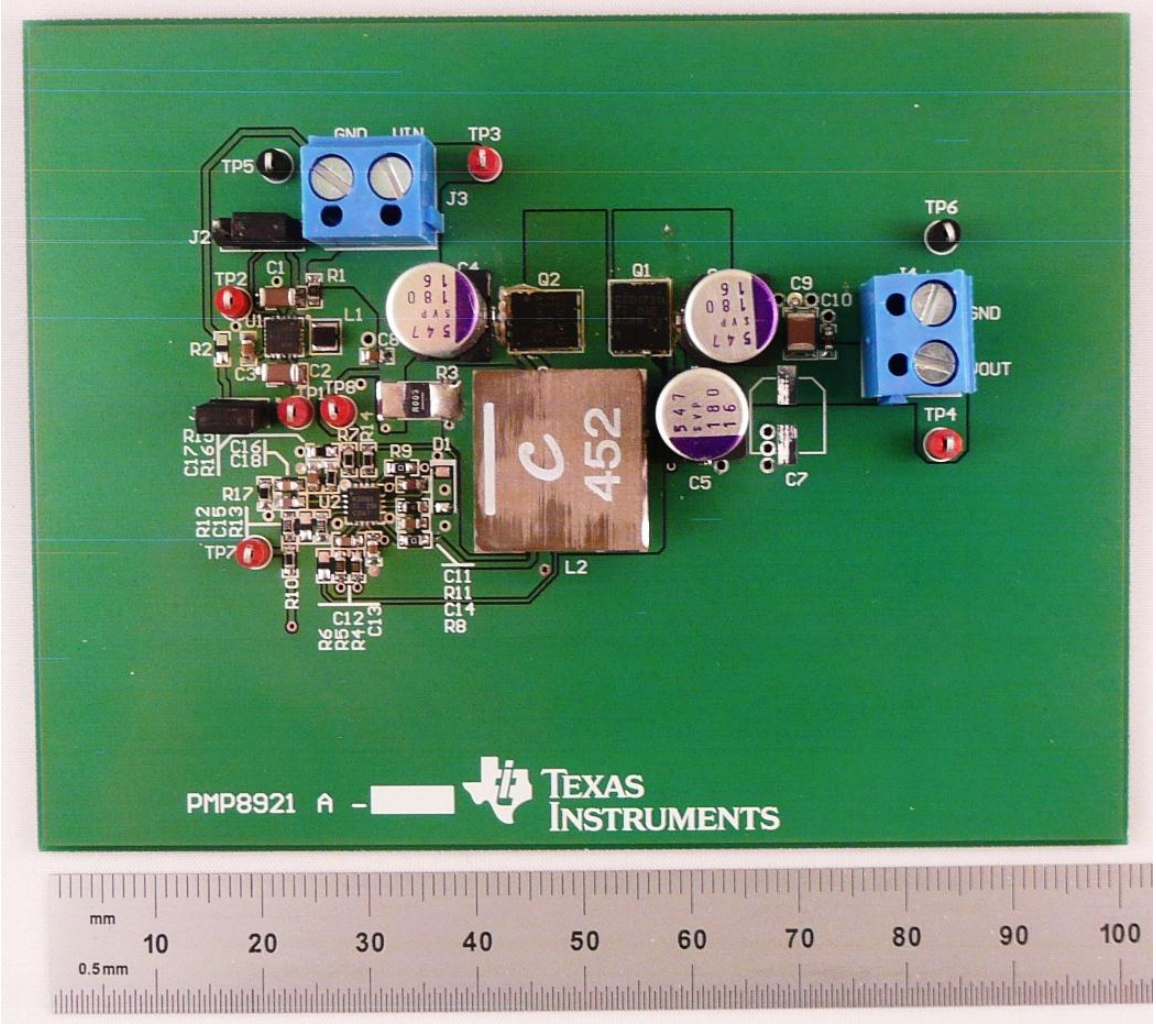
The plot below shows the loop gain and phase margin with the output loaded to 1A and 4A. The input voltage was set to 3.0V.

Band Width = 3.04KHz, Phase Margin = 87 degrees (12V@1A)
Band Width = 1.94KHz, Phase Margin = 69 degrees (12V@4A)



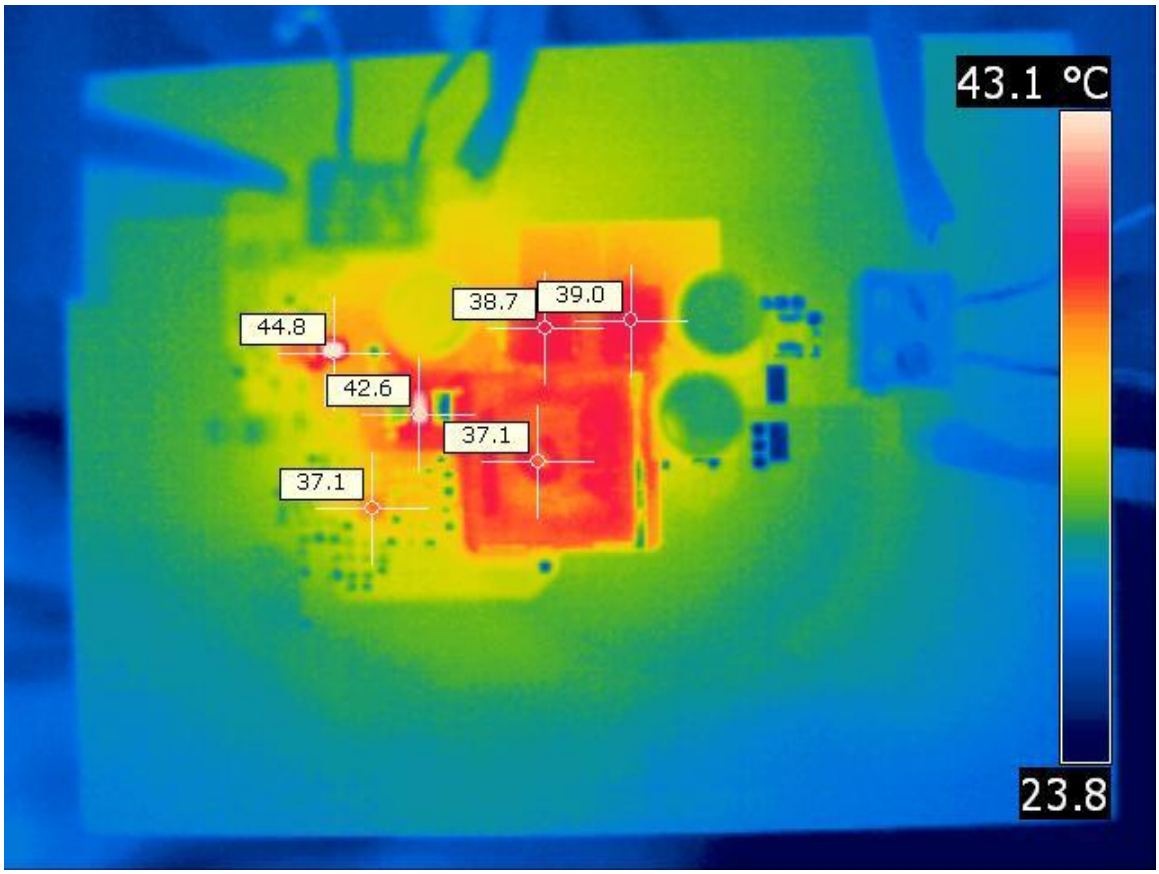
7 Photo

The photo below shows the PMP8921 REVB assy.

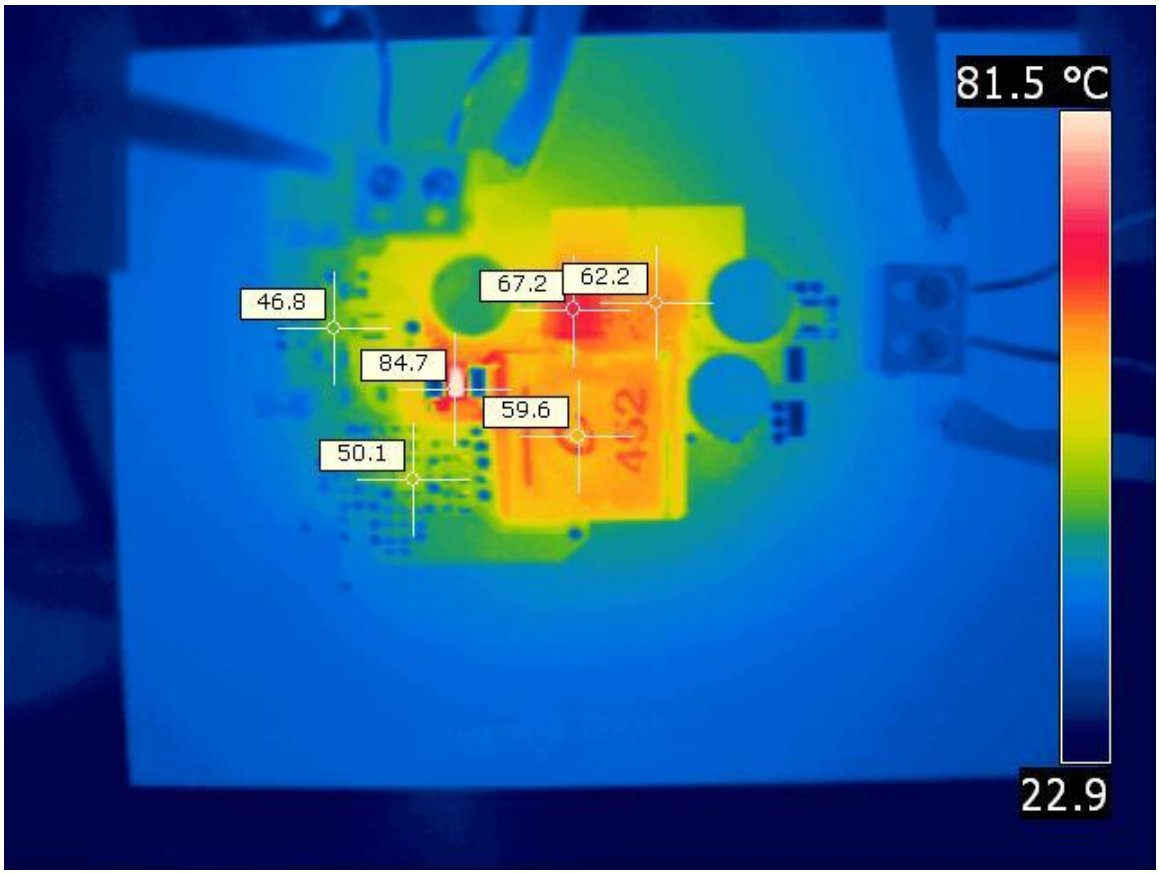


8 Thermal Image

A thermal image is shown below operating at 7.6V input and 4A output (room temp and no airflow).



A thermal image is shown below operating at 3.8V input and 4A output (room temp and no airflow).



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