User's Guide

SLVUAA8–September 2014

TPS68470EVM

This user's guide describes the characteristics, operation, and use of the TPS68470EVM evaluation module (EVM). This EVM is designed to help evaluate and test the various operating modes of the TPS68470. The user's guide includes hardware/software/power-on setup instructions, setup for common tests with accompanying data, a schematic diagram and printed-circuit board (PCB) layout drawings, and a bill of materials (BOM) for the evaluation module.

Contents

List of Figures

List of Tables

1 Introduction

The TPS68470 device is an advanced power management IC that powers a Compact Camera Module (CCM), generates the clock for the image sensor, drives a dual LED for flash, and incorporates two LED drivers for general-purpose indicators. The TPS68470 is capable of generating all needed power rails in a CCM. The device contains a state-of-the-art buck converter, a high-efficiency boost converter, seven LDOs (programmable output voltages), seven GPIOs, clock generation (programmable PLL, 24-MHz crystal oscillator), and the module is controlled via an I2C interface.

1.1 Related Documentation from Texas Instruments

Datasheet: TPS68470, Power Management IC for Compact Camera Module Applications (SLVSCJ1).

1.2 Required Equipment

In order for this EVM to operate properly, the following components must be connected and properly configured:

1.2.1 Personal Computer (PC or Laptop)

A computer with a USB port is required to operate this EVM. The TPS68470 graphical user interface (GUI), which run on a PC, communicates with the EVM via the PC USB port. Commands can be sent to the EVM and can read the contents of the internal registers.

1.2.2 Printed-Circuit Board Assembly

The TPS68470EVM PCB contains the IC and its required external components. This board contains several jumpers, switches, and connectors that allow customization of the board for specific operating conditions.

1.2.3 USB to I^2C Adapter (with Accompanying Cables)

The USB2ANY (HPA665) box is the link that allows the PC and the EVM to communicate. The adapter connects to the PC with the supplied USB to USB mini cable on one side and to the EVM through the supplied ribbon cable on the other. When a command is written to the EVM, the GUI sends the command to the PC USB port. The adapter receives the USB command and converts the signal to an I^2C protocol. It then sends the signal to the TPS68470 board. When a status register is read from the EVM, the PC sends a command to read a register on the EVM. When the EVM receives the command, it reports the status of the register via the interface. The adapter receives the information on the interface, converts it to a USB protocol, and then sends it to the PC.

1.2.4 Device Software

TI provides software to assist with EVM evaluation. The required software to give commands to the EVM is the TPS68470EVM GUI. Default installation settings provide a shortcut to the GUI start-up on the desktop.

1.2.5 Lab Equipment

In order to power on and properly evaluate the device, standard electrical lab equipment must be used. This includes:

- Two power supplies, each capable of output voltage 5 V and up to 4 A
- Source meter capable of output voltage 3.3 V with 4-wire sense mode
- Electronic current load capable of output loads up to 4 A
- Digital multimeter (DMM) capable of accurately measuring voltages 0–10 V, or beyond
- Several probes and cables for supply, source meter, load, and DMM use
- Oscilloscope, 2 channels or higher, 300 MS/s sampling or higher, at least 1 voltage and 1 current probe
- Mini flathead screwdriver
- Color-coded wires (red and black preferred), recommended AWG: 20 gauge
- Wire cutters/strippers

1.3 EVM Warnings and Restrictions

This EVM is intended for use for engineering development, demonstration, or evaluation purposes only. Persons handling the product must have electronics training and observe good engineering practice standards. Before operation of device, please read the following warnings.

1.3.1 Input and Output Voltage Ranges

It is important to operate this EVM within the input voltage range of 2.97 V to 3.63 V and the output voltage ranges specified in the TPS68470 datasheet (SLVSCJ1). Exceeding the specified input range may cause unexpected operation or irreversible damage to the EVM. Likewise, applying loads outside of the specified output range may result in unintended operation or possible permanent damage to the EVM. If there is any uncertainty as to the input voltages and load specifications, contact a TI field representative.

1.3.2 Electrostatic Discharge (ESD)

This device has ESD sensitive components. Before evaluating the board, ensure the environment is ESD safe and only persons who are properly trained to handle ESD sensitive devices are performing the tests and evaluations.

2 Setup

2.1 Hardware

The following section describes default hardware settings that must be established for the EVM to operate. Figure 1 illustrates a fully-configured device.

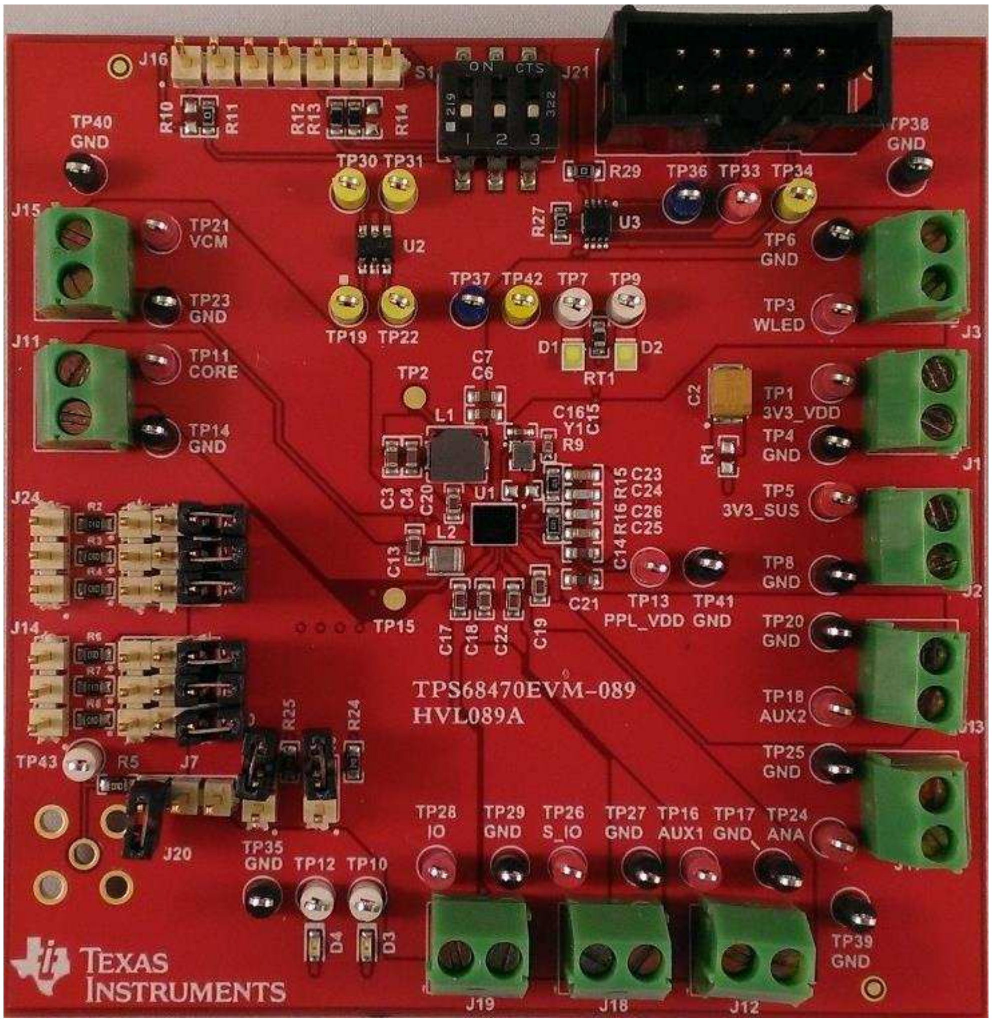

Figure 1. TPS68470 EVM

The TPS68470 EVM is placed in correct orientation, color-coded wires are placed on J1 and J2 properly (red to power, black to ground) with power supply probes attached, all jumpers are placed in default setting, all switches are in their default mode, and the USB2ANY cable is properly connected to J21.

2.1.1 Default Jumper Settings

By default, no jumper connections are required for all of the standard features to operate. Spare jumpers are placed on J4–J10, J22, and J23 in case any modifications are desired.

2.1.2 Default Switch Settings

Ensure the switches on S1 are configured as follows:

- S1A (RESET_IN) should be flipped low (down when viewed from the correct orientation)
- S1B (S_VSYNC) should be flipped low (down when viewed from the correct orientation)
- S1C (S_STROBE) should be flipped high (up when viewed from the correct orientation)

2.1.3 USB2ANY Connection

Connect the USB to USB mini cable from the PC or laptop's USB port to the USB2ANY (HPA665) box and allow the computer to install the drivers automatically. Next, connect the ribbon cable at the other end of the interface box to the EVM on J21.

2.1.4 Input Power Wires

Always connect the power supply to the screw terminal and **not** the test points (labeled TP, followed by a number). Place wires (keep the wires around 1 inch in length, stripped about 1 cm on both ends) in the J1 and J2 terminals (use a flathead mini screwdriver to loosen and tighten). Be sure to strip enough of the wire so that a good connection is made with the terminal and the conductive material, and enough space is left over on the other end for power probes. Connect the red wire on the power side (indicated next to the red TP, also the first connection point from the top of the screw terminal) and the black wire to the ground terminal of the junction. Refer to Figure 1.

2.2 Power-On

The following sections describe the proper way to power on and off the TPS68470EVM. The two input power rails are 3V3_SUS and 3V3_VDD:

2.2.1 3V3_SUS

Set the power supply to 3.3 V and while the supply is off, connect it to 3V3_SUS on J2. Remember to connect the probes in the correct order (power is on the red TP side of the J2 terminal and ground is on the black TP side of the J2 terminal) to the wires.

2.2.2 3V3_VDD

Set the power supply to 3.3 V, and while the supply is off, connect it to 3V3_VDD on J1. Remember to connect the probes in the correct order (power is on the red TP side of the J1 terminal and ground is on the black TP side of the J1 terminal) to the wires.

2.2.3 Power-on Sequence

A proper power-on sequence begins with turning on 3V3_SUS, then turning on 3V3_VDD. They may be turned on at the same time; however, do not turn on 3V3_VDD first. Doing so may damage the device.

2.2.4 Power-off Sequence

A proper power-off sequence begins with turning off 3V3_VDD, then turning off 3V3_SUS. They may be turned them off at the same time; however, do not turn off 3V3_SUS first. Doing so may damage the device.

2.3 Software

Power on the device as per Section 2.2 and run the TPS68470EVM GUI (default installation settings place a shortcut on the desktop). Before writing commands to the EVM, study the GUI overview in Section 2.3.1.

2.3.1 GUI Overview

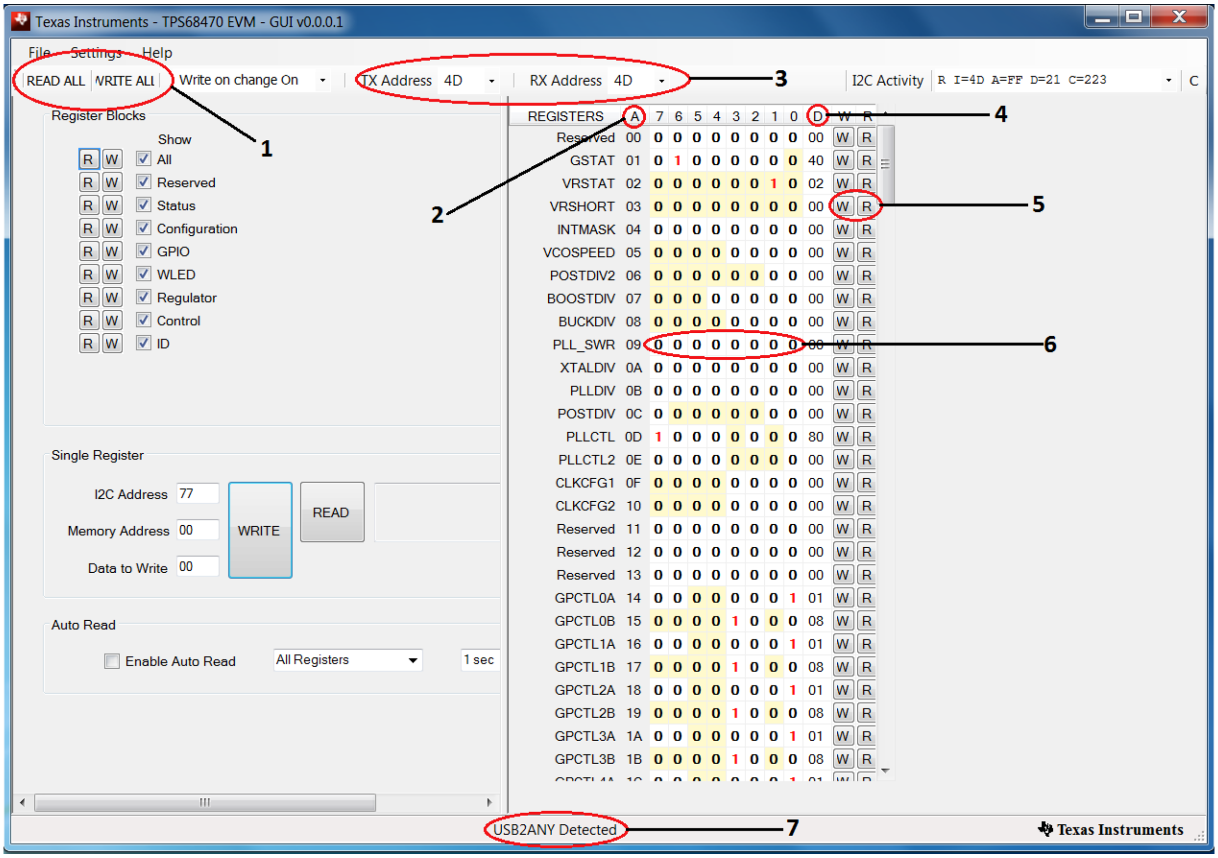

Figure 2. TPS68470EVM Graphical User Interface Layout

1. *READ ALL* and *WRITE ALL* buttons, read and write to all register bits, respectively. Use *READ ALL* occasionally to check whether the I^2C still has a successful connection. Refer to Section 3.6 on how to check for a successful I^2C connection.
2. The *Register Address* column displays the address for the registers.
3. *I2C Addresses:* Make sure these addresses read *'4D'*. If not, set *TX Address* and *RX Address* to *'4D'*.
4. The *Data* column controls the bit settings. Enter the settings required for the register in HEXADECIMAL format here, then select *'W'* to write.
5. *'W'* and *'R'* buttons write and read the bits of that register, respectively.
6. *Binary data bits* are the bits for each register. Hover briefly over any bit to display what function it controls. Click individual bits to change from *'0'* to *'1'* and vice versa.
7. *Connection Status:* Make sure this reads *'USB2ANY Detected'* to determine if the computer successfully detects the USB2ANY box.

Once the device is powered on, connected to the computer through the USB2ANY box, and the GUI is up and running, check for a solid I^2C connection. To ensure that a proper connection has been established between the GUI and device, check that the register *REVID* (address 0xFF) has a bit setting of 0x21 (remember, bit settings are shown in the D, or *Data* column).

3 Common Tests

Once a proper setup (hardware, software, power-on, I^{2}C connection) has been established, explore the various features of the TPS68470EVM by writing commands to the GUI registers. The following sections detail general tests for testing the operation of the EVM. The examples assume the device is properly powered on and the GUI is running. TI recommends doing a power cycle (power-off, power-on) before each test.

3.1 Voltage Regulator Functionality

The TPS68470 includes a buck and a boost regulator, as well as seven other LDOs, all with programmable output voltages specified via the GUI.

3.1.1 Buck

The programmable voltage rail (VR) output voltage range is from 0.9 V to 1.95 V, with 25-mV increments. Refer to Figure 3 for the voltage codes.

To enable the Buck converter, use the following guide:

- On the GUI, set VDCTL (address 0x48) bit 2 to *'0'* and bit 0 to *'1'* (enables the buck converter, sets clock control to internal oscillator)
- Choose an output voltage from 0.9 V to 1.95 V the range specified above by programming VDVAL (address 0x42). For this example, set the buck to 1.775 V.
- Set VDVAL (address 0x42) bit settings to 0x23 (sets output voltage to 1.775 V)
- Measure the voltage across CORE on TP11 and TP14 (GND), and verify the output voltage is now 1.775 V

Bit Definition		
The VR output voltage range is from 0.9 V to 1.95 V for codes 0x00 to 0x2A in increments of 25 mV. Codes above 0x2A will yield a 1.95-V output.		
0x00 : 0.9V	0x10 : 1.295V	0x20 : 1.695V
0x01 : 0.922V	0x11 : 1.322V	0x21 : 1.726V
0x02 : 0.949V	0x12 : 1.350V	0x22 : 1.742V
0x03 : 0.973V	0x13 : 1.369V	0x23 : 1.774V
0x04 : 0.999V	0x14 : 1.399V	0x24 : 1.790V
0x05 : 1.025V	0x15 : 1.420V	0x25 : 1.824V
0x06 : 1.048V	0x16 : 1.452V	0x26 : 1.842V
0x07 : 1.071V	0x17 : 1.474V	0x27 : 1.878V
0x08 : 1.096V	0x18 : 1.497V	0x28 : 1.897V
0x09 : 1.121V	0x19 : 1.521V	0x29 : 1.915V
0x0A : 1.148V	0x1A : 1.545V	0x2A : 1.954V
0x0B : 1.176V	0x1B : 1.571V	0x2B : 1.954V
0x0C : 1.198V	0x1C : 1.597V	...
0x0D : 1.221V	0x1D : 1.624V	0x3E : 1.954V
0x0E : 1.245V	0x1E : 1.652V	0x3F : 1.954V
0x0F : 1.269V	0x1F : 1.666V	

Figure 3. List of Programmable Voltage Codes for CORE (Buck)

3.1.2 Boost

The programmable output voltage in voltage mode is from 3.68 V to 5.48 V in 120-mV steps. Refer to Figure 4 for the voltage codes. Only the last 4 bits are programmable (bit 3,2,1,0).

To enable the Boost regulator, use the following guide:

- On the GUI, set VWLEDCTL (address 0x31) bit 3 to *'0'*, bit 2 to *'1'*, and bit 0 to *'1'* (sets clock control to internal oscillator, sets constant output voltage mode, and enables the boost regulator)
- Choose an output voltage from 3.68 V to 5.48 V, the range specified above, by programming VWLEDVAL (address 0x2B). For this example, the boost is set to 5.48 V.
- Set VWLEDVAL (address 0x2B) bit settings to 0x0F (sets output voltage to 5.48 V)
- Measure the voltage across WLED on TP3 and TP6 (GND), and verify the output is now 5.48 V

Bit Definition	
Boost output voltage in voltage mode, 120-mV steps	-
0000 : 3.68V	1000 : 4.64V
0001 : 3.80V	1001 : 4.76V
0010 : 3.92V	1010 : 4.88V
0011 : 4.04V	1011 : 5.00V
0100 : 4.16V	1100 : 5.12V
0101 : 4.28V	1101 : 5.24V
0110 : 4.40V	1110 : 5.36V
0111 : 4.52V	1111 : 5.48V

Figure 4. List of Programmable Voltage Codes for WLED (Boost)

3.1.3 LDOs

There are seven LDOs featured on the TPS68470EVM. Refer to Table 1 for the registers that correspond to each LDO on the GUI, and refer to Table 2 for the voltage level codes. Before turning on the LDOs, the device must be powered on as per Section 2.2.

Table 1. LDO Registers and Actions for Turn-On

LDO	Register w/Address	Action	Result
LDO_PLL (TP13 and TP14)	PLLCTL (0x0D)	Set bit 0 to 1	Enables the LDO (2.7 V)
LDO_IO (TP28 and TP29)	VIOVAL (0x3F)	Refer to Table 2 for voltage codes	Sets output voltage to corresponding value from code
LDO_VCM (TP21 and TP23)	VCMCTL (0x44)	Set bit 0 to 1	Enables the LDO
	VCMVAL (0x3C)	Refer to Table 2 for voltage codes	Sets output voltage to corresponding value from code
LDO_AUX1 (TP16 and TP17)	VAUX1CTL (0x45)	Set bit 0 to 1	Enables the LDO
	VAUX1VAL (0x3D)	Refer to Table 2 for voltage codes	Sets output voltage to corresponding value from code
LDO_AUX2 (TP18 and TP20)	VAUX2CTL (0x46)	Set bit 0 to 1	Enables the LDO
	VAUX2VAL (0x3E)	Refer to Table 2 for voltage codes	Sets output voltage to corresponding value from code
LDO_S_IO (TP26 and TP27)	S_I2C_CTL (0x43)	Set bit 1 to 1	Enables the LDO
	VSIOVAL (0x40)	Refer to Table 2 for voltage codes	Sets output voltage to corresponding value from code
LDO_ANA (TP24 and TP25)	VACTL (0x47)	Set bit 0 to 1	Enables the LDO
	VAVAL (0x41)	Refer to Table 2 for voltage codes	Sets output voltage to corresponding value from code

Table 2. Voltage Codes for LDOs

Bit Definition
The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV
0x00 : 0.875V
0x01 : 0.8928V
...
0x7C : 3.082V
0x7D : 3.10V

3.2 Efficiency

The TPS68470 includes high-efficiency Buck and Boost converters. The Buck automatically enters PFM mode at low currents (< 80 mA) to conserve power and raise efficiency.

3.2.1 Buck

Use the following steps for an efficiency setup for the Buck converter. Refer to Figure 5 for a proper efficiency setup. Record the measurements in a spreadsheet format.

1. With everything powered off, connect a source meter (4-wire sense) in series with a DMM current meter (Iin) to 3V3_VDD. Connect the source probes to their usual location (on the wires on the screw terminal) and connect the sense wires to the test points [TP1 and TP4 (GND)].
2. Place red and black stripped and cut wires on the CORE screw terminal, similar to the input power rails. Connect the output wire (red) of CORE in series with a DMM current meter **(Iout)** to an electronic load. If the electronic load has 4-wire sense mode, place the sense wires on the test points [TP11 and TP14 (GND)].
3. Place DMM probes on the test points across 3V3_VDD (TP1, TP4) **(Vin)** and the test points across CORE (TP11, TP14) **(Vout)**.

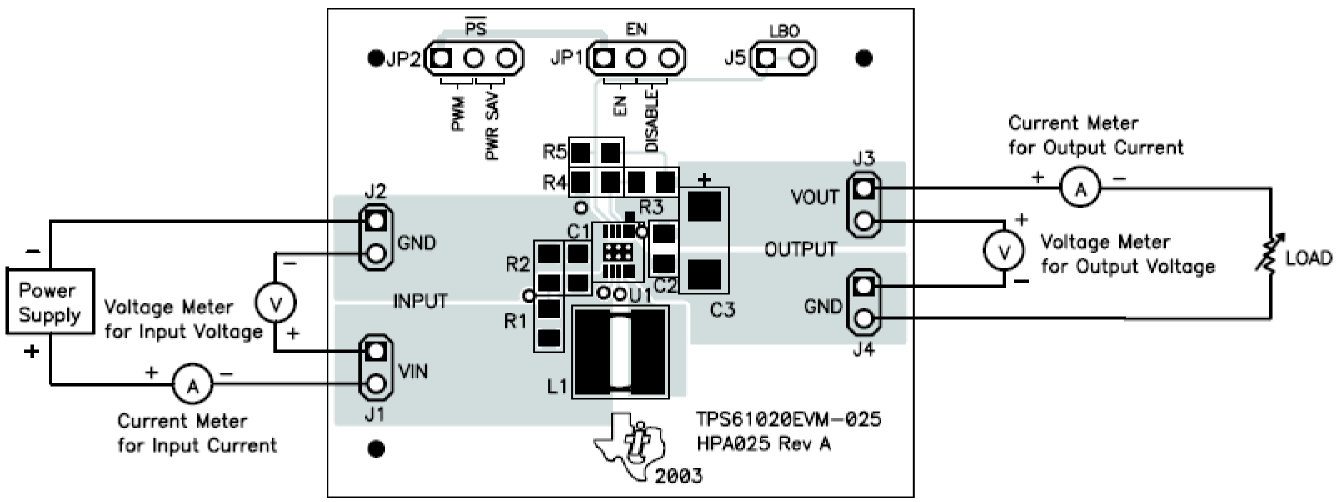

Figure 5. Recommended Efficiency Setup

4. Power on the device (refer to Section 2.2). With the Buck not enabled yet, record the input current (Iin), this is the non-buck Iq. Subtract the non-buck Iq from the subsequent input currents with the Buck enabled for accurate measurements.
5. Enable the Buck by setting VDCTL (address 0x48) bit 2 to *‘0’* and bit 0 to *‘1’*.
6. Choose the output voltage (see Figure 3) and set VDVAL (address 0x42) to that value.

7. Turn on the electronic load and record the measurements (Vin, Vout, In, Iout). TI recommends stepping-up the load by 10-mA increments, up till 100 mA (to accurately record PFM performance) and then up till 500 mA in 100-mA increments. Do not exceed a 500-mA load. The Buck features an internal current limit to protect the device.

$$\text{Efficiency}(\%) = \frac{\text{Vout} \times \text{Iout}}{\text{Vin} \times \text{Iin}} \times 100 \tag{1}$$

8. After recording the results, power off the load and power off the device.

3.2.2 Boost

Use the following steps for an efficiency setup for the Boost converter. Refer to Figure 5 for a proper efficiency setup. TI recommends recording measurements in a spreadsheet format.

1. With everything powered off, connect a source meter (4-wire sense) in series with a DMM current meter **(Iin)** to 3V3_VDD. Connect the source probes to their usual location (on the wires on the screw terminal) and connect the sense wires to the test points (TP1 and TP4 (GND)).
2. Place red and black stripped and cut wires on the WLED screw terminal, similar to the input power rails. Connect the output wire (red) of WLED in series with a DMM current meter **(Iout)** to an electronic load. If your electronic load has 4-wire sense mode, place the sense wires on the test points (TP3 and TP6 (GND)).
3. Place DMM probes on the test points across 3V3_VDD **(Vin)** and the test points across WLED **(Vout)**.
4. Power on the device (as detailed in Section 2.2).
5. Enable the Boost by setting VWLEDCTL (address 0x31) bit 3 to *'0'*, bit 2 to *'1'*, and bit 0 to *'1'*.
6. Choose the output voltage (see Figure 4) and set VWLEDVAL (address 0x2B) to that value.
7. Turn the electronic load on and record the measurements using appropriate increments for Iout.
8. Refer to Equation 1 in Section 3.2.1 to calculate efficiency.
9. When through recording the results, power off the load and then power off the device.

3.3 Voltage Ripple

Voltage ripple measurements on the TPS68470EVM should be taken with the probe directly in contact with the input and output capacitors. Use a small ground ring to minimize loop area and therefore reduce noise. Refer to *Understanding, Measuring, and Reducing Output Voltage Ripple*.

3.3.1 Buck

Once the ripple measurement is setup, the device is powered on, and the specified load is in the CORE screw terminal, place the voltage probe across C1 to see the input voltage ripple and C13 for the output voltage ripple. Figure 6 through Figure 9 show the buck ripple at no load and at 500-mA load, as specified by the captions.

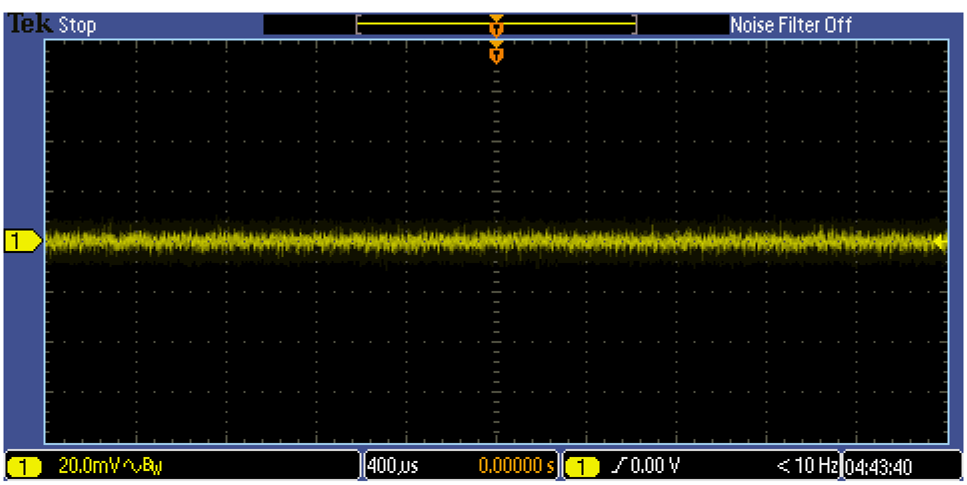

Figure 6. Buck Input Ripple with No Load

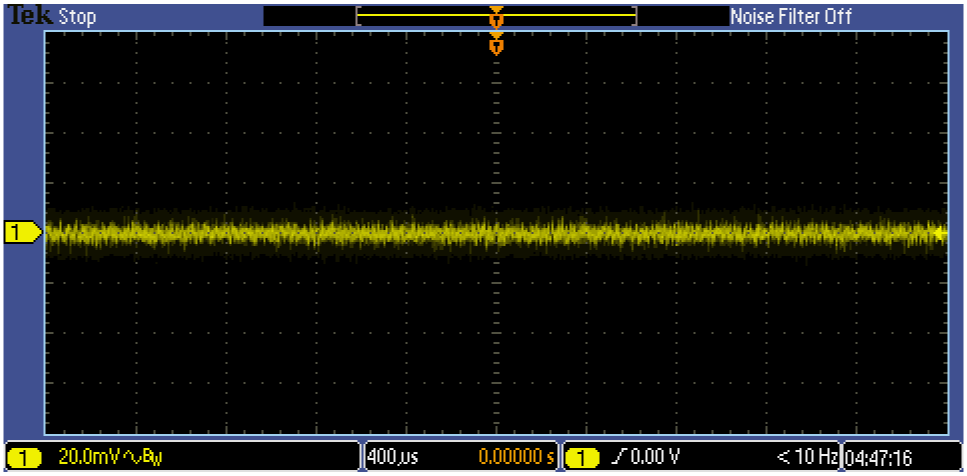

Figure 7. Buck Input Ripple with 500-mA Load

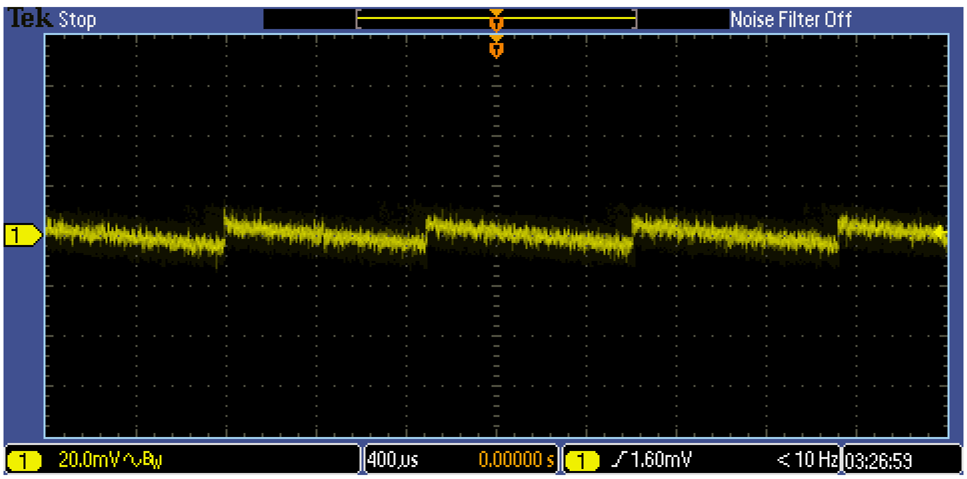

Figure 8. Buck Output Ripple with No Load

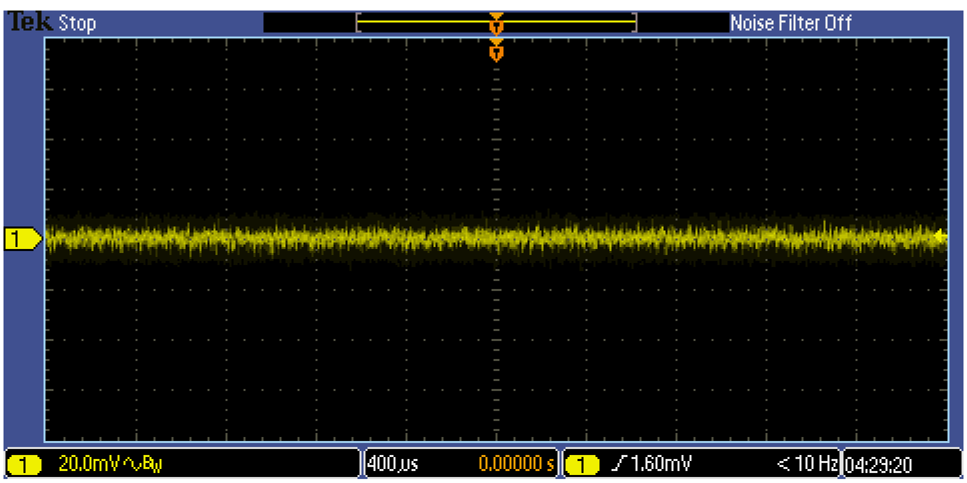

Figure 9. Buck Output Ripple with 500-mA Load

3.3.2 Boost

Once the ripple measurement is set up, the device is powered on, and the specified load is in the WLED screw terminal, place the voltage probe across C4 to see the input voltage ripple and C6 for the output voltage ripple. Figure 10 through Figure 13 show the boost ripple at no load and at 500-mA load, as specified by the captions.

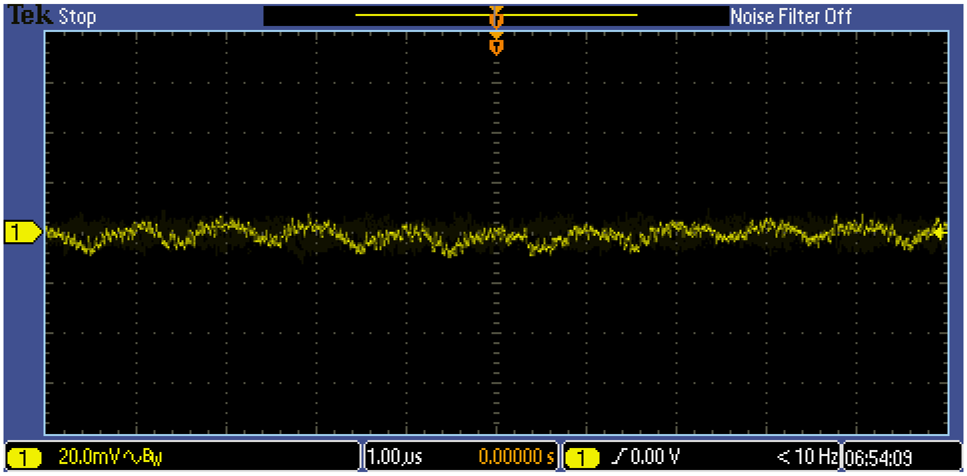

Figure 10. Boost Input Ripple with No load

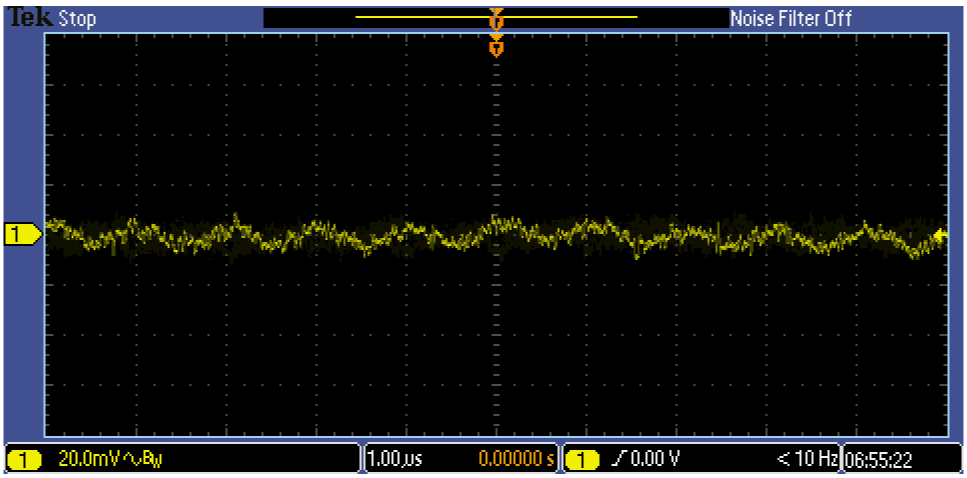

Figure 11. Boost Input Ripple with 500-mA Load

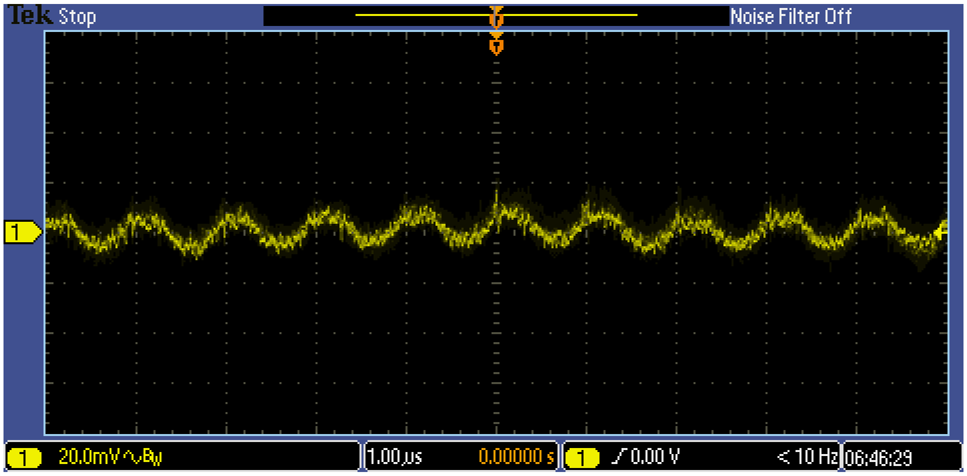

Figure 12. Boost Output Ripple with No Load

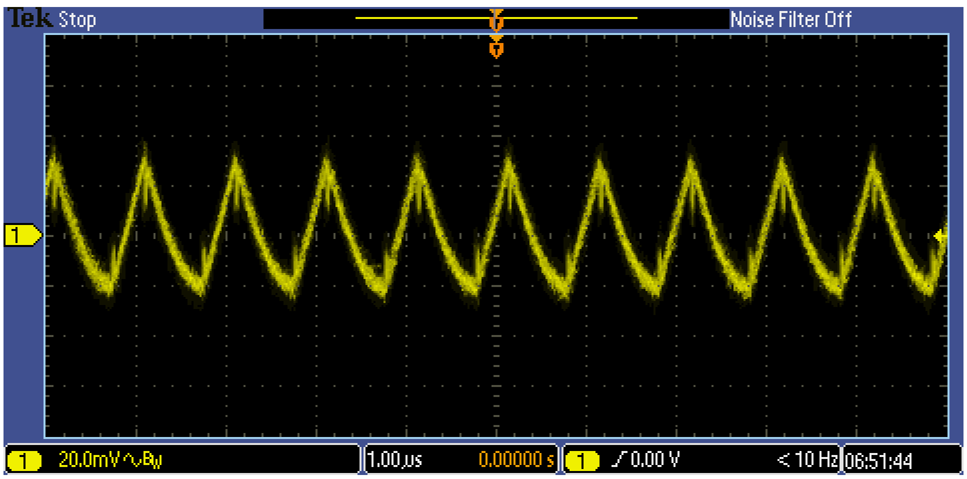

Figure 13. Boost Output Ripple with 500-mA Load

3.4 Transient

For the most accurate transient measurements, make sure the wire leads are cut very short and the load directly connects to the CORE (buck) or WLED (boost) screw terminals. Like the ripple measurements, connect the voltage probes directly across the output capacitors (C13 for buck, C6 for boost)

3.4.1 Buck

Figure 14 through Figure 16 show the expected results when setting the buck at 1.8 V. Refer to Figure 3 for the voltage codes that achieve this output.

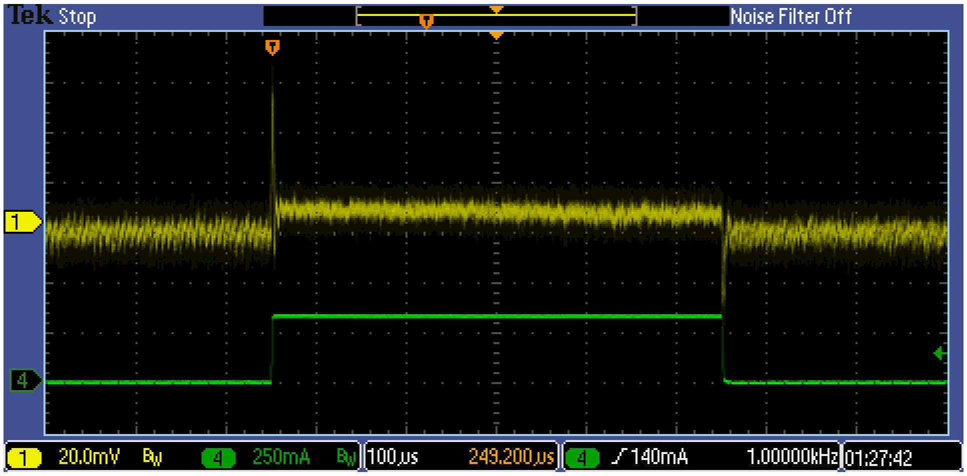

Figure 14. Buck Transient Response at 1.8-V Output

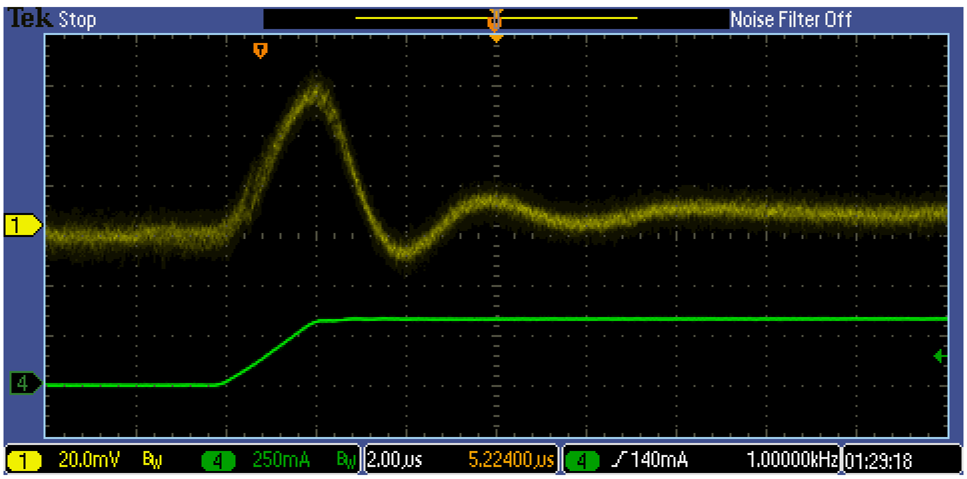

Figure 15. Buck Transient Response at 1.8-V Output – Rising Edge

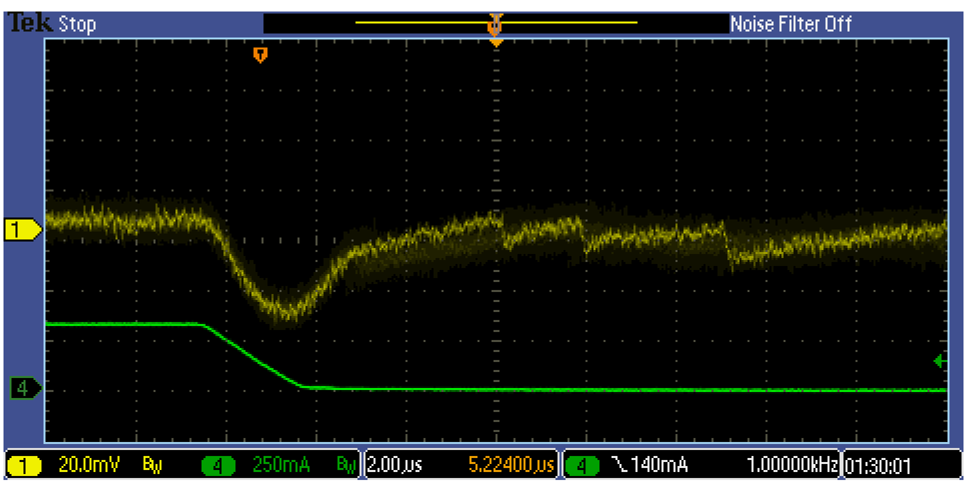

Figure 16. Buck Transient Response at 1.8-V Output – Falling Edge

3.4.2 Boost

Figure 17 through Figure 19 show the expected results when setting the boost at 4.27 V. Refer to Figure 4 for the voltage code that achieve this output.

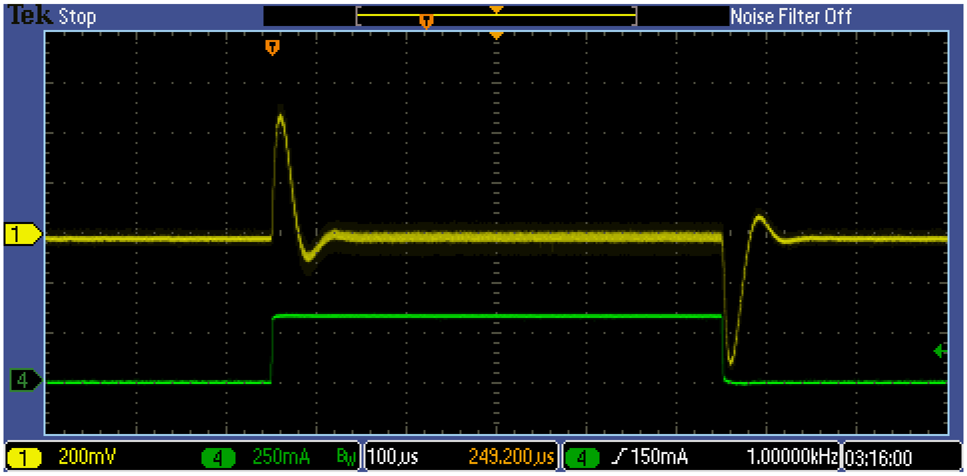

Figure 17. Boost Transient Response at 4.27-V Output

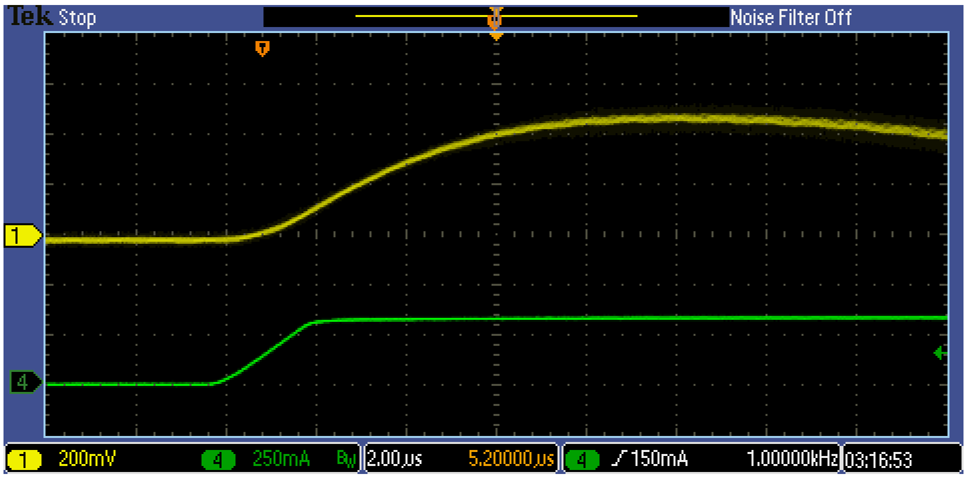

Figure 18. Boost Transient Response at 4.27-V Output – Rising Edge

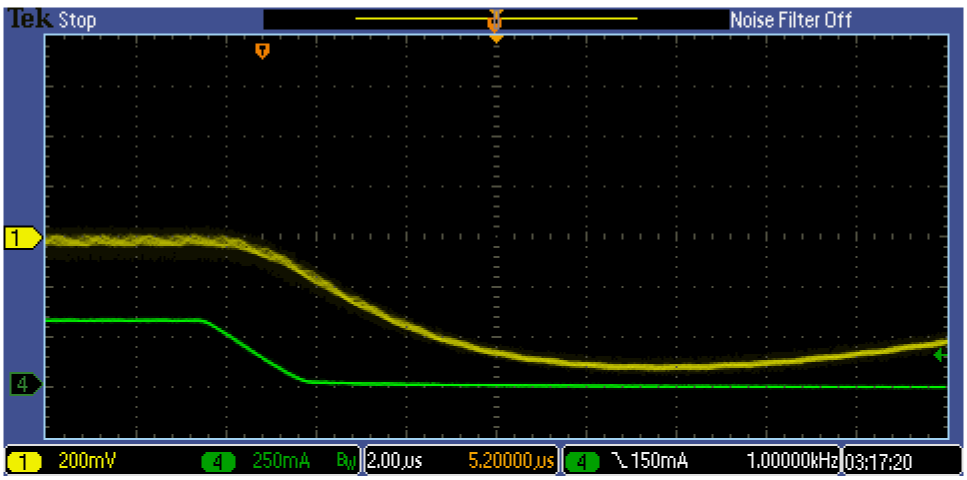

Figure 19. Boost Transient Response at 4.27-V Output – Falling Edge

3.5 Clock Configurations

The TPS68470EVM has a built in crystal oscillator (24 MHz), phase lock loop (PLL), and clock dividers for clock generation to the sensor and internal switching converters. The PLL is used to multiply the crystal oscillator frequency by a programmable factor such that the clock pins are in the range of 4–64 MHz in 0.1-MHz increments.

3.5.1 Internal Oscillator

The following outlines enabling the clock using the built-in crystal oscillator frequency, which in the TPS68470EVM is 24 MHz.

- Power on the device as per Section 2.2
- Set CLKCFG1 (address 0x0F) bit settings to 0x05 (sets HCLK_A, HCLK_B outputs to crystal oscillator frequency)
- Set S_I2C_CTL (address 0x43) bit 1 to 1 (enables the S_IO LDO)
- **Note:** Make sure the oscilloscope is set to *Full Bandwidth* mode
- Use the oscilloscope probe to check TP19 and TP22 (A, B, non-buffered) and TP30 and TP31 (A, B, buffered waveform) and verify a square waveform with 24-MHz (approximate period of 40–43 ns) outputs at the pins
- Power off the device
- Figure 20 shows the expected output at either HCLK pin

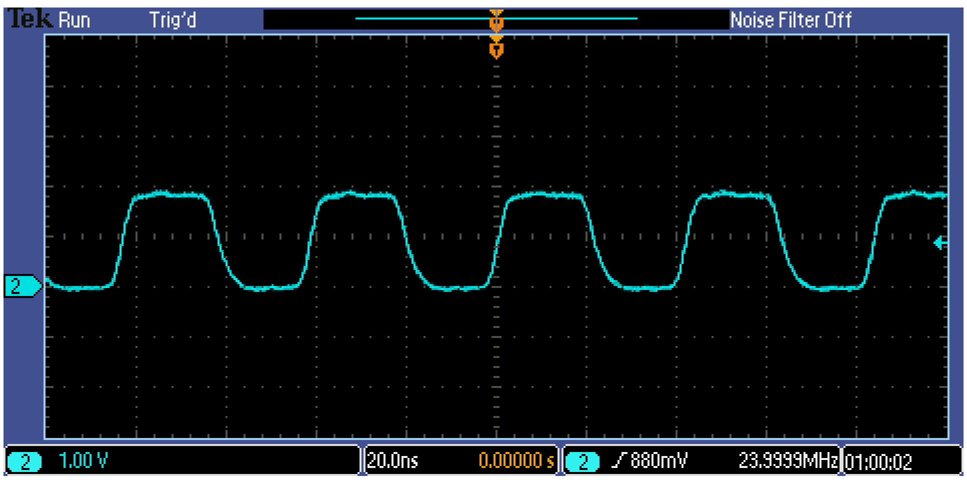

Figure 20. 24-MHz Square Wave Output at HCLK

3.5.2 PLL Multiplier

Enable and set the PLL multiplier to output a PLL_VCO_CLK frequency than can be used to output a frequency range of 4 to 64MHz on the HCLK pins. Refer to the datasheet (SLVSCJ1) under Clock Generation for more information.

fHCLK = PLL_VCO_CLK / POSTDIV FACTOR (2)

Where:

POSTDIV FACTOR = 2POSTDIV[1:0] which can be set to 1, 2, 4 or 8 (3)

PLL_VCO_CLK = (PLLDIV[8:0] + 320) x PLL_REF_CLK (4)

PLL_REF_CLK = fcrystal / (XTALDIV[7:0] + 30) (5)

"ƒcrystal" will equal 24 MHz in all factory shipped EVMs for TPS68470.

Use the following registers to set the programmable values:

- XTALDIV[7:0] (address 0x0A)
- PLLDIV[8:0] (address 0x0B for upper 8 bits and address 0x0C for LSB)
- POSTDIV[1:0] (address 0x0C)

The following steps are an example procedure to set up the fHCLK outputs at 64 MHz.

1. Determine the value for POSTDIV[1:0]

fHCLK = PLL_VCO_CLK / POSTDIV FACTOR

POSTDIV FACTOR = 2POSTDIV[1:0] = PLL_VCO_CLK / fHCLK

PLL_VCO_CLK in this example must be set to 64MHz in order to be able to divide down to 64MHz.

POSTDIV FACTOR = 64MHz / 64MHz= 1

Set POSTDIV[1:0] to ‘00’

2. Determine the value for XTALDIV[7:0]

PLL_REF_CLK = fcrystal / (XTALDIV[7:0] + 30)

XTALDIV[7:0] = (fcrystal / PLL_REF_CLK) – 30 Note: Choose a value for XTALDIV[7:0] such that PLL_REF_CLK = 100 kHz, or as close as possible to that value.

XTALDIV[7:0] = (24MHz / 100KHz) – 30

XTALDIV[7:0] = 210 (D2 in hex)

3. PLL_VCO_CLK = (PLLDIV[8:0] + 320) x PLL_REF_CLK

PLLDIV[8:0] = (PLL_VCO_CLK / PLL_REF_CLK) – 320

Where PLL_VCO_CLK = 64MHz and PLL_REF_CLK = 100 KHz

PLLDIV[8:0] = (64MHz / 100KHz) – 320

PLLDIV[8:0] = 320 (140 in hex)

- 1. Power on the device as per Section 2.2.
- 2. Set S_I2C_CTL (address 0x43) bit 1 to ‘1’ (enables the LDO).
- 3. Set CLKCFG1 (address 0x0F) bit settings to 0x0A (set output for HCLKs to programmable PLL).
- 4. Set CLKCFG2 (address 0x10) bit settings to 0x0F (drive strength = 8 mA).
- 5. Set XTALDIV[7:0] (address 0x0A) bit settings to 0xD2 from calculations above.
- 6. Set PLLDIV[8:1] (address 0x0B) bit settings to 0xA0 (upper 8 bits of PLLDIV[8:0]).
- 7. Set PLLDIV[0] (address 0x0C) bit setting to ‘0’ (LSB of PLLDIV[8:0].
- 8. POSTDIV[1:0] (address 0x0C) bit settings to ‘00’ (gives a POSTDIV FACTOR or 1
- 9. Set PLLCTL (address 0x0D) bit 0 to ‘1’ (enable PLL).
- 10. Use the oscilloscope probe to check the waveform at TP19 and TP22 (A, B, non-buffered) and TP30 and TP31 (A, B, buffered waveform) and verify a 64-MHz waveform.

3.6 Schematic

Figure 21 illustrates the TPS68470EVM schematic.

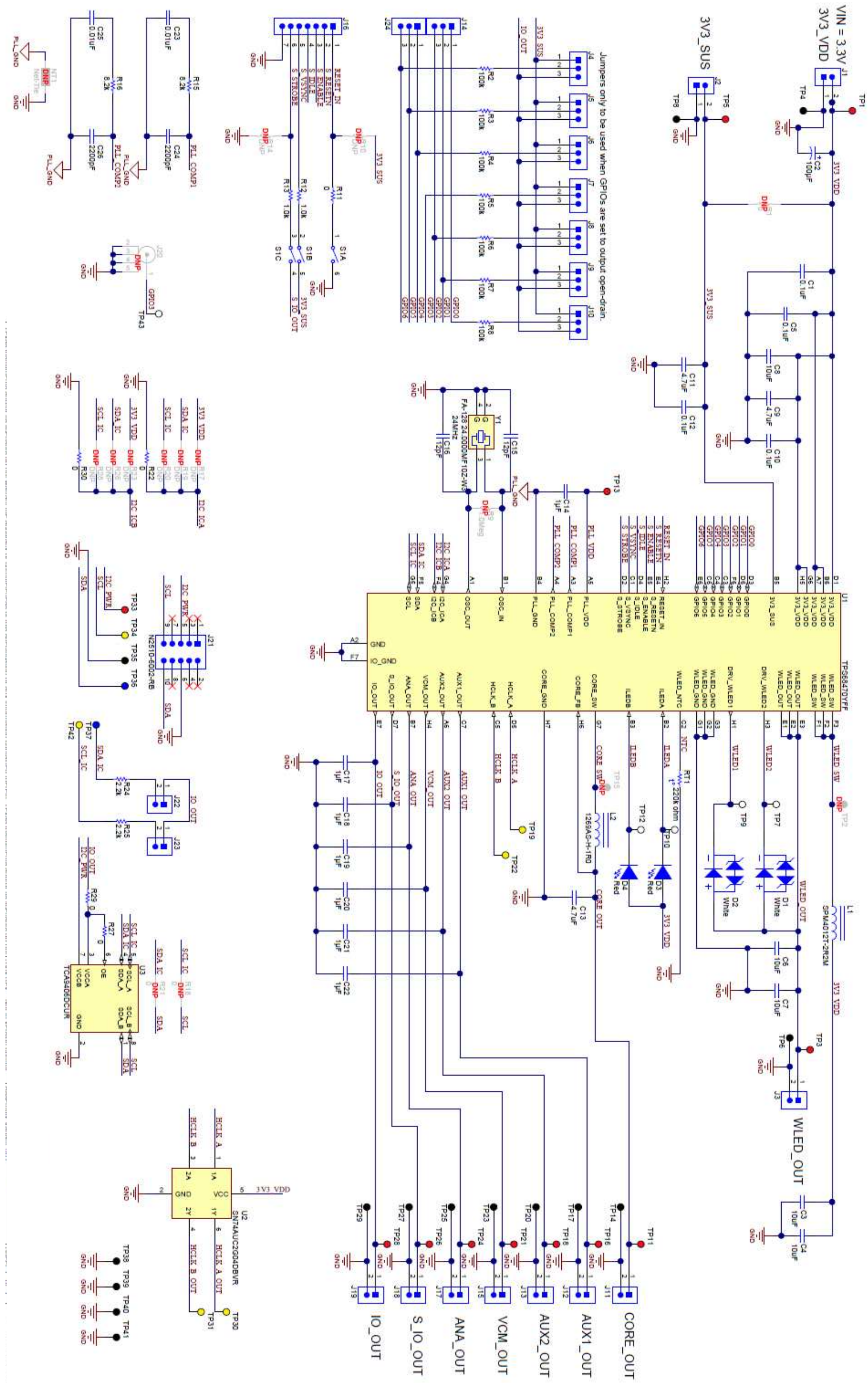

Figure 21. TPS68470 Schematic

3.7 PCB Layout

Figure 22 through Figure 27 illustrate the TPS68470EVM PCB layouts.

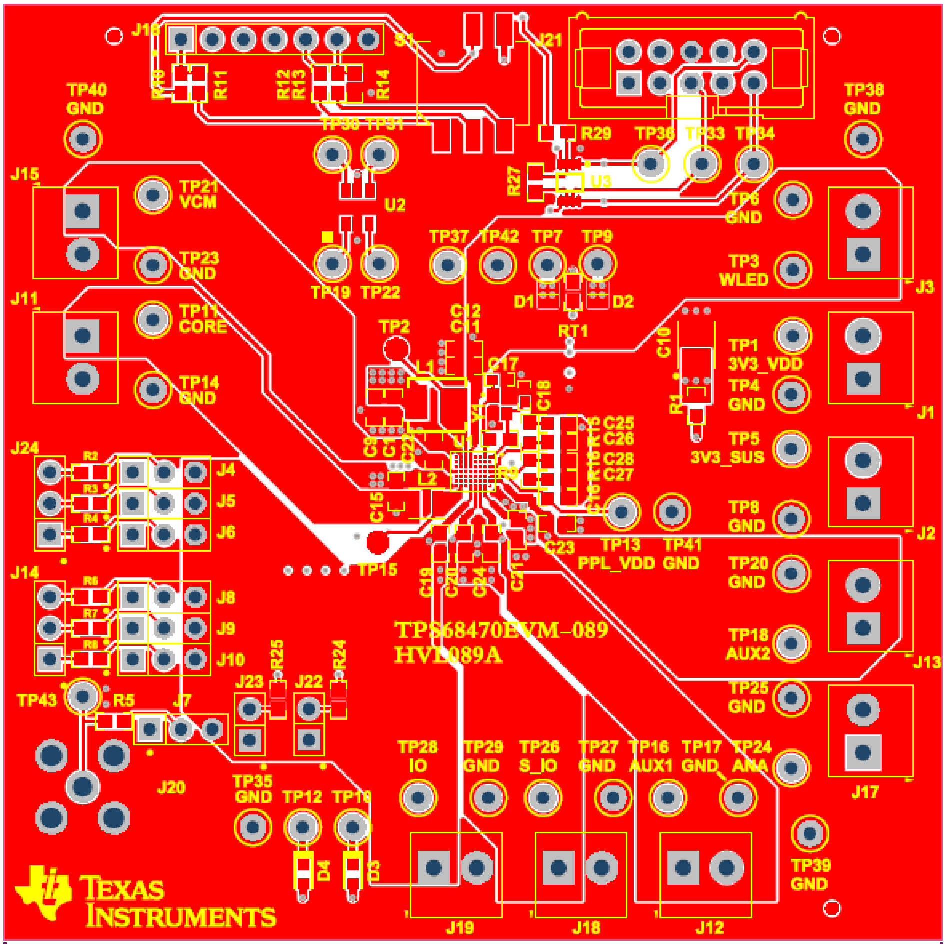

Figure 22. Top Overlay

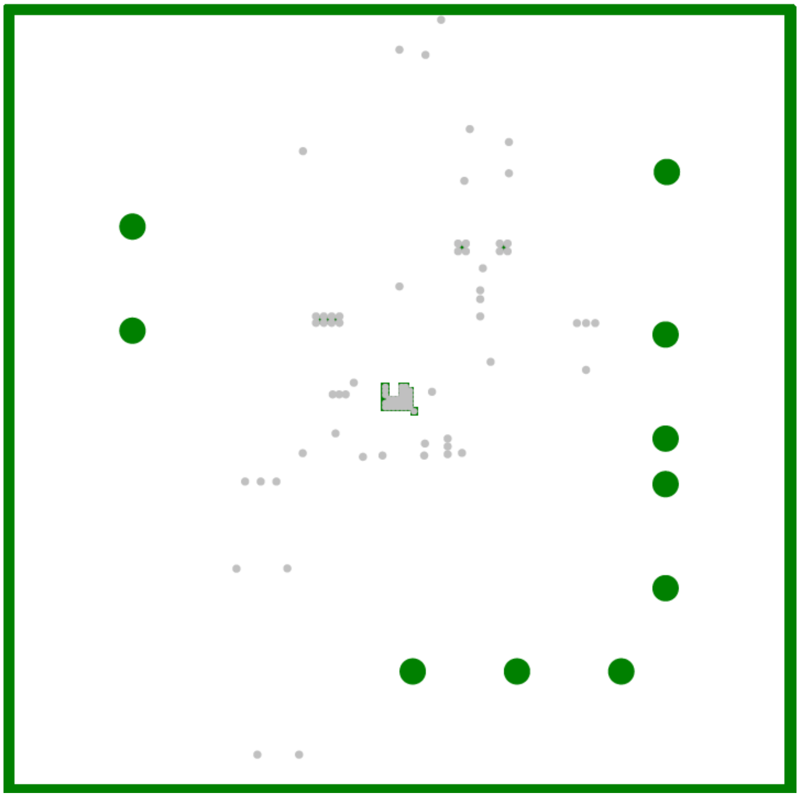

Figure 23. Ground Plane

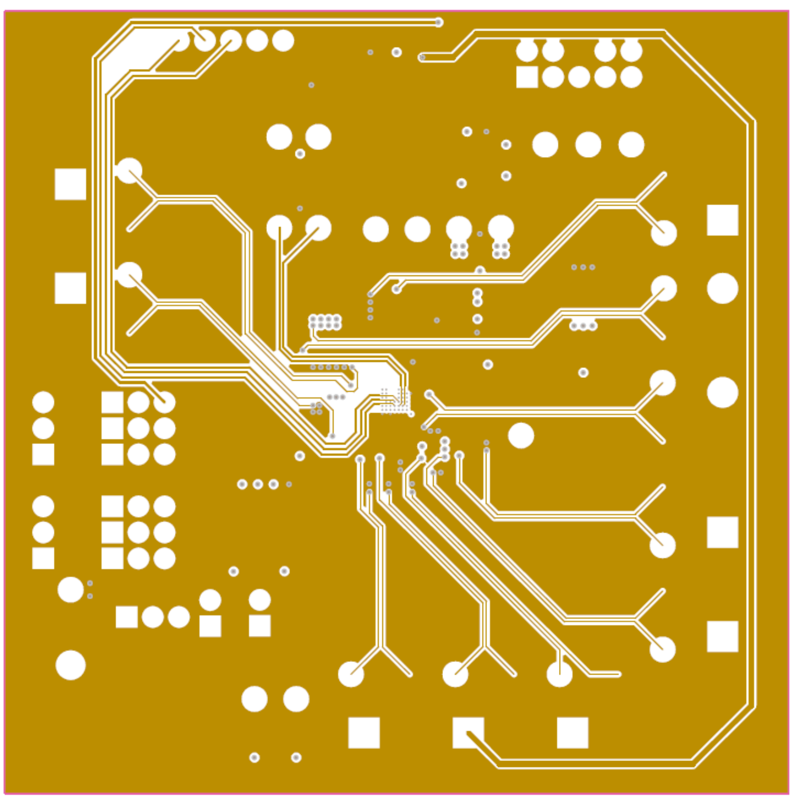

Figure 24. Sig 1

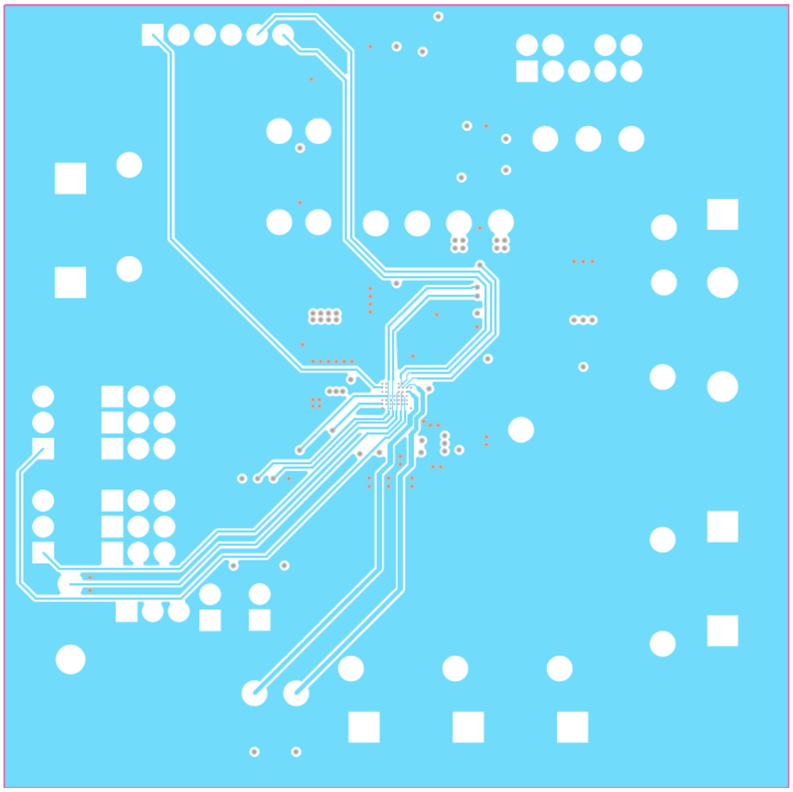

Figure 25. Sig 2

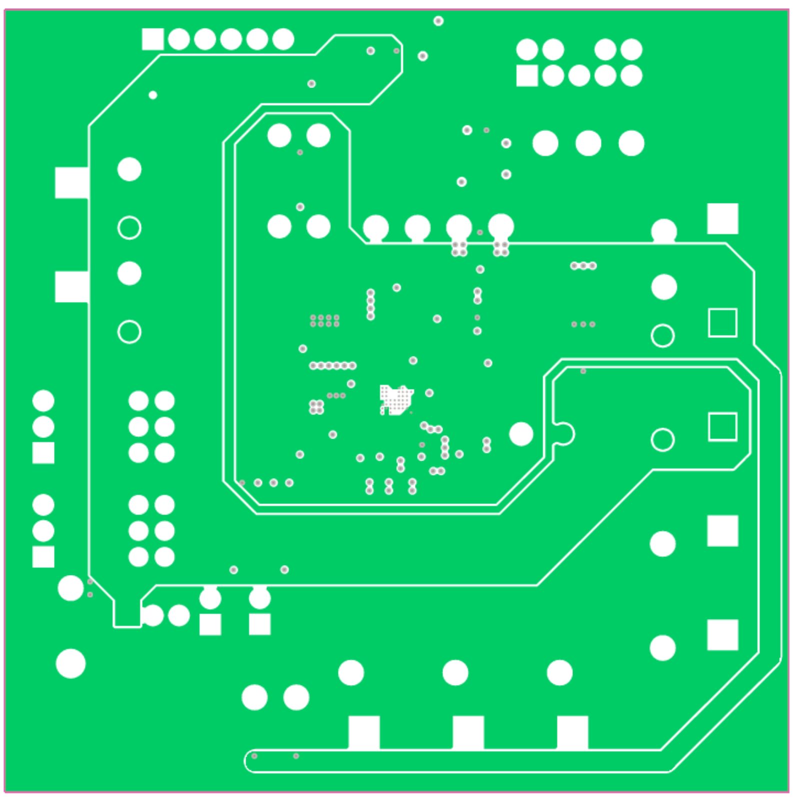

Figure 26. Power Connections

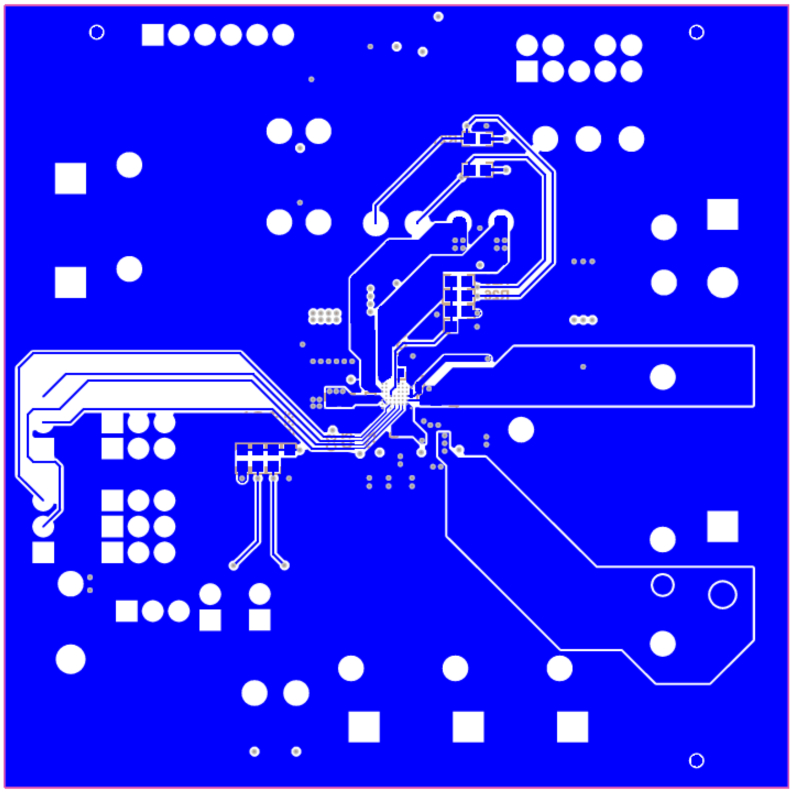

Figure 27. Bottom Layer

3.8 Bill of Materials

Table 3 lists the TPS68470EVM BOM.

Table 3. Bill of Materials for TPS68470EVM

Quantity	Designator	Description	Manufacturer	Part Number
1	PCB	Printed Circuit Board	Any	HVL089
3	C1, C2, C9	CAP, CERM, 10µF, 6.3V, ±20%, X5R, 0603	TDK	C1608X5R0J106M
3	C3, C13, C15	CAP, CERM, 4.7µF, 6.3V, ±20%, X5R, 0603	TDK	C1608X5R0J475M
4	C4, C6, C7, C14	CAP, CERM, 0.1µF, 6.3V, ±10%, X5R, 0402	TDK	C1005X5R0J104K
1	C10	CAP, TA, 100µF, 6.3V, ±20%, 0.7 ohm, SMD	Kemet	T495B107M006ATE700
2	C11, C12	CAP, CERM, 10µF, 10V, ±20%, X5R, 0603	TDK	C1608X5R1A106M
7	C16, C19–C24	CAP, CERM, 1µF, 6.3V, ±10%, X5R, 0603	TDK	C1608X5R0J105K
2	C17, C18	CAP, CERM, 12pF, 25V, ±5%, C0G/NP0, 0402	Murata	GRM1555C1E120JA01D
2	C25, C27	CAP, CERM, 0.01µF, 50V, ±10%, X7R, 0603	TDK	C1608X7R1H103K
2	C26, C28	CAP, CERM, 2200pF, 50V, ±10%, X7R, 0603	TDK	C1608X7R1H222K
2	D1, D2	High Power Flash ELCH08	Everlight	ELCH08-5070J6J8284110-N0
2	D3, D4	LED, Red, SMD	Lite-On	LTST-C190CKT
4	H1, H2, H3, H4	Bumpon, Cylindrical, 0.312 X 0.200, Black	3M	SJ61A1
10	J1–J3, J11–J13, J15, J17–J19	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
9	J4–J10, J14, J24	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec	TSW-103-07-G-S
1	J16	Header, TH, 100mil, 7x1, Gold plated, 230 mil above insulator	Samtec	TSW-107-07-G-S
1	J21	Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	3M	N2510-6002-RB
2	J22, J23	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec	TSW-102-07-G-S
1	L1	Inductor, Wirewound, Metal Composite, 2.2µH, 3.3A, 0.095 Ω, SMD	TDK	SPM4012T-2R2M
1	L2	Inductor, Shielded, Ferrite, 1.5uH, SMD	Toko	1269AS-H-1R0
7	R2–R8	RES, 100kΩ, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100KJNEA
5	R11, R22, R27, R29, R30	RES, 0 Ω, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA
2	R12, R13	RES, 1.0kΩ, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K00JNEA
2	R15, R16	RES, 8.2kΩ, 5%, 0.1W, 0603	Vishay-Dale	CRCW06038K20JNEA
2	R24, R25	RES, 2.2kΩ, 5%, 0.1W, 0603	Vishay-Dale	CRCW06032K20JNEA
1	RT1	Thermistor NTC, 220kΩ, 5%, 0603	Murata	NCP18WM224J03RB
1	S1	Switch, Slide, SPST 3 poles, SMT	CTS Electrocomponents	219-3LPST
9	SH-J1–SH-J9	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA
12	TP1, TP3, TP5, TP11, TP13, TP16, TP18, TP21, TP24, TP26, TP28, TP33	Test Point, Miniature, Red, TH	Keystone	5000
15	TP4, TP6, TP8, TP14, TP17, TP20, TP23, TP25, TP27, TP29, TP35, TP38–TP41	Test Point, Miniature, Black, TH	Keystone	5001
5	TP7, TP9, TP10, TP12, TP43	Test Point, Miniature, White, TH	Keystone	5002
6	TP19, TP22, TP30, TP31, TP34, TP42	Test Point, Miniature, Yellow, TH	Keystone	5004
2	TP36, TP37	Test Point, Miniature, Blue, TH	Keystone	5117
1	U1	TPS68470YFF, YFF0056AGAG	Texas Instruments	TPS68470YFF
1	U2	Dual Inverter	Texas Instruments	SN74AUC2G04DBVR
1	U3	TCA9406 Dual Bidirectional 1-MHz I2C-BUS and SMBus Voltage Level-Translator, 1.65 to 3.6 V, –40°C to 85°C, 8-pin US8 (DCU), Green (RoHS & no Sb/Br)	Texas Instruments	TCA9406DCUR
1	Y1	Crystal, 24MHz, 12pF, SMD	Epson	FA-128 24.0000MF10Z-W3

ADDITIONAL TERMS AND CONDITIONS, WARNINGS, RESTRICTIONS, AND DISCLAIMERS FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) markets, sells, and loans all evaluation boards, kits, and/or modules (EVMs) pursuant to, and user expressly acknowledges, represents, and agrees, and takes sole responsibility and risk with respect to, the following:

1. User agrees and acknowledges that EVMs are intended to be handled and used for feasibility evaluation only in laboratory and/or development environments. Notwithstanding the foregoing, in certain instances, TI makes certain EVMs available to users that do not handle and use EVMs solely for feasibility evaluation only in laboratory and/or development environments, but may use EVMs in a hobbyist environment. All EVMs made available to hobbyist users are FCC certified, as applicable. Hobbyist users acknowledge, agree, and shall comply with all applicable terms, conditions, warnings, and restrictions in this document and are subject to the disclaimer and indemnity provisions included in this document.
2. Unless otherwise indicated, EVMs are not finished products and not intended for consumer use. EVMs are intended solely for use by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.
3. User agrees that EVMs shall not be used as, or incorporated into, all or any part of a finished product.
4. User agrees and acknowledges that certain EVMs may not be designed or manufactured by TI.
5. User must read the user's guide and all other documentation accompanying EVMs, including without limitation any warning or restriction notices, prior to handling and/or using EVMs. Such notices contain important safety information related to, for example, temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.
6. User assumes all responsibility, obligation, and any corresponding liability for proper and safe handling and use of EVMs.
7. Should any EVM not meet the specifications indicated in the user's guide or other documentation accompanying such EVM, the EVM may be returned to TI within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI TO USER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. TI SHALL NOT BE LIABLE TO USER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES RELATED TO THE HANDLING OR USE OF ANY EVM.
8. No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which EVMs might be or are used. TI currently deals with a variety of customers, and therefore TI's arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services with respect to the handling or use of EVMs.
9. User assumes sole responsibility to determine whether EVMs may be subject to any applicable federal, state, or local laws and regulatory requirements (including but not limited to U.S. Food and Drug Administration regulations, if applicable) related to its handling and use of EVMs and, if applicable, compliance in all respects with such laws and regulations.
10. User has sole responsibility to ensure the safety of any activities to be conducted by it and its employees, affiliates, contractors or designees, with respect to handling and using EVMs. Further, user is responsible to ensure that any interfaces (electronic and/or mechanical) between EVMs and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
11. User shall employ reasonable safeguards to ensure that user's use of EVMs will not result in any property damage, injury or death, even if EVMs should fail to perform as described or expected.
12. User shall be solely responsible for proper disposal and recycling of EVMs consistent with all applicable federal, state, and local requirements.

Certain Instructions. User shall operate EVMs within TI's recommended specifications and environmental considerations per the user's guide, accompanying documentation, and any other applicable requirements. Exceeding the specified ratings (including but not limited to input and output voltage, current, power, and environmental ranges) for EVMs may cause property damage, personal injury or death. If there are questions concerning these ratings, user should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the applicable EVM user's guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using EVMs' schematics located in the applicable EVM user's guide. When placing measurement probes near EVMs during normal operation, please be aware that EVMs may become very warm. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use EVMs.

Agreement to Defend, Indemnify and Hold Harmless. User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

Safety-Critical or Life-Critical Applications. If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

RADIO FREQUENCY REGULATORY COMPLIANCE INFORMATION FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) evaluation boards, kits, and/or modules (EVMs) and/or accompanying hardware that is marketed, sold, or loaned to users may or may not be subject to radio frequency regulations in specific countries.

General Statement for EVMs Not Including a Radio

For EVMs not including a radio and not subject to the U.S. Federal Communications Commission (FCC) or Industry Canada (IC) regulations, TI intends EVMs to be used only for engineering development, demonstration, or evaluation purposes. EVMs are not finished products typically fit for general consumer use. EVMs may nonetheless generate, use, or radiate radio frequency energy, but have not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or the ICES-003 rules. Operation of such EVMs may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Important Notice for Users of EVMs Considered “Radio Frequency Products” in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 本開発キットは技術基準適合証明を受けておりません。 本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス· インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

http://www.tij.co.jp

Texas Instruments Japan Limited

(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265