User's Guide

LM5127EVM-FLEX Evaluation Module

ABSTRACT

The LM5127EVM-FLEX evaluation module showcases the features and performance of the LM5127-Q1 three channel synchronous controller, consisting of a one flexible topology controller (channel 1) and two buck controllers (channel 2 and channel 3). In the standard configuration, the flexible topology (channel 1) is configured as a pre-boost controller supplying the two independent buck controllers (channel 2 and channel 3). The input voltage range is from 3 V to 18 V, providing two output voltage rails of 5 V at 5 A and 3.3 V at 7 A. This evaluation module is designed to handle input transients up to 42 V and operates at a switching frequency of 440 kHz. Functionality in the standard configuration includes: adjustable soft-start for each channel, bypass mode operaiton for the pre-boost channel, programmable cycle-by-cycle peak current limit, hiccup mode short circuit protection, overvoltage protection for each channel, independent enable pins for each channel, programable wake-up and sleep threshold, power good indicators for each channel, selectable switching mode operation (forced-PWM, skip and diode emulation mode), and optional frequency dithering. This evaluation module also supports dual phase buck operation between channel 2 and channel 3, and channel 1 configured as a buck controller.

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1 Introduction

The LM5127EVM-FLEX is designed for use with a wide input voltage range of 3 V to 42 V to produce two tightly regulated output voltages of 5 V at 5 A and 3.3 V at 7 A. Figure 1-1 shows the standard configuration of the LM5127EVM-FLEX. It is configured as a typical front end power supply in 12 V automotive applications. Channel 1 implements a synchronous pre-boost, supplying adequate voltage for the two synchronous buck controllers (channel 2 / channel 3) to maintain output regulation for input voltage transients as low as 3 V. The free-running switching frequency is 440 kHz and synchronization to an external clock signal is possible at higher or lower frequency. The main discrete power-train components (inductors and MOSFETs) are automotive AEC-Q200 rated.

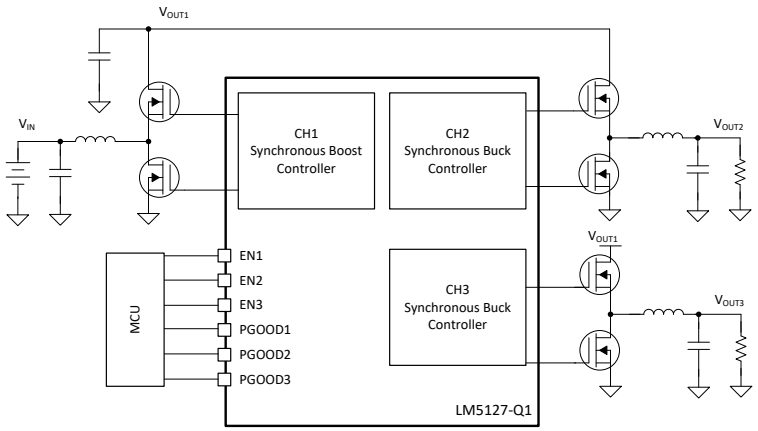

Figure 1-1. Typical Application Circuit

1.1 Applications

- Mutli-rail DC/DC power supply
- Front-stage power supply for automotive infotainment, cluster, body control, and ADAS

1.2 Features

The LM5127EVM-FLEX has the following features :

- Wide input voltage range from 3 V to 18 V
  - 5 V required for start-up
  - Maximum transient voltage of 42 V
- Operating frequency of 440 kHz with external clock synchronization up or down by 20%
- Bypass mode operation when channel 1 is configured as a boost controller.
- LDO mode operating when $V_{IN} \cong V_{OUT}$ for channels configured as a buck controller.
- Selectable forced-PWM (FPWM), skip mode or diode emulation mode (DEM) using the CFG/MODE pin
- Tightly regulated buck output voltages of 5 V and 3.3 V with better than ±1% set point accuracy
  - Fixed output voltage of 5 V or 3.3 V using internal low leakage current, high impedance feedback resistors
  - Programmable output voltage with external feedback resistors adjustable from 0.8 V to 42 V
- High power conversion efficiency across wide load current ranges:
  - Half-load efficiency of 94.2% at V_{IN} = 13.5 V, I_{OUT2} = 2.5 A, I_{OUT3} = 3.5 A, R_{CFG} = 19.1 kΩ
  - Full-load efficiency of 93.8% at V_{IN} = 13.5 V, I_{OUT2} = 5 A, I_{OUT3} = 7 A, R_{CFG} = 19.1 kΩ
- Over current protection configurable by the RES pin
  - Hiccup mode short circuit protection, cycle-by-cycle peak current limiting, latch-off peak current limiting
- Selectable output voltage with low leakage, high impedance, internal feedback resistor when a channel is configured a buck controller
- Optional frequency dithering for improved EMI performance
- Enable pins (EN1, EN2, EN3) and Power good (PGOOD1, PGOOD2, PGOOD3) indicators for each channel
- Adjustable soft-start for each channel (SS1, SS2, SS3)
- Programmable wake-up and sleep voltage threshold (DIS/BMOUT pin).

- Overvoltage protection for each channel
- Flexible Topology capable for multiple configurations. See Section 7 for details.
  - Flexible topology on channel 1 (boost controller or buck controller)
  - Single output or dual phase interleaved buck controllers (channel 2 and channel 3)

2 EVM Setup

2.1 EVM Characteristics

Table 2-1 shows the evaluation module characteristics in the standard configuration and according to Section 6.

Table 2-1. EVM characteristics

Parameter	Test Condition		MIN	TYP	MAX	UNIT
INPUT VOLTAGE CHARACTERISTICS						
Input voltage range	Operation		3		18	V
	Start-up		5			V
	Transient				42	V
Input current, no load	V_{EN1} = V_{EN2} = V_{EN3} = 5 V I_{OUT1} = I_{OUT2} = I_{OUT3} = 0 A VCH1A = 13.5 V, VCCX = V_{OUT2}, VDDX = V_{OUT3}, CFG/MODE = tied to AGND	V_{IN} = VCH1A = 9 V		50		µA
		V_{IN} = VCH1A = 12 V		50		µA
		V_{IN} = VCH1A = 18 V		50		µA
Input current shutdown	V_{EN1} = V_{EN2} = V_{EN3} = 0 V	V_{IN} = VCH1A= 13.5 V		4		µA
CHANNEL 1 OUTPUT CHARACTERISITICS (Pre-boost)						
Output voltage (V_{OUT1})				6.9		V
Maximum output current (I_{OUT1})	VCH1A > 3 V			10		A
CHANNEL 2 OUTPUT CHARACTERISITICS (SINGLE BUCK)						
Output voltage (V_{OUT2})				5		V
Maximum output current (I_{OUT2})	VCH1A > 3 V			5		A
CHANNEL 3 OUTPUT CHARACTERISITICS (SINGLE BUCK)						
Output voltage (V_{OUT3})	VCH1A > 3 V			3.3		V
Maximum output current (I_{OUT3})				7		A
SYSTEM CHARACTERISITICS						
Switching Frequency	VCH1A = 13.5 V			440		kHz
Half Load Efficiency (η_{HALF})	I_{OUT2} = 2.5 A, I_{OUT3} = 3.5 A	VCH1A = 9 V		95.3		%
		VCH1A = 13.5 V		94.2		%
		VCH1A = 18 V		92.8		%
Full Load Efficiency (η_{FULL})	I_{OUT2} = 5 A, I_{OUT3} = 7 A (ADD table note	VCH1A = 9 V		94.5		%
		VCH1A = 13.5 V		93.8		%
		VCH1A = 18 V		92.1		%

3 EVM Photo

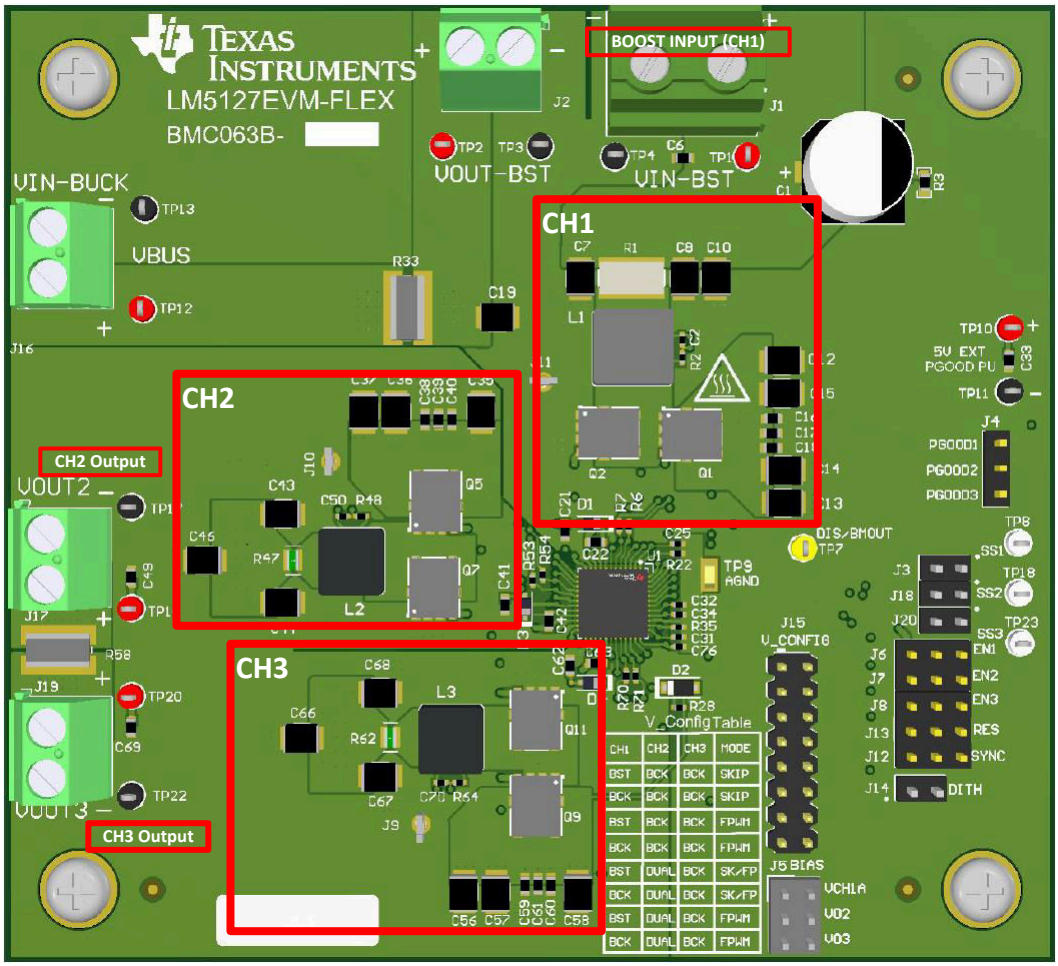

Figure 3-1. EVM Photo: Front

CAUTION

Prolonged operation with low input at full power will cause heating of Q1 and Q2. Board surface is hot. Do not touch. Contact may cause burns.

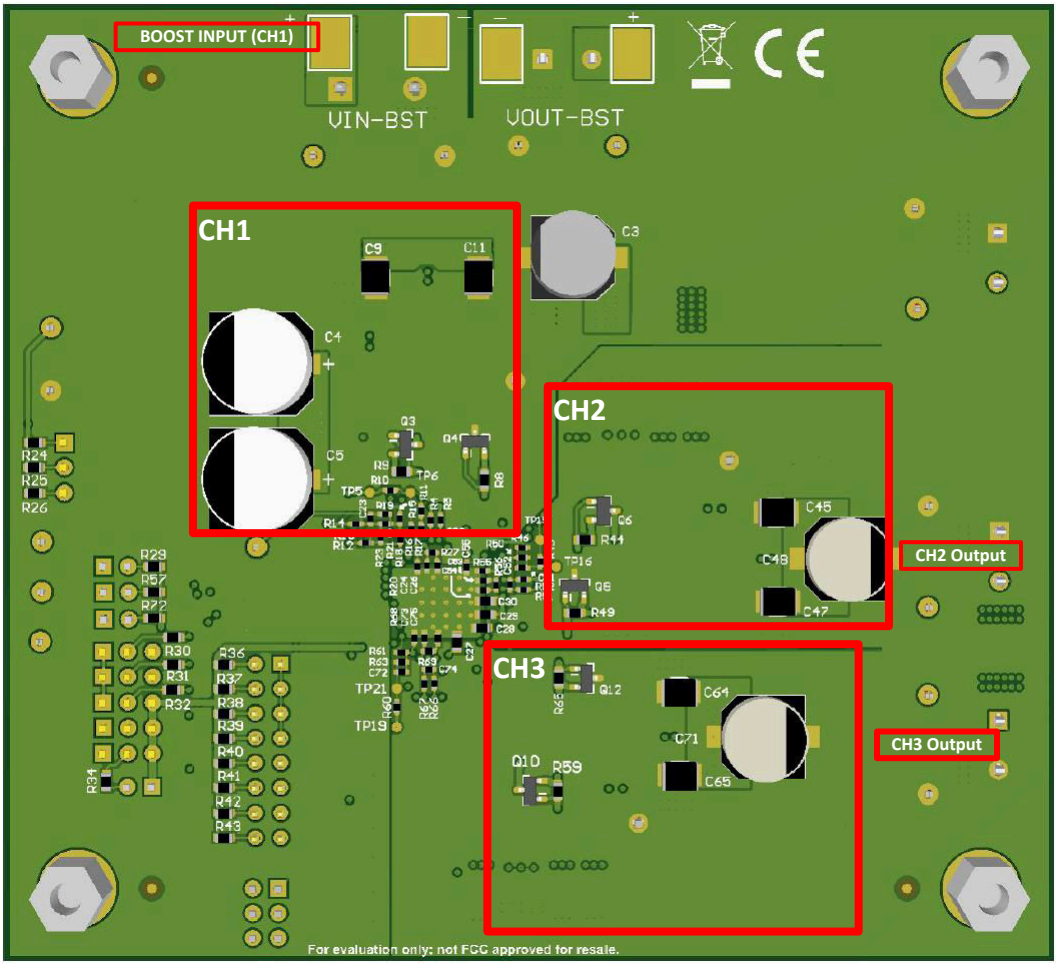

Figure 3-2. EVM Photo: Back

4 Testing Procedures

The following test equipment is needed to test the LM5127EVM-FLEX as shown in the Figure 4-1 and in the standard configuration according to Section 6.

- Power supply: The input voltage source (VIN) should be a variable supply. The power supply should source 3 V to 42 V and be able to supply more than 30 A or current.
- Electronic Load
  - Electronic load 2: Capable of at least 5 A at a voltage of 5 V
  - Electronic load 3: Capable of at least 7 A at a voltage of 3.3 V
- Multimeters
  - Voltmeter 1 (V_{IN}): Capable of measuring the input voltage range up to 42 V
  - Voltmeter 2 (V_{OUT2}): Capable of measuring output voltage of 5 V
  - Voltmeter 3 (V_{OUT3}): Capable of measuring output voltage of 3.3 V
  - Ammeter 1 (I_{IN}): Capable of 30 A DC measurement. A shunt resistor may also be used to measure the input current.
  - Ammeter 2 (I_{OUT2}): Capable of at least 5 A DC measurement
  - Ammeter 3 (I_{OUT3}): Capable of at least a 7 A DC measurement

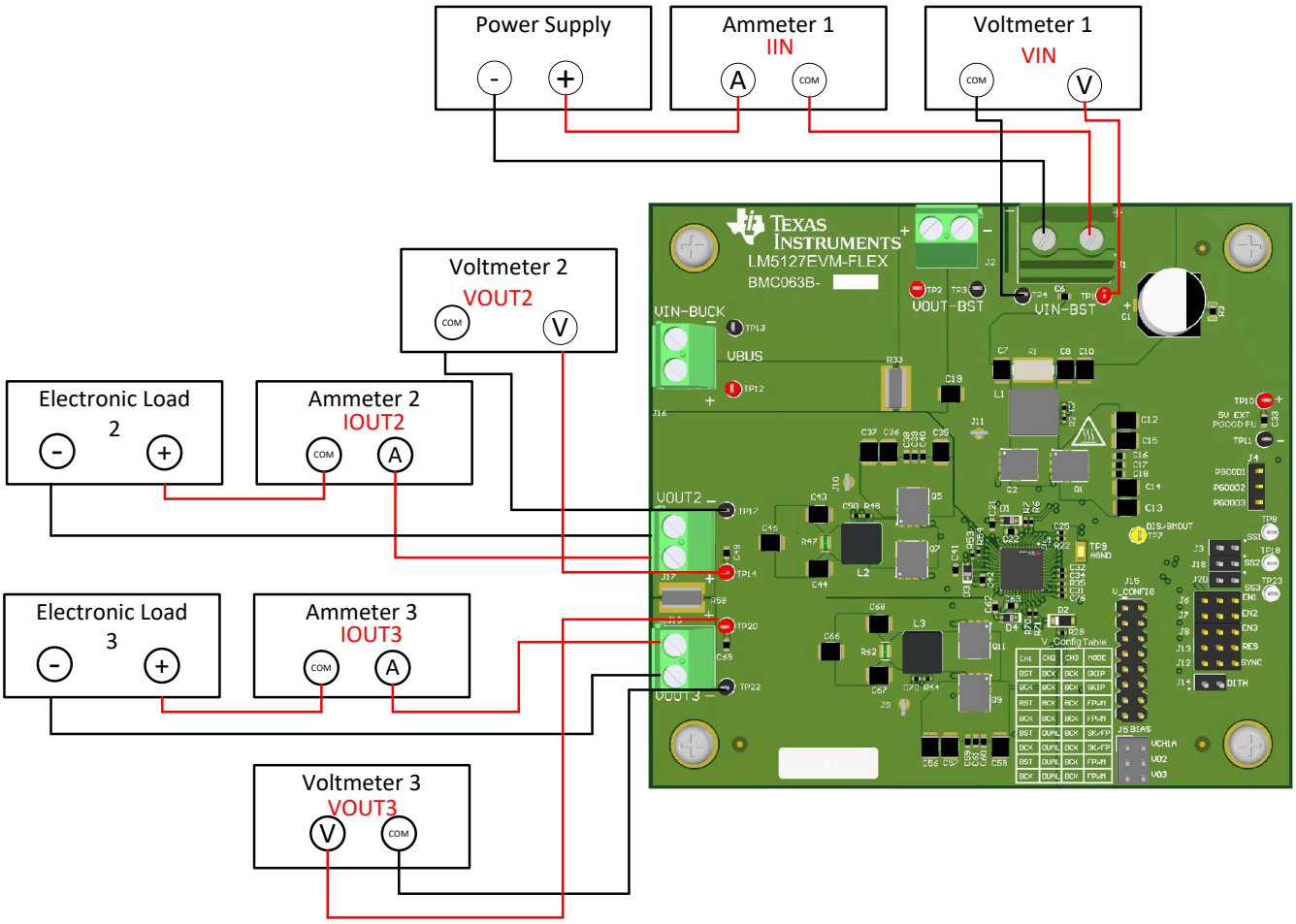

Figure 4-1. EVM Test Setup

4.1 EVM Connectors and Test Points

Table 4-1 lists the EVM jumper descriptions.

Table 4-1. Jumper Descriptions

Jumper	Name	Description
J1	VCH1A	When CH1 is configured as a boost controller this jumper is the connection for the input power for the boost controller. When CH1 is configured as a buck controller this is the output voltage for the buck controller
J2	VCH1B	When CH1 is configured as a boost controller this jumper is the connection for the output power for the boost controller. When CH1 is configured as a buck controller this is the input voltage for the buck controller
J3	SS1	Populating this jumper will enable diode emulation mode (DEM) on CH1
J4	PGOOD1/PGOOD2/PGOOD3	Probe points for PGOOD1, PGOOD2, PGOOD3. An external 5 V must be applied between TP10 and TP11 for these signals to be active
J5	VCCX	Bias voltage connection to the VCCX pin from one of the output channels on the board. Connecting pin 1 and pin 2 biases the VCCX with VCH1A. This connection is typically made when CH1 is configured as a buck controller. Connecting pin 3 and pin 4 biases the VCCX with VOUT2. Connecting pin 5 and pin 6 biases the VCCX with VOUT3.
J6	EN1	Input to enable or disable CH1. Connecting pin 1 and pin 2 enables CH1 by connecting the EN1 pin to the BIAS pin. Connecting pin 2 to pin 3 disables CH1 by connecting EN1 to GND.
J7	EN2	Input to enable or disable CH2. Connecting pin 1 and pin 2 enables CH2 by connecting the EN2 pin to the BIAS pin. Connecting pin 2 to pin 3 disables CH2 by connecting EN2 to GND.
J8	EN3	Input to enable or disable CH3. Connecting pin 1 and pin 2 enables CH3 by connecting the EN3 pin to the BIAS pin. Connecting pin 2 to pin 3 disables CH3 by connecting EN3 to GND.
J9, J10, J11	PGND	Power ground connections for oscilloscope measurements.
J12	SYNC/DITHER/VCC_HOLD	Configures the SYNC/Dither/VCC_HOLD pin based on the application specifications. Connecting pin 1 and pin 2 will enable the VCC hold functionality. Connecting a function generator between pin 2 and pin 3 allows for external clock synchronization if C34 is removed and J14 is left open. J14 and J12 should not be populated at the same time.
J13	RES	Configuration of the RES pin. Connecting pin 1 and pin 2 enables cycle by cycle peak current limiting with no hiccup mode. Connecting pin 2 and pin 3 latches the channel off until the appropriate enable pin is toggled. If the jumper is left of the hiccup mode time is determined by the value of capacitor connected to the RES pin (C34)
J14	Dither	Leaving this jumper and J12 open enables frequency dithering functionality. When pin 1 and pin 2 are connected frequency dithering, external clock synchronization and VCC_HOLD are disabled.
J15	CFG/MODE	This pin configures the LM5127 to the appropriate topology and switching mode for the application. For the standard configuration of this EVM the jump should be connected between pin 1 and pin 2 (SKIP) or between pin 5 and pin 6 (FPWM/DEM). See Table 4-3 for more detail on the device configuration.
J16	VBUS	Input voltage rail of CH2 and CH3 buck controllers. VBUS can be tied to VCH1B by populating R33 with a 0Ω resistor.
J17	VOUT2	Output voltage connection of CH2
J18	SS2	Populating this jumper will enable diode emulation mode (DEM) on CH2
J19	VOUT3	Output voltage connection of CH3
J20	SS3	Populating this jumper will enable diode emulation mode (DEM) on CH3

Table 4-2 lists the EVM test point descriptions.

Table 4-2. Test Point Description

Test Point	Name	Description
TP1	VCH1A	Positive voltage probe point for VCH1A
TP2	VCH1B	Positive voltage probe point for VCH1B

Table 4-2. Test Point Description (continued)

Test Point	Name	Description
TP3	PGND	Ground probe point for VCH1B
TP4	PGND	Ground probe point for VCH1A
TP5	VCH1B (+)	CH1 loop response positive injection point
TP6	VCH1B (-)	CH1 loop response negative injection point
TP7	DIS/BMOUT	DIS/BMOUT pin probe point
TP8	SS1	SS1 pin probe point
TP9	AGND	AGND probe point
TP10	5V_EXT (+)	Positive external 5V connection to pull PGOODx to 5V
TP11	5V_EXT (-)	Negative connection for external 5V PGOOD supply.
TP12	VBUS	Positive voltage probe point for VBUS
TP13	PGND	Ground probe point for VBUS
TP14	VOUT2	Positive voltage probe point for VOUT2
TP15	VOUT2(+)	CH2 loop response positive injection point
TP16	VOUT2(-)	CH2 loop response negative injection point
TP17	PGND	Ground probe point for VOUT2
TP18	SS2	SS2 pin probe point
TP19	VOUT3(+)	CH3 loop response positive injection point
TP20	VOUT3	Positive voltage probe point for VOUT3
TP21	VOUT3(-)	CH3 loop response negative injection point
TP22	PGND	Ground probe point for VOUT3
TP23	SS3	SS3 pin probe point

Table 4-3 lists the LM5127-Q1 pin CFG/MODE connection details (J15).

Table 4-3. CFG/MODE (J15) Connection Details

Configuration	Pin Connection	CH1	CH2	CH3	Switching Mode
1 (0Ω) **1**	1 to 2	Boost	Single Buck	Single Buck	Skip Mode
2 (9.53kΩ)	3 to 4	Buck			
3 (19.1kΩ) **1**	5 to 6	Boost			FPWM/DEM
4 (29.4kΩ)	7 to 8	Buck			
5 (41.2kΩ)	9 to 10	Boost	Dual Phase Buck		CH1: SkipCH2/CH3: FPWM/DEM
6 (54.9kΩ)	11 to 12	Buck			
7 (71.5kΩ)	13 to 14	Boost			FPWM/DEM
8 (90.9kΩ)	15 to 16	Buck			

5 Test Results

5.1 Efficiency

Figure 5-1 through Figure 5-6 show the efficiency graphs for the EVM.

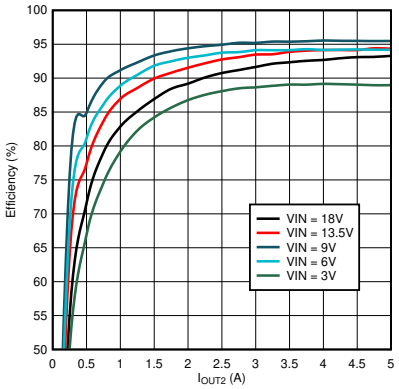

Figure 5-1. Efficiency vs. I_{OUT2} (FPWM, I_{OUT3} = 0 A)

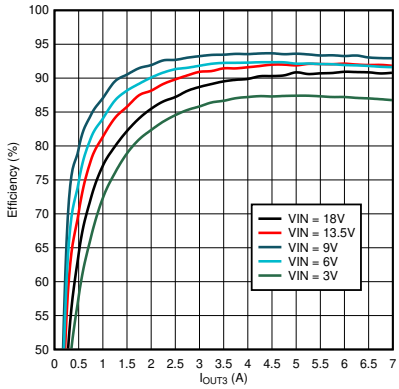

Figure 5-2. Efficiency vs. I_{OUT3} (FPWM, I_{OUT2} = 0 A)

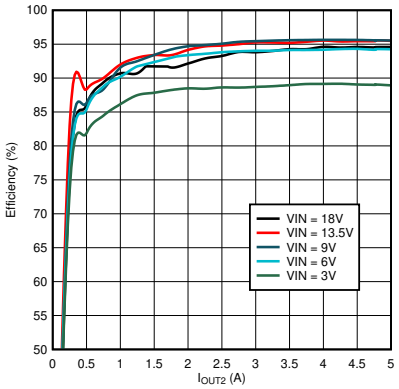

Figure 5-3. Efficiency vs. I_{OUT2} (DEM, I_{OUT3} = 0 A)

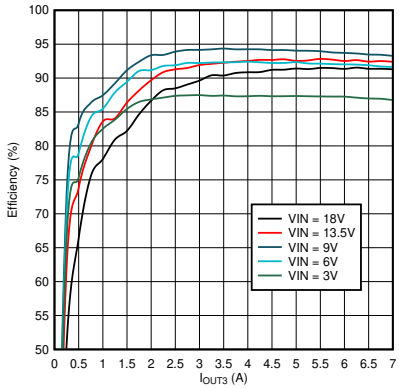

Figure 5-4. Efficiency vs. I_{OUT3} (DEM, I_{OUT2} = 0 A)

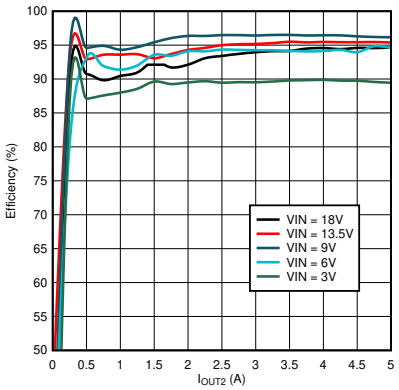

Figure 5-5. Efficiency vs. I_{OUT2} (Skip mode, I_{OUT3} = 0 A)

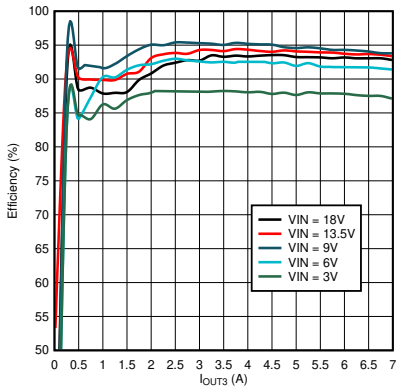

Figure 5-6. Efficiency vs. I_{OUT3} (Skip mode, I_{OUT2} = 0 A)

5.2 Thermal Performance

Figure 5-7 and Figure 5-8 illustrate the EVM thermal images. There is no airflow flow over the EVM.

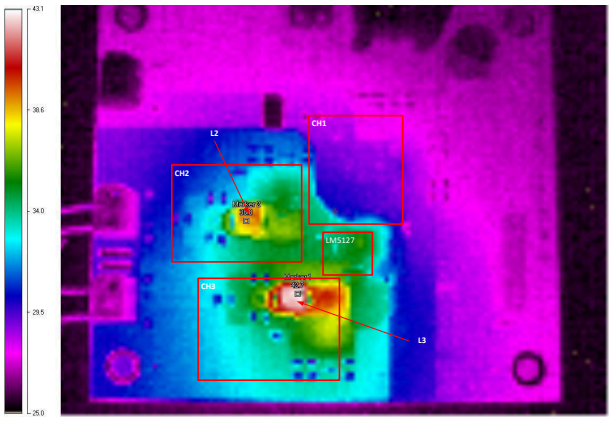

Figure 5-7. Thermal Performance V_{IN} = 13.5 V, I_{OUT2} =5 A, I_{OUT3} = 7 A

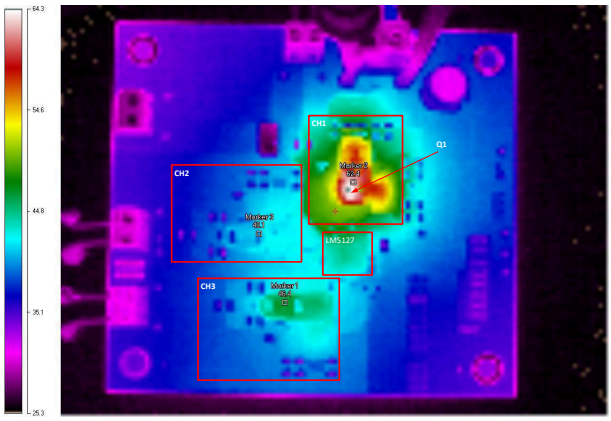

Figure 5-8. Thermal performance V_{IN} = 3 V, I_{OUT2} =5 A, I_{OUT3} = 7 A

5.3 Steady State

Figure 5-9 through Figure 5-14 show the steady state waveforms for the EVM.

CH1 Boost

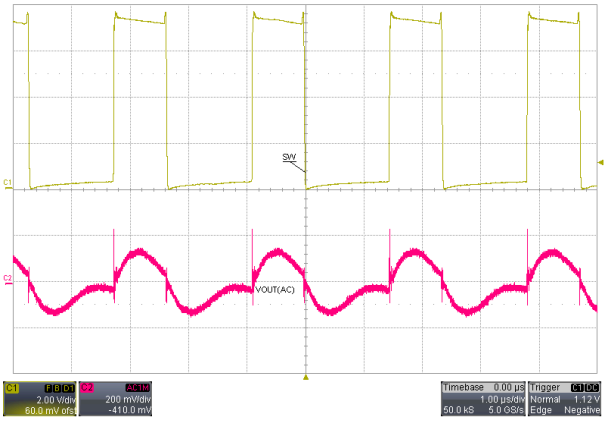

Figure 5-9. Steady State CH1, V_{IN} = 3 V, I_{OUT1} = 10 A

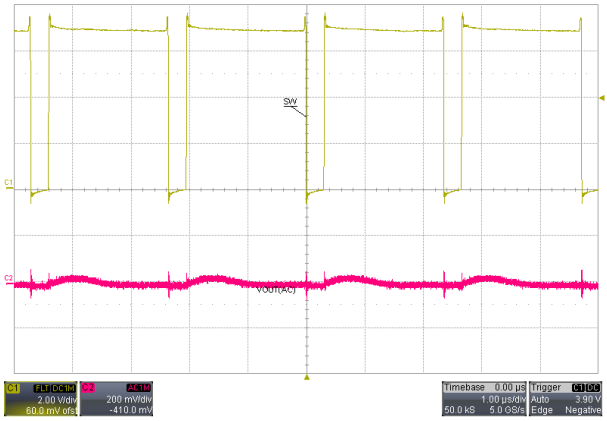

Figure 5-10. Steady State CH1, V_{IN} = 6 V, I_{OUT1} = 10 A

CH2 Buck

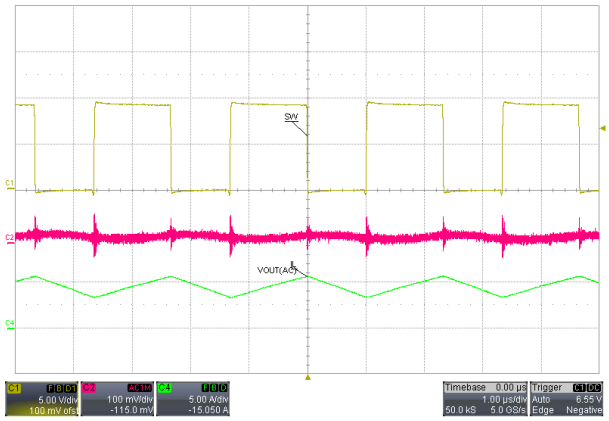

Figure 5-11. Steady State CH2, V_{IN} = 6 V, I_{OUT2} = 5 A

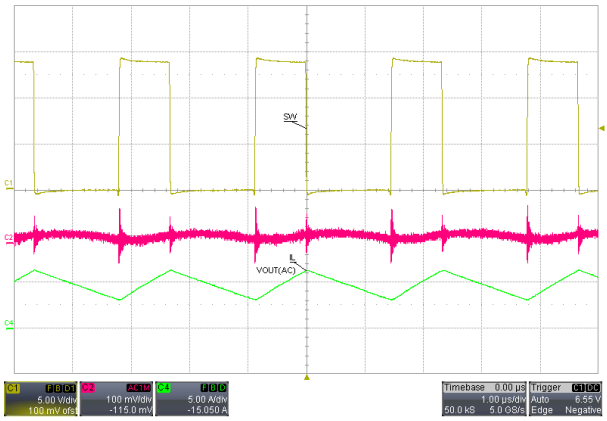

Figure 5-12. Steady State CH2, V_{IN} = 13.5 V, I_{OUT2} = 5 A

CH3 Buck

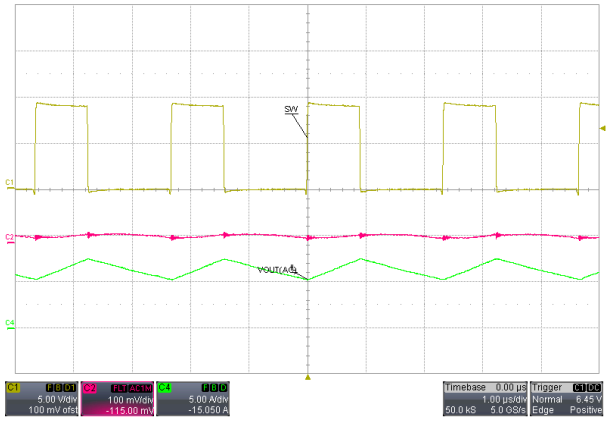

Figure 5-13. Steady State CH3, V_{IN} = 6 V, I_{OUT3} = 7 A

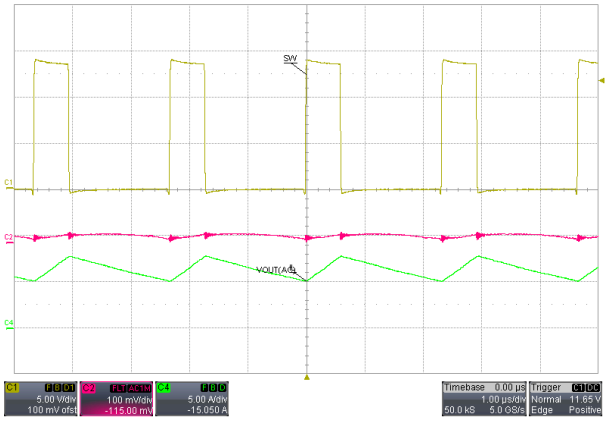

Figure 5-14. Steady State CH3, V_{IN} = 13.5 V, I_{OUT3} = 7 A

5.4 Load Transient

Figure 5-15 through Figure 5-20 show the EVM load transient waveforms.

CH1 Boost Load Transients

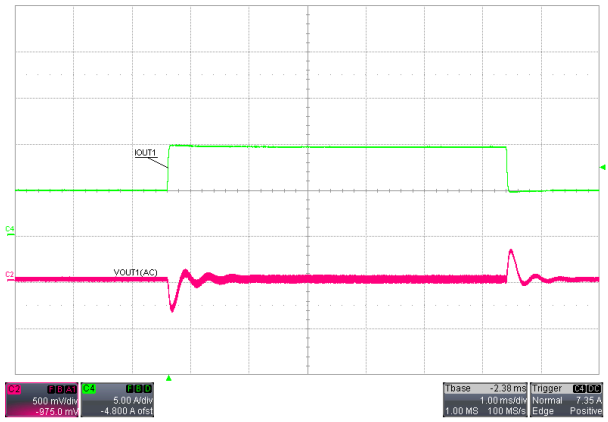

Figure 5-15. Load Transient, CH1, V_{IN} = 3 V, FPWM, I_{OUT1} = 5 A to 10 A at 1 A/µs

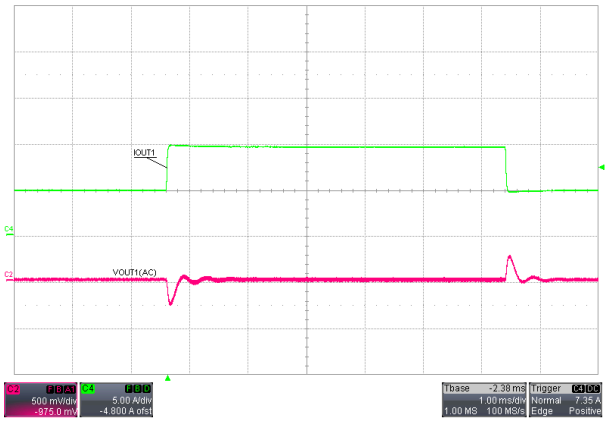

Figure 5-16. Load Transient, CH1, V_{IN} = 6 V, FPWM, I_{OUT1} = 5 A to 10 A at 1 A/µs

CH2 Buck Transients

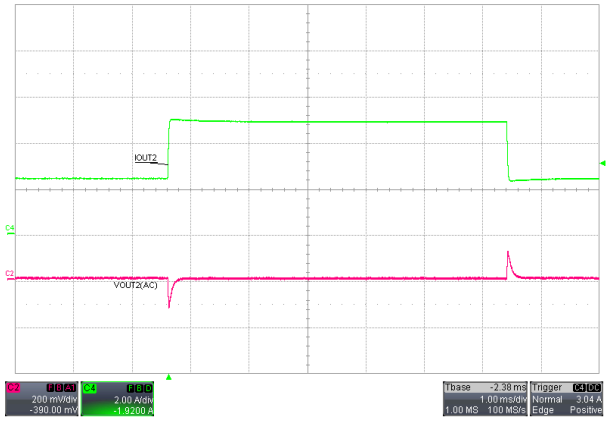

Figure 5-17. Load Transient, CH2, V_{IN} = 6 V, I_{OUT2} = 2.5 A to 5 A at 1 A/µs

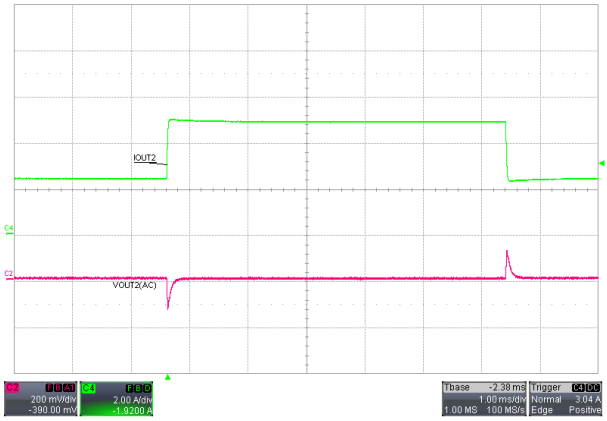

Figure 5-18. Load Transient, CH2, V_{IN} = 13.5 V, I_{OUT2} = 2.5 A to 5 A at 1 A/µs

CH3 Load Transients

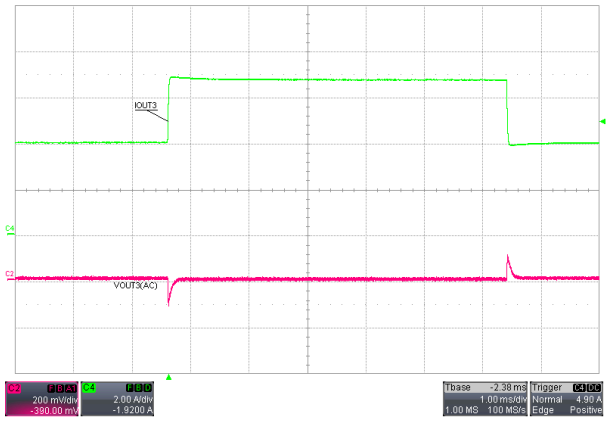

Figure 5-19. Load Transient, CH3, V_{IN} = 6 V, I_{OUT3} = 4 A to 7 A at 1 A/µs

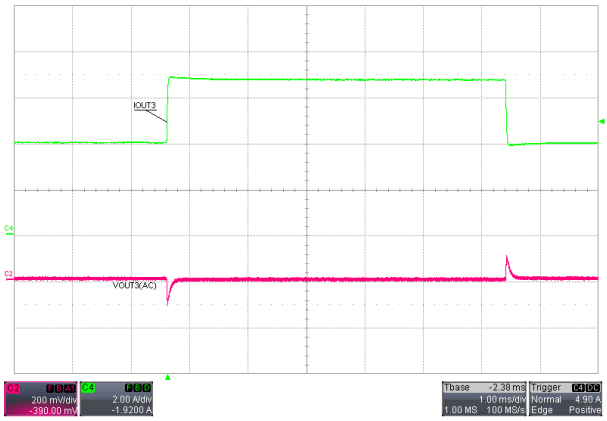

Figure 5-20. Load Transient, CH3, V_{IN} = 13.5 V, I_{OUT3} = 4 A to 7 A at 1 A/µs

5.5 Line Transient Responses

Section 5.5 presents voltage transients on the input voltage rail (VCH1A). In Figure 5-21 and Figure 5-22, all three channels are enabled, channel 2 is loaded at 5 A and channel 3 is loaded as 7 A.

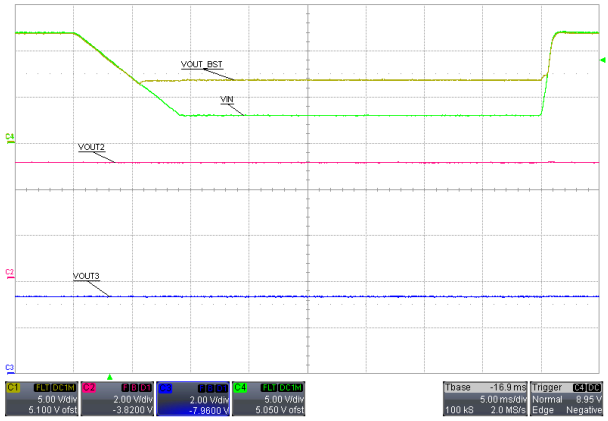

Figure 5-21. Cold-Crank Response to V_{IN} = 3 V, I_{OUT2} = 5 A, I_{OUT3} = 7 A

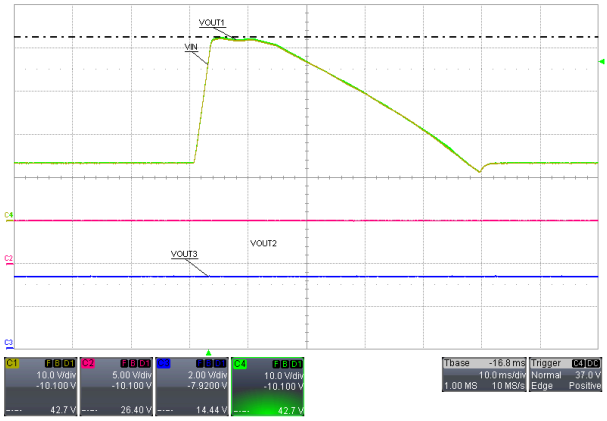

Figure 5-22. Load Dump Response to V_{IN} = 42 V, I_{OUT2} = 5 A, I_{OUT3} = 7 A

6 Schematics, PCB Layers, and Bill of Materials

The following sections contain the schematics, PCB layers, and bill of materials for this evaluation module.

6.1 Schematics

Figure 6-1 and Figure 6-2 show the EVM schematics.

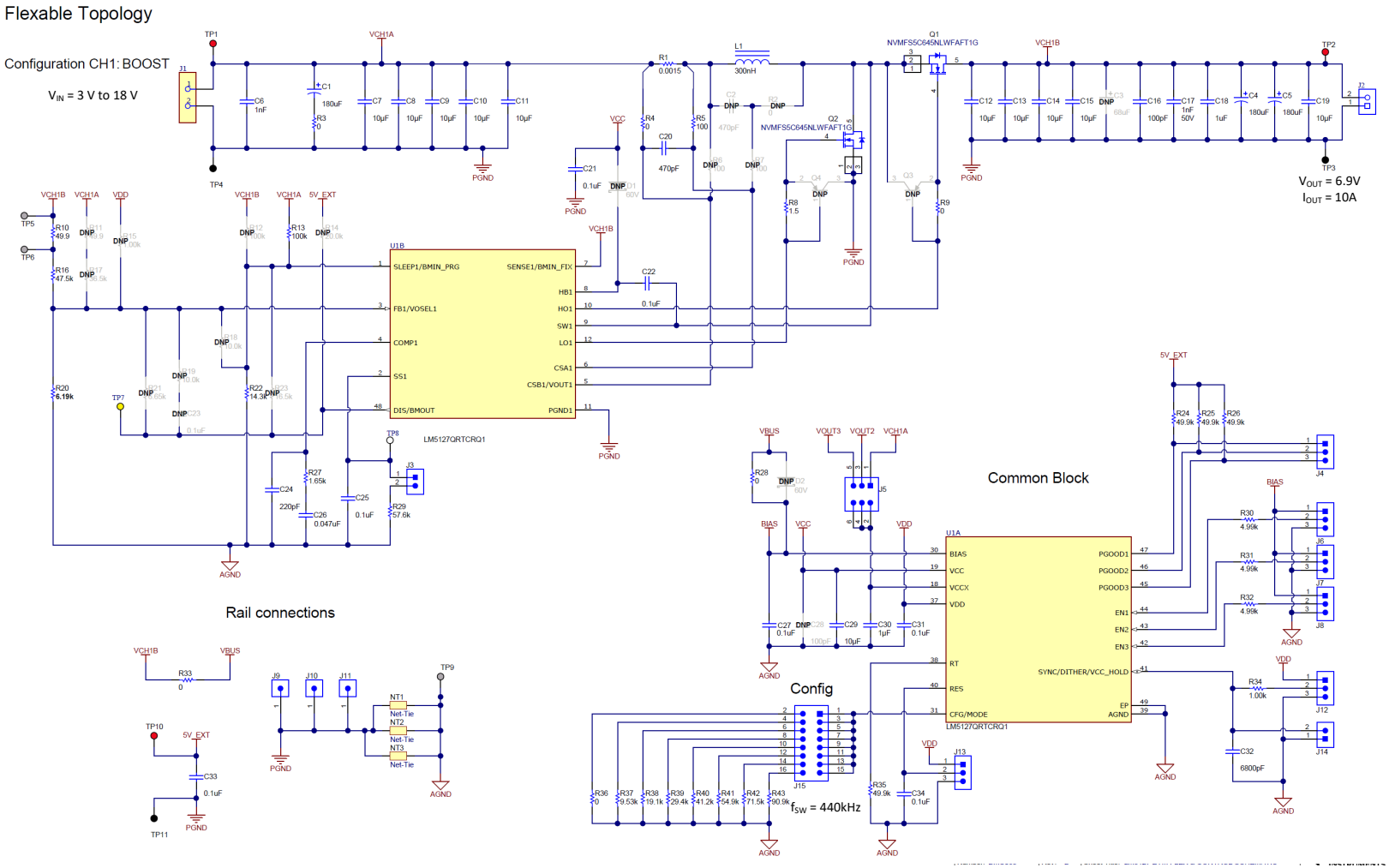

Figure 6-1. Schematic Page 1

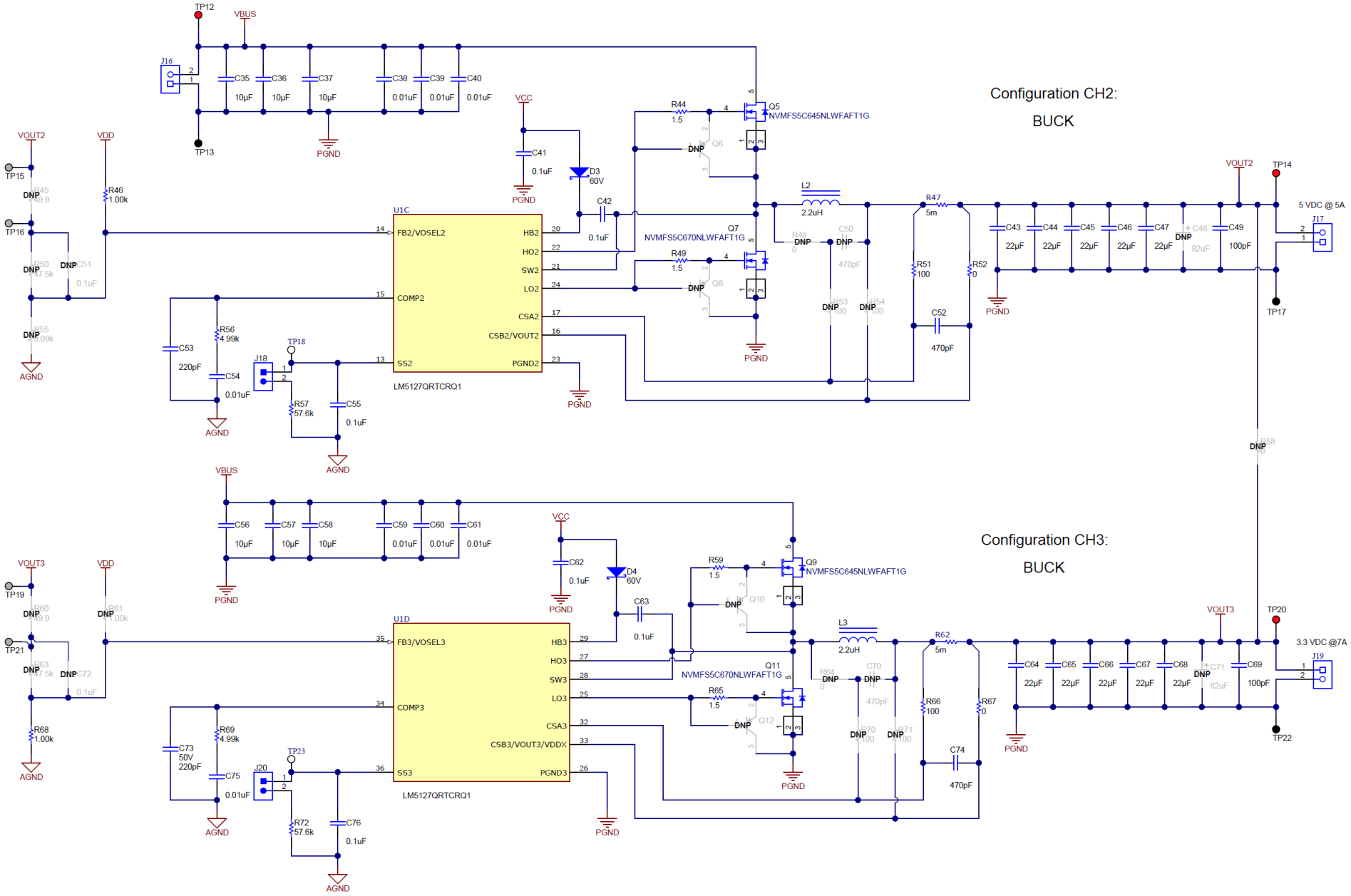

Figure 6-2. Schematic Page 2

6.2 PCB Layers

Figure 6-3 through Figure 6-10 illustrate the EVM PCB layout images.

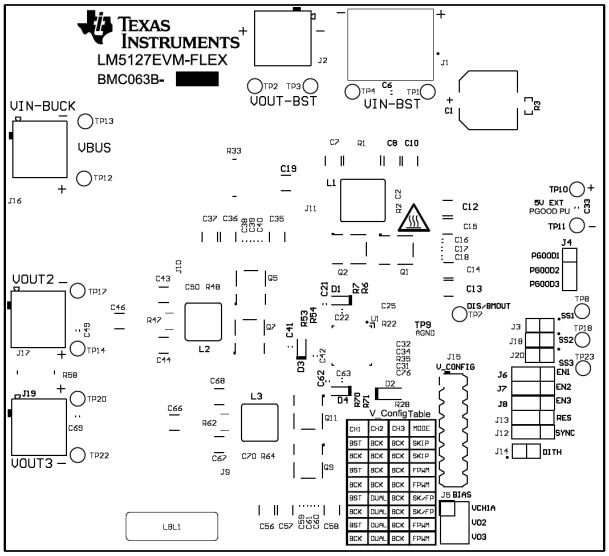

Figure 6-3. Layout: Top Silk Screen

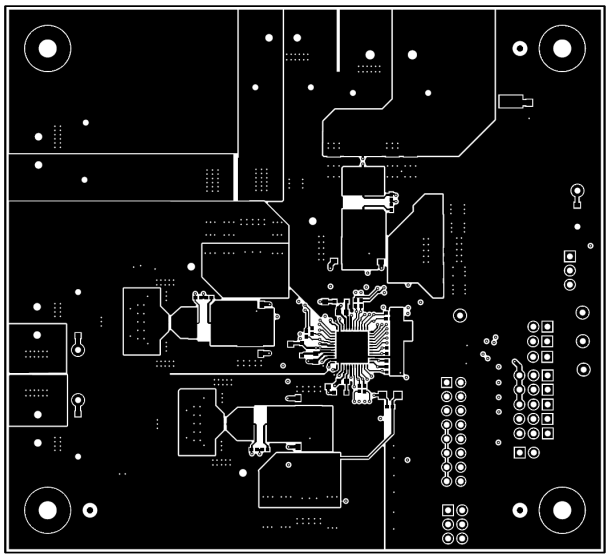

Figure 6-4. Layout: Top Layer

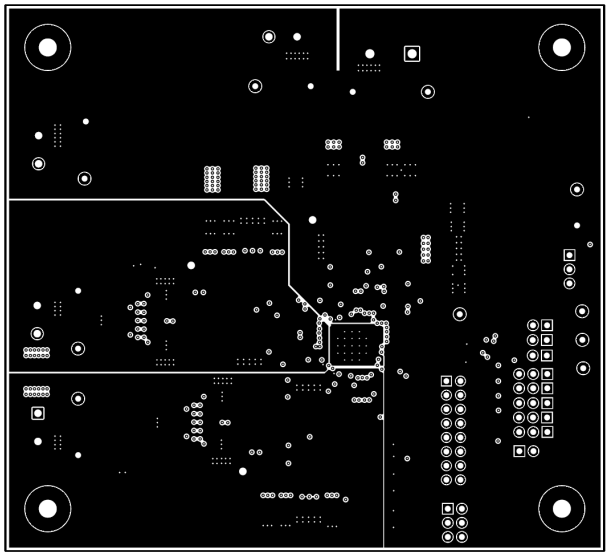

Figure 6-5. Layout: Signal Layer 1

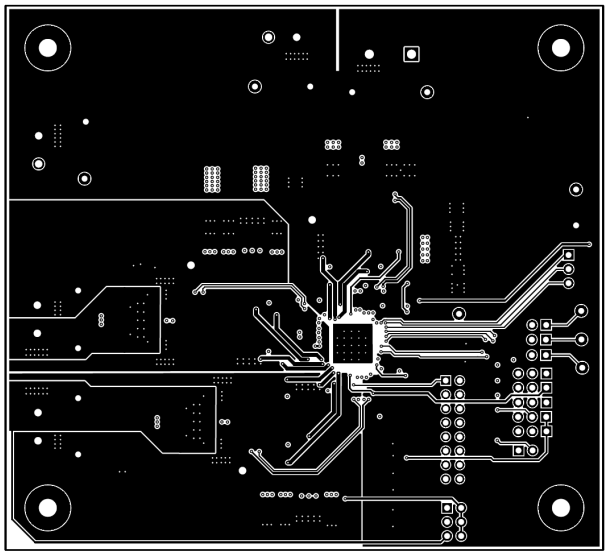

Figure 6-6. Layout: Signal Layer 2

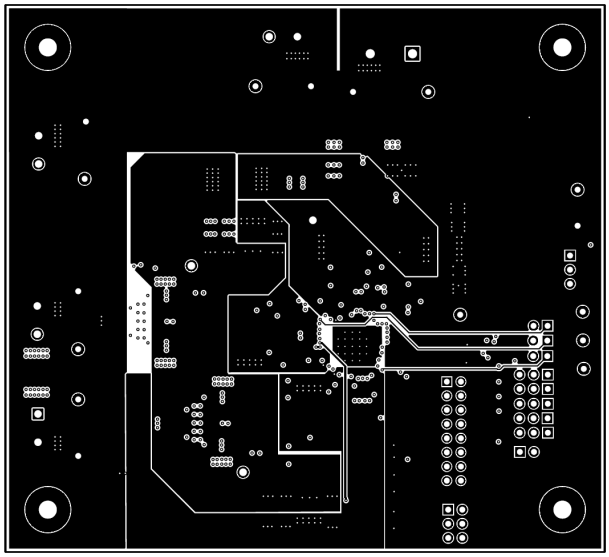

Figure 6-7. Layout: Signal Layer 3

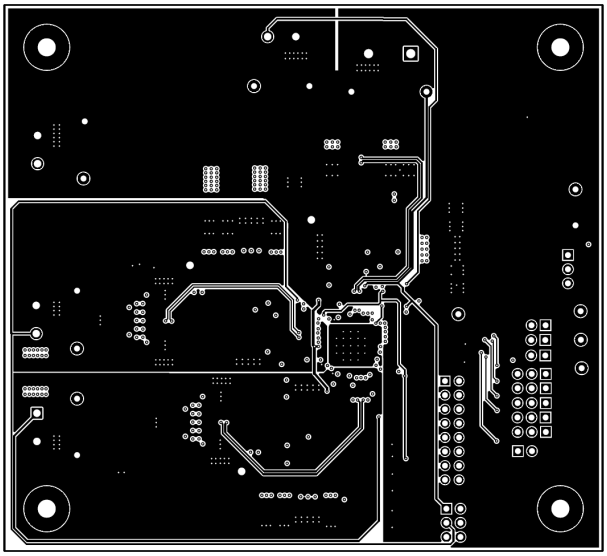

Figure 6-8. Layout: Signal Layer 4

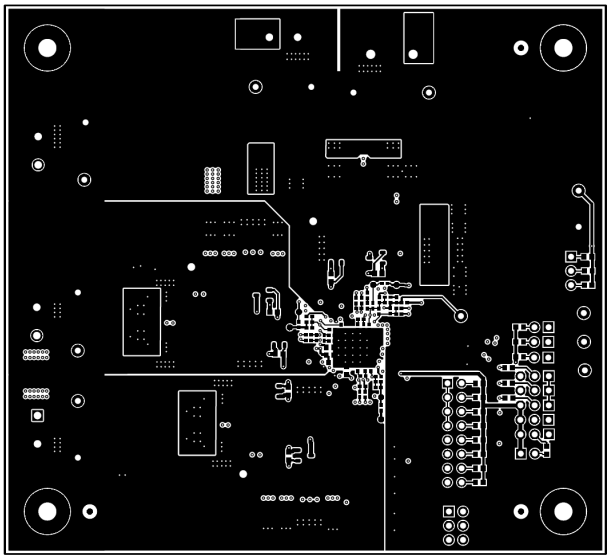

Figure 6-9. Layout: Bottom Layer

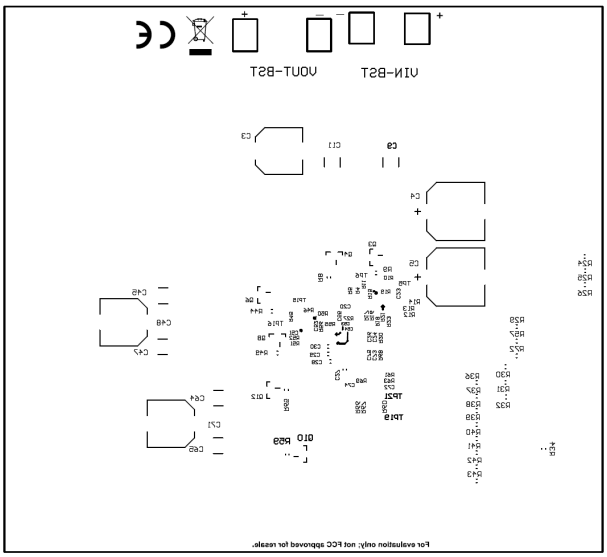

Figure 6-10. Layout: Bottom Silk Screen

6.3 Bill of Materials

Table 6-1 lists the EVM bill of materials.

Table 6-1. Bill of Materials

Reference Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C1, C4, C5	3	180uF	CAP, Aluminum Polymer, 180 uF, 50 V, +/- 20%, 0.019 ohm, SMD, 2-Leads, Dia 10.5mm, Pin Spacing 8mm SMD	SMD, 2-Leads, Dia 10.5mm, Pin Spacing 8mm	PCR1H181MCL1GS	Nichicon
C6, C17	2	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603X102K5RACTU	Kemet
C7, C8, C9, C10, C11, C12, C13, C14, C15, C19, C35, C36, C37, C56, C57, C58	16	10uF	CAP, CERM, 10 µF, 50 V,+/- 10%, X7S, AEC-Q200 Grade 1, 1210	1210	CGA6P3X7S1H106K250AE	TDK
C16, C49, C69	3	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C101J5GACTU	Kemet
C18, C30	2	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
C20, C52, C74	3	470pF	CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	GCM155R71H471KA37D	MuRata
C21, C22, C27, C33, C41, C42, C62, C63	8	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R1H104K080AA	TDK
C24	1	220pF	CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0402	0402	04025A101FAT2A	TDK
C25, C31, C34, C55, C76	5	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	C0402C104K4RACAUTO	Kemet
C26	1	0.047uF	CAP, CERM, 0.047 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H473K050BB	TDK
C29	1	10uF	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, AEC-Q200 Grade 2, 0603	0603	GRT188C81C106ME13D	MuRata
C32	1	6800pF	CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B2X7R1H682K050BA	TDK
C38, C39, C40, C59, C60, C61	6	0.01uF	CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R2A103K080AA	TDK
C43, C44, C45, C46, C47, C64, C65, C66, C67, C68	10	22uF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	C1210C226K3RAC7800	Kemet
C53, C73	2	220pF	CAP, CERM, 220 pF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402	CGA2B2C0G1H221J050BA	TDK
C54, C75	2	0.01uF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0402	0402	520L103KT16T	AT Ceramics
D3, D4	2	60V	Diode, Schottky, 60 V, 1 A, SOD-323F	SOD-323F	PMEG6010CEJ,115	Nexperia
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5	Standoff	1902C	Keystone

Table 6-1. Bill of Materials (continued)

Reference Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
J1	1		TERM BLOCK 2POS 7.62MM PCB HORIZ	HDR2	T70243500000G	Amphenol Anytek
J2, J16, J17, J19	4		Terminal Block, 5.08 mm, 2x1, TH	2POS Terminal Block	1715721	Phoenix Contact
J3, J14, J18, J20	4		Header, 100mil, 2x1, Tin, TH	Header 2x1	90120-0122	Molex
J4, J6, J7, J8, J12, J13	6		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
J5	1		Header, 100mil, 3x2, Tin, TH	3x2 Header	PEC03DAAN	Sullins Connector Solutions
J9, J10, J11	3		TEST POINT SLOTTED .118	Test point, TH Slot Test point	1040	Keystone
J15	1		Header, 2.54mm, 8x2, Gold, TH	Header, 2.54mm, 8x2, TH	PRPC008DAAN-RC	Sullins Connector Solutions
L1	1	300nH	Inductor, Shielded, Composite, 300 nH, 27.6 A, 0.00175 ohm, SMD	XAL7030	XAL7030-301MEB	Coilcraft
L2, L3	2	2.2uH	Inductor, Shielded, Composite, 2.2 uH, 16 A, 0.0067 ohm, AEC-Q200 Grade 1, SMD	6.36x6.56mm	XEL6060-222MEB	Coilcraft
Q1, Q2, Q5, Q9	4	60V	MOSFET, N-CH, 60 V, 100 A, AEC-Q101, SO-8FL	SO-8FL	NVMFS5C645NLWFAFT1G	ON Semiconductor
Q7, Q11	2	60V	MOSFET, N-CH, 60 V, 17 A, AEC-Q101, SO-8FL	SO-8FL	NVMFS5C670NLWFAFT1G	ON Semiconductor
R1	1	0.0015	RES, 0.0015, 5%, 2 W, 2512 WIDE	2512 WIDE	PML100HZPJV1L5	Rohm
R3, R9, R36	3	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R4, R28, R52, R67	4	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R5, R51, R66	3	100	RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100RJNED	Vishay-Dale
R8, R44, R49, R59, R65	5	1.5	RES, 1.5, 5%, 0.1 W, 0603	0603	ERJ-3GEYJ1R5V	Panasonic
R10	1	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF49R9X	Panasonic
R13	1	100k	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R16	1	47.5k	RES, 47.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040247K5FKED	Vishay-Dale
R20	1	6.19k	RES, 6.19 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K19FKED	Vishay-Dale
R22	1	14.3k	RES, 14.3 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040214K3FKED	Vishay-Dale
R24, R25, R26	3	49.9k	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349K9FKEA	Vishay-Dale
R27	1	1.65k	RES, 1.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K65FKED	Vishay-Dale
R29, R57, R72	3	57.6k	RES, 57.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060357K6FKEA	Vishay-Dale

Table 6-1. Bill of Materials (continued)

Reference Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
R30, R31, R32	3	4.99k	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K99FKEA	Vishay-Dale
R33	1	0	RES, 0, 5%, 2 W, 2512 WIDE	2512 WIDE	RCL12250000Z0EG	Vishay Draloric
R34	1	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R35	1	49.9k	RES, 49.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040249K9FKED	Vishay-Dale
R37	1	9.53k	RES, 9.53 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06039K53FKEA	Vishay-Dale
R38	1	19.1k	RES, 19.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060319K1FKEA	Vishay-Dale
R39	1	29.4k	RES, 29.4 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060329K4FKEA	Vishay-Dale
R40	1	41.2k	RES, 41.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060341K2FKEA	Vishay-Dale
R41	1	54.9k	RES, 54.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060354K9FKEA	Vishay-Dale
R42	1	71.5k	RES, 71.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060371K5FKEA	Vishay-Dale
R43	1	90.9k	RES, 90.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060390K9FKEA	Vishay-Dale
R46, R68	2	1.00k	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00FKED	Vishay-Dale
R47, R62	2	5m	5 mOhms ±1% 1W Chip Resistor Wide 0805 (2012 Metric), 0508 Automotive AEC-Q200, Current Sense Metal Foil	0805_WIDE	KRL2012E-M-R005-F-T5	Susumu
R56, R69	2	4.99k	RES, 4.99 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K99FKED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	7		CONN JUMPER S2 (1 x 2) Position Shunt Connector Black Open Top 0.100	JUMPER	QPC02SXGN-RC	Sullins
TP1, TP2, TP10, TP12, TP14, TP20	6		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP3, TP4, TP11, TP13, TP17, TP22	6		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP7	1		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP8, TP18, TP23	3		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone

Table 6-1. Bill of Materials (continued)

Reference Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
U1	1		2.2MHz Wide VIN Automotive Front-stage Multi-rail DC/DC	VQFN48	LM5127QRTCRQ1	Texas Instruments

7 EVM Modifications

Section 7 describes possible modifications outside of the default configuration that can be used to further evaluate the LM5127-Q1. These configurations include: channel 1 configuration as a buck controller, channel 2 and channel 3 configuration to a dual phase interleaved buck controller.

7.1 Configure Channel 1 as a Buck Controller

Section 7.1 describes how to configure channel 1 as a buck controller. Figure 7-1 shows the typical application when channel 1 is configured as a buck controller.

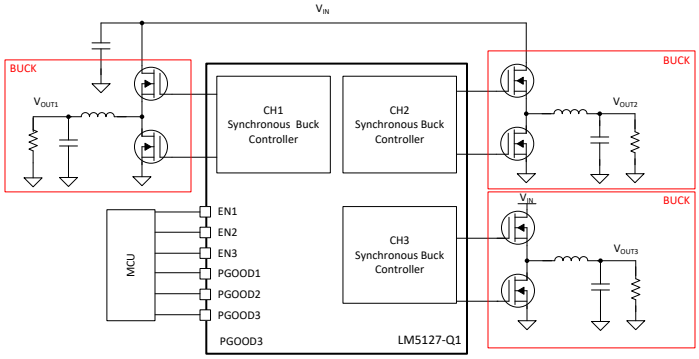

Figure 7-1. Channel 1 as Buck Controller

7.1.1 Component Modifications

Table 7-1 indicates the components that must be changed from the default configuration to configure channel 1 as a buck controller. These changes result in channel 1 producing a 5 V output, capable of providing 5 A of output current.

Table 7-1. Modifications to Configure Channel 1 a Buck Controller

Component	Action	Comment
Feedback network configuration		
R10	Do not populate	
R16	Do not populate	
R20	Do not populated	
R15	Populate with 1 kΩ	Configures VOUT1 to be 5 V
BMOUT configuration		
R12	Populate with 100 kΩ	
R22	Populate with 30.1 kΩ	Sets BMIN_PRG to ~ 6.5 V
R13	Do not populate	
R14	Populate with 20 kΩ	
Compensation configuration		
R27	4.99 kΩ	Same component as R56
C26	10 nF	Same component as C54
C24	220 pF	Similar component as C53
Power-train component configuration		
D1	Populate	Similar component as D3
R1	5 mΩ	Similar component as R47
L1	2.2 µH	Same component as L2
C7, C8, C9, C10, C11	22 µF	Similar component as C43
C1	Do not populate	
C6	100 pF	Similar component as C49

7.1.2 CFG/MODE Pin Selection

Table 7-2 shows the possible CFG/MODE pin settings to configure channel 1 as a buck . If a dual phase buck configuration for channel 2 and channel 3 is required see Section 7.2 for details on the proper configuration. For proper test setup see Section 7.3

Table 7-2. CFG/MODE Pin Connections for Channel 1 Configured as a Buck Controller (J15)

PIN	Pin Connection	CH1	CH2	CH3	Switching Mode
2 (9.53kΩ)	3 to 4	Buck	Single Phase Buck	Single Phase Buck	Skip
4 (29.4kΩ)	7 to 8	Buck			FPWM/DEM
6 (54.9kΩ)	11 to 12	Buck	Dual Phase Buck		Skip
8 (90.9kΩ)	15 to 16	Buck			FPWM/DEM

7.2 Configure Channel 2 and Channel 3 as a Dual Phase Buck Controller

Section 7.2 describes how to configure channel 2 and channel 3 as a dual phase interleaved buck controller. Figure 7-2 and Figure 7-3 show the typical applications when channel 2 and channel 3 is configured as a dual phase buck controller.

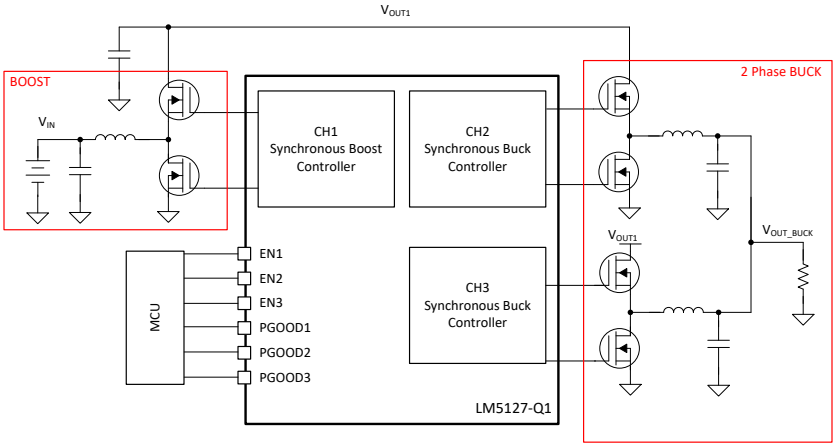

Figure 7-2. Channel 1 as a Boost, Channel 2 and Channel 3 as Dual Phase Buck Controller

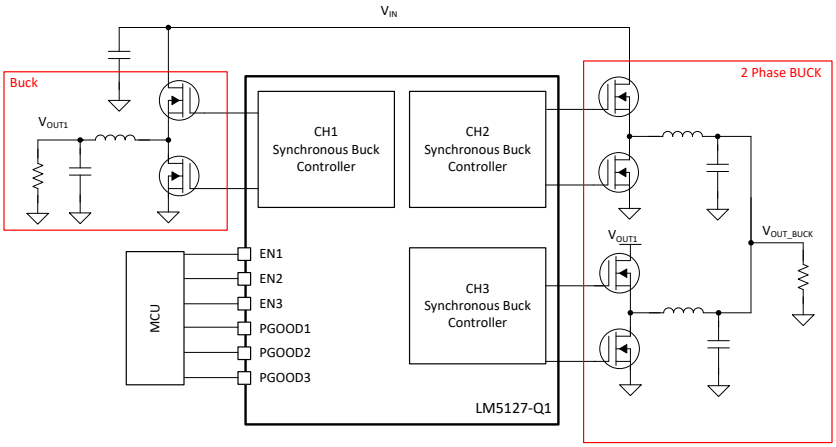

Figure 7-3. Channel 1 as a Buck, Channel 2 and Channel 3 as a Dual Phase Buck Controller

7.2.1 Component Modifications

Table 7-3 indicates the components that must be changed from the default configuration to configure channel 2 and channel 3 as a dual phase buck controller. These changes result in channel 2 and channel 3 producing a 3.3 V output, capable of providing 14 A of output current.

Table 7-3. Modifications to Configure Channel 2 and Channel 3 as Dual Phase Buck Controller

Component	Action	Comment
Feedback network configuration		
R46	Do not populate	
R55	Populate with 1 kΩ	Configures output voltage to be 3.3 V
R68	0 Ω	Short FB3 to ground
Compensation configuration		
R69	Do not populate	
C75	Do not populate	
C73	Do not populate	
Soft-Start configuration		
C76	Do not populate	
J20	Open	J18 can be used to enable diode emulation mode
Powertrain component configuration		
R58	Short with 0 Ω resistor	Connects the output of channel 2 and channel

7.2.2 CFG/MODE Pin Selection

Table 7-4 shows the possible CFG/MODE pin settings to configure channel 2 and channel 3 as a dual phase buck . If a buck configuration for channel 1 is required see Section 7.1 for details on the proper configuration of channel 1. For proper test setup see Section 7.3

Table 7-4. CFG/MODE Pin Connections for Channel 2 and Channel 3 Configured as a Dual Phase Buck Controller (J15)

Configuration	Pin Connection	CH1	CH2	CH3	Switching Mode
5 (41.2kΩ)	9 to 10	Boost	Dual Phase Buck		CH1: Skip CH2/CH3: FPWM/DEM
6 (54.9kΩ)	11 to 12	Buck			
7 (71.5kΩ)	13 to 14	Boost			FPWM/DEM
8 (90.9kΩ)	15 to 16	Buck			

7.3 EVM Modification Test Setups

Figure 7-4 through Figure 7-6 show how to properly setup the evaluation module for the configurations described in Section 7.1 and Section 7.2.

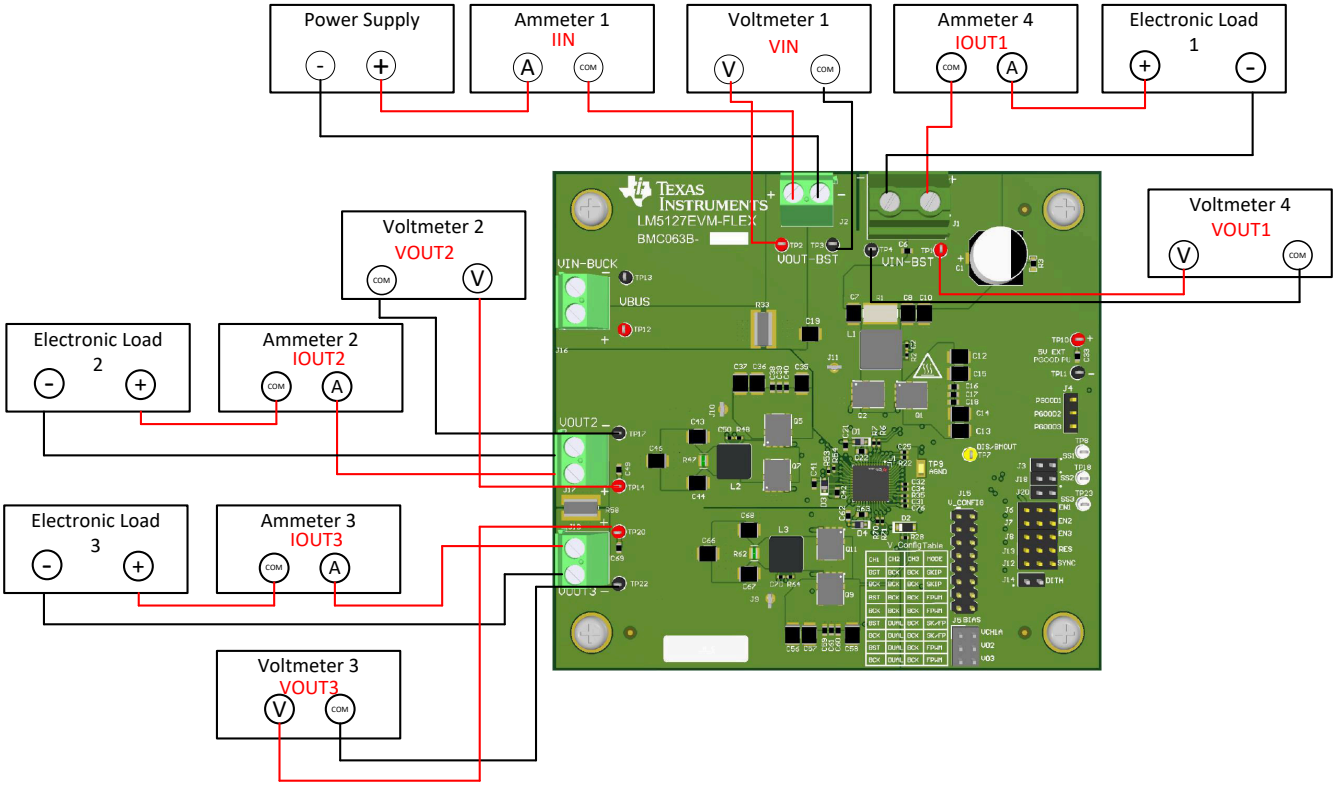

Figure 7-4. Channel 1 as a Buck Controller, Channel 2 and Channel 3 as Independent Buck Controllers

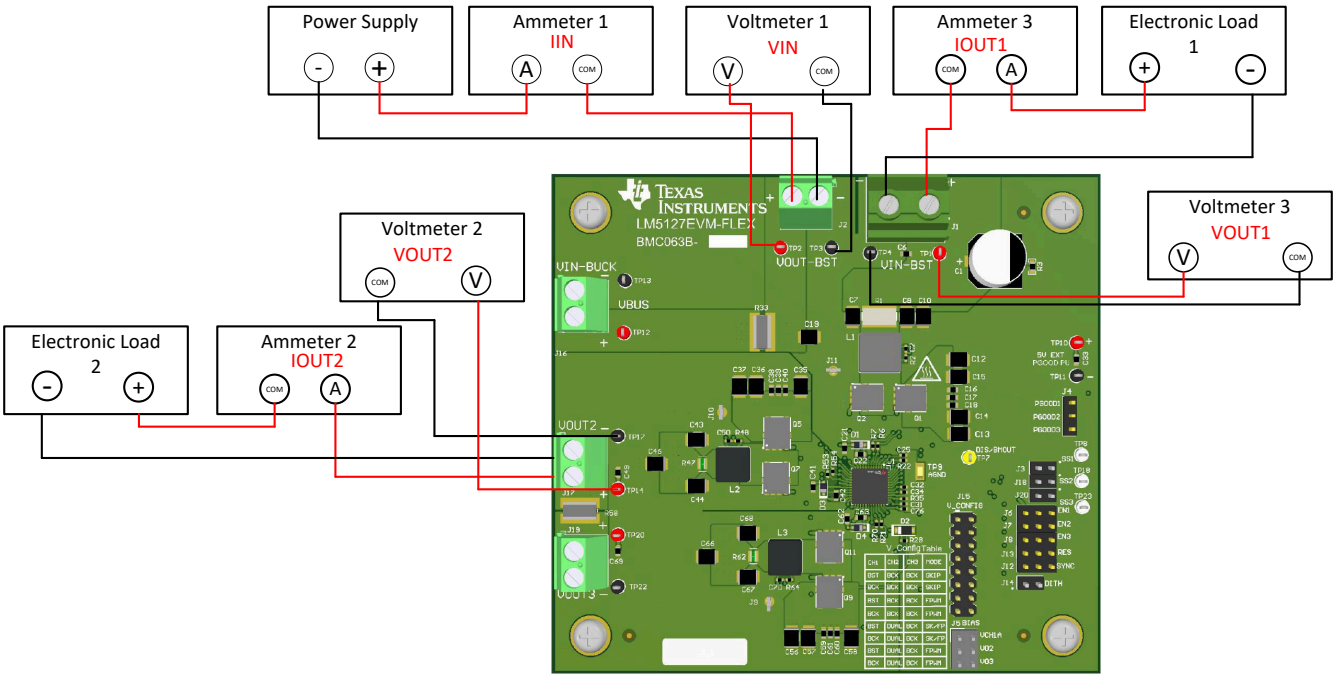

Figure 7-5. Channel 1 as a Buck Controller, Channel 2 and Channel 3 as Dual Phase Buck Controller

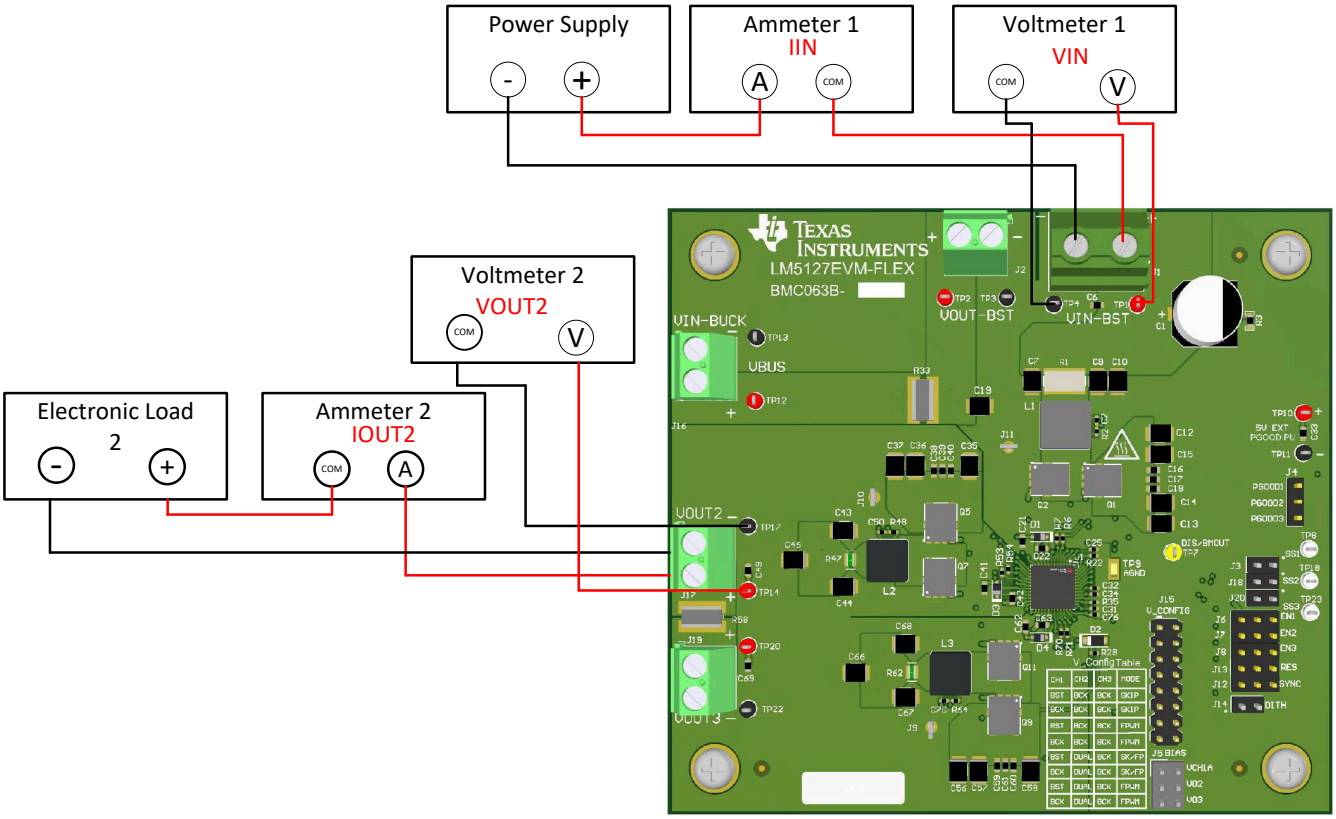

Figure 7-6. Channel 1 as a Boost Controller, Channel 2 and Channel 3 as a Dual Phase Buck Controller

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2020) to Revision A (December 2020)	Page
• Updated schematics	16
• Updated bill of materials	20
• Added EVM Modifications	24

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