User's Guide

TPS54KC23EVM Step-Down Converter Evaluation Module

ABSTRACT

This user's guide contains information for the TPS54KC23EVM evaluation module and the TPS54KC23 DC/DC converter. Also included are the performance characteristics, schematic, and bill of materials for the TPS54KC23EVM.

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1 Introduction

1.1 Background

The TPS54KC23 DC/DC converter are synchronous buck converters designed to provide up to a 30-A output. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

The high-side and low-side MOSFETs are incorporated inside the TPS54KC23 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54KC23 to achieve high efficiencies and helps to keep the junction temperature low at the rated output current. An external divider allows for an adjustable output voltage. The TPS54KC23 MSEL pin provides selectable switching frequency, light load operation mode, and internal compensation. Current limit setting and soft start configuration are set via ILIM and SS pins respectively. Lastly, the TPS54KC23 includes an enable pin and a power good output which can be used for sequencing multiple regulators.

This evaluation module includes two designs with the TPS54KC23. The first design (U1) is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54KC23 regulator. The small area design fits within 250 mm^2. The second design (U2) is designed to demonstrate the high efficiency that can be achieved when designing with the TPS54KC23 regulator. The second design also includes jumpers that can be used to easily evaluate the features of the TPS54KC23.

Table 1-1. Input Voltage and Output Current Summary

EVM	RELATED IC	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54KC23EVM	U1	V_{IN} = 8 V to 16 V	0 A to 30 A
TPS54KC23EVM	U2	V_{IN} = 4.5 V to 16 V	0 A to 30 A

1.2 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS54KC23EVM. Observe all safety precautions.

WARNING

The TPS54KC23EVM can become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board and can result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

1.3 Performance Characteristics Summary

A summary of the TPS54KC23EVM performance characteristics is provided in Table 1-2 and Table 1-3. The TPS54KC23EVM is designed and tested for V_{IN} = 8 V to 16 V for U1 and V_{IN} = 4.5 V to 16 V for U2. Characteristics are given for an input voltage of V_{IN} = 12 V and output voltage of 0.8 V, unless otherwise specified. The ambient temperature is room temperature (20°C to 25°C) for all measurements, unless otherwise noted.

Table 1-2. TPS54KC23EVM Small Size (U1) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			8	12	16	V
Input current	V_{IN} = 8 V, I_O = 30 A			3.9		A
V_{IN} start voltage	Set by EN pin resistor divider			7.18		V
V_{IN} stop voltage	Set by EN pin resistor divider			5.98		V
Output voltage setpoint				0.802		V
Output current range	V_{IN} = 8 V to 16 V		0		30	A
Line and load regulation	V_{IN} = 8 V to 16 V, I_{OUT} = 0 A to 30 A			±0.31		%
Load transient response	I_{OUT} = 5 A to 20 A	Voltage change		-15		mV
		Recovery time		68		µs
	I_{OUT} = 5 A to 20 A	Voltage change		20		mV
		Recovery time		64		µs
Input ripple voltage	I_{OUT} = 30 A			864		mVPP
Output ripple voltage	I_{OUT} = 30 A			20		mVPP
Output rise time	Set by SS pin capacitor			139		µs
Current limit	Set by ILIM pin resistor			30.6		A
Switching frequency (f_{SW})	Set by MSEL pin resistor			1400		kHz
Peak efficiency	I_{OUT} = 15 A			83.3		%
IC case temperature	I_{OUT} = 30 A, 15-minute soak			128		°C

Table 1-3. TPS54KC23EVM High Efficiency (U2) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			4.5	12	16	V
Input current	V_{IN} = 4.5 V, I_{OUT} = 30 A			6.5		A
V_{IN} start voltage	Set by EN pin resistor divider			3.84		V
V_{IN} stop voltage	Set by EN pin resistor divider			3.20		V
Output voltage setpoint				0.802		V
Output current range	V_{IN} = 4.5 V to 16 V		0		30	A
Line and load regulation	V_{IN} = 4.5 V to 16 V, I_{OUT} = 0 A to 30 A			±0.4%		
Load transient response	I_{OUT} = 5 A to 20 A	Voltage change		–4		mV
		Recovery time		54		µs
	I_{OUT} = 5 A to 20 A	Voltage change		4		mV
		Recovery time		55		µs
Input ripple voltage	I_{OUT} = 30 A			472		mVPP
Output ripple voltage	I_{OUT} = 30 A			4.8		mVPP
Output rise time	Set by SS pin capacitor			944		µs
Current limit	Set by ILIM pin resistor			30.6		A
Switching frequency (f_{SW})	Set by MSEL pin resistor, J8 short pins 3 and 4			800		kHz
Peak efficiency	I_{OUT} = 8 A			89.1		%
IC case temperature	I_{OUT} = 30 A, 15-minute soak			97		°C

2 Configurations and Modifications

These evaluation modules are designed to provide access to the features of the TPS54KC23. The U2 design provides jumpers for testing different configurations. Jumper selections must be made prior to enabling the TPS54KC23.

If a desired configuration is not available, then some modifications can be made to this module. When modifications are made to the components on the EVM, the internal compensation option selected with the MSEL pin resistor needs to be changed. Changes to the f_{SW}, output voltage, output inductor, and output capacitors can require a change in the compensation. TPS54KC23 data sheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, f_{SW}, and inductance. Verify that all components have sufficient voltage and current ratings.

2.1 Output Voltage

In the U1 design, the output voltage is set by the resistor divider network of R2 (R_{FBT}) and R6 (R_{FBB}). R6 is fixed at 8.25 kΩ to set the FB divider current at approximately 61 µA. The output voltage is set to 0.8V as default. To change the output voltage of the EVM, the value of resistor R2 must change. Changing the value of R2 can change the output voltage above the 0.5-V reference voltage (V_{REF}). The value of R2 for a specific output voltage can be calculated using Equation 1.

In the U2 design, the output voltage is set by the resistor divider network of R15 (R_{FBT}) and R12 (R_{FBB}). R15 is fixed at 8.25 kΩ to set the FB divider current at approximately 61 µA. The output voltage is set to 0.8V as default. To change the output voltage of the EVM, the value of resistor R12 must change. Changing the value of R12 can change the output voltage above the 0.5-V reference voltage (V_{REF}). The value of R12 for a specific output voltage can be calculated using Equation 1. After changing R12, the feed forward capacitor (C51) also needs to be changed.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

2.2 Frequency and Operation Mode Setting (MSEL Pin)

In the U2 design, jumper J8 can change between MSEL pin selections shown in Table 2-1. If the desired option is unavailable, then change one of the resistors to the value that sets the desired option.

In the U1 design, change the MSEL resistor to the value which sets the desired option.

Table 2-1. MSEL Pin Selection

JUMPER SETTING	MSEL RESISTOR (kΩ)	OPERATION UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)	RAMP
1 to 2 pin shorted	0	FCCM	800	RAMP4
3 to 4 pin shorted	4.99	FCCM	800	RAMP3
5 to 6 pin shorted	7.50	FCCM	800	RAMP2
7 to 8 pin shorted	10.5	FCCM	800	RAMP1
9 to 10 pin shorted	56.2	Skip-mode	800	RAMP4
11 to 12 pin shorted	64.9	Skip-mode	800	RAMP3
13 to 14 pin shorted(1)	75.0	Skip-mode	800	RAMP2
15 to 16 pin shorted	86.6	Skip-mode	800	RAMP1

(1) Default Setting

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54KC23EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes. Measurements are taken with the following conditions unless otherwise noted.

- 12-V input
- Room temperature (20°C to 25°C)
- U1 with the default setting output voltage of 0.802 V, switching frequency of 1400 kHz, and maximum current limit setting
- U2 with the default setting output voltage of 0.802 V, switching frequency of 800 kHz, and maximum current limit setting
- With the other converter disabled

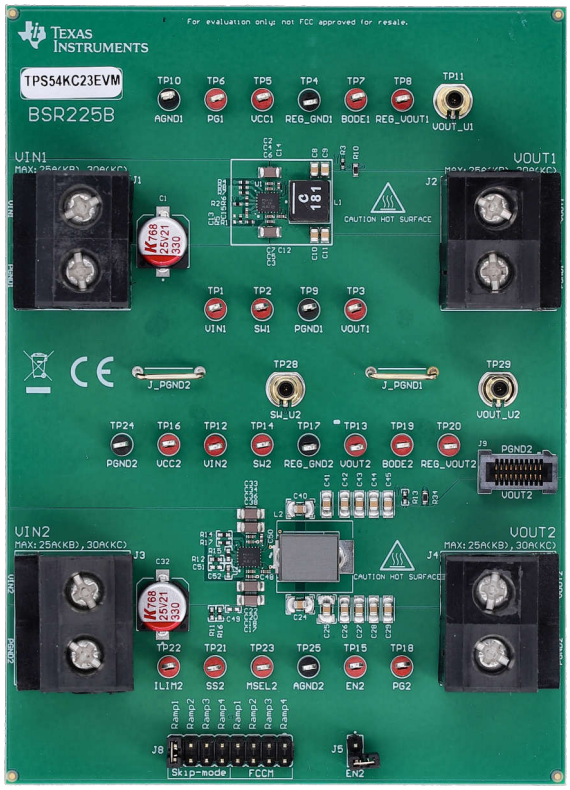

Figure 3-1. TPS54KC23EVM

3.1 Input/Output Connections

The TPS54KC23EVM is provided with input connectors, output connectors, and test points as shown in Table 3-1 and Table 3-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 10 A must be connected to the VIN and PGND terminal blocks (J1 for U1, and J3 for U2) through a pair of 18-AWG wires or better.

For U1, the load must be connected to J2 and for U2, the load must be connected to J4. A pair of 10-AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near 33 A before the TPS54KC23 goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

Table 3-1. Connectors and Jumpers

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
J1	VIN1	U1	VIN screw terminal to connect input voltage (see Table 1-1 for VIN range)
J2	VOUT1	U1	VOUT screw terminal to connect load to output
J3	VIN2	U2	VIN screw terminal to connect input voltage (see Table 1-1 for VIN range)
J4	VOUT2	U2	VOUT screw terminal to connect load to output
J5	EN2	U2	EN pin selection header: Open = (EN pin shorted to AGND) Short = (EN pin connected to VIN pin through resistor divider)
J8	-	U2	MSEL selection header. Use shunt to select MSEL resistor (see Table 2-1 for MSEL pin selection)

Table 3-2. Test Points

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
TP1	VIN1	U1	VIN test point. Use this for efficiency measurements.
TP2	SW1	U1	SW node test point
TP3	VOUT1	U1	VOUT test point
TP4	REG_GND1	U1	PGND test point. Use this for efficiency measurements.
TP5	VCC1	U1	VCC test point
TP6	PG1	U1	PGOOD output test point (pulled up to VCC pin through a 10-kΩ resistor)
TP7	BODE1	U1	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP8	REG_VOUT1	U1	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.
TP9	PGND1	U1	PGND test point. Use this for efficiency measurements.
TP10	AGND1	U1	AGND test point
TP11	VOUT_U1	U1	SMB connector to measure output voltage. When using this test point, set the scope for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP12	VIN2	U2	VIN test point
TP13	VOUT2	U2	VOUT test point
TP14	SW2	U2	SW test point
TP15	EN2	U2	EN test point
TP16	VCC2	U2	VCC test point
TP17	REG_GND2	U2	PGND test point. Use this for efficiency measurements.
TP18	PG2	U2	PGOOD output test point (pulled up to VCC pin through a 10-kΩ resistor)
TP19	BODE2	U2	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP20	REG_VOUT2	U2	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.

Table 3-2. Test Points (continued)

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
TP21	SS2	U2	SS test point
TP22	ILIM2	U2	ILIM test point
TP23	MSEL2	U2	MSEL test point
TP24	PGND2	U2	PGND test point. Use this for efficiency measurements.
TP25	AGND2	U2	AGND test point
TP28	SW_U2	U2	SMB connector to measure SW node. When using this test point, set the scope for 50-Ω termination. The combination of 50-Ω termination and 450-Ω series resistance creates a 10:1 attenuation.
TP29	VOUT_U2	U2	SMB connector to measure output voltage. When using this test point, set the scope for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.

3.2 Efficiency

Figure 3-2 through Figure 3-5 show the efficiency for both designs on the TPS54KC23EVM. The test points listed in Table 3-3 are used for the efficiency measurement. Use these test points to minimize the contribution of PCB parasitic power loss to the measured power loss.

The following are some additional test setup considerations to minimize external sources of power dissipation.

- Disable the other regulator to avoid including the switching quiescent current of the other regulator in the efficiency measurement.
- Do not measure the SW pin of U2 with TP28 while measuring the efficiency of U2. Measuring the SW pin with this test point loads this node with 500 Ω and the efficiency measurement includes the power lost in this external resistance.

Table 3-3. Efficiency Measurement Test Points

RELATED IC	TEST POINT NAME	REFERENCE DESIGNATOR	FUNCTION
U1	VIN1	TP1	Input voltage test point connected near pins of U1
	PGND1	TP9	PGND reference test point for input voltage
	REG_VOUT1	TP8	Output voltage test point near output inductor of U1
	REG_GND1	TP4	PGND reference test point for output voltage
U2	VIN2	TP12	Input voltage test point connected near pins of U2
	PGND2	TP24	PGND reference test point for input voltage
	REG_VOUT2	TP20	Output voltage test point near output inductor of U2
	REG_GND2	TP17	PGND reference test point for output voltage

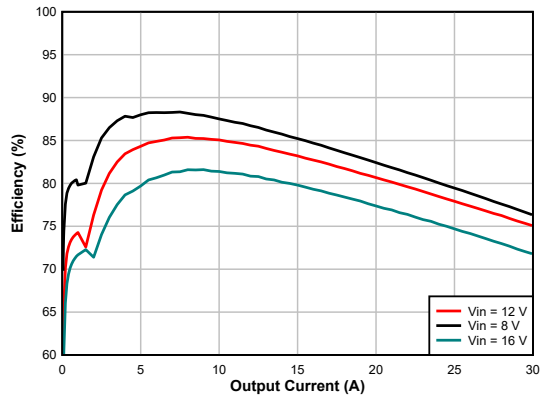

Figure 3-2. U1 Efficiency – Skip-Mode (Default)

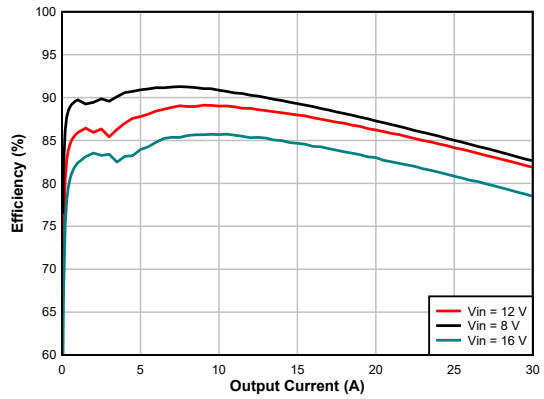

Figure 3-3. U2 Efficiency – Skip-Mode (Default)

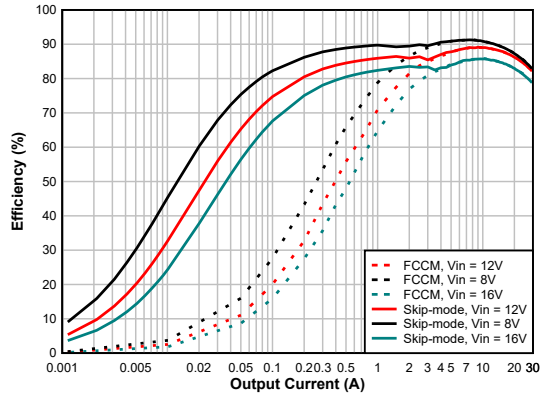

Figure 3-4. U2 Efficiency - FCCM vs Skip-Mode

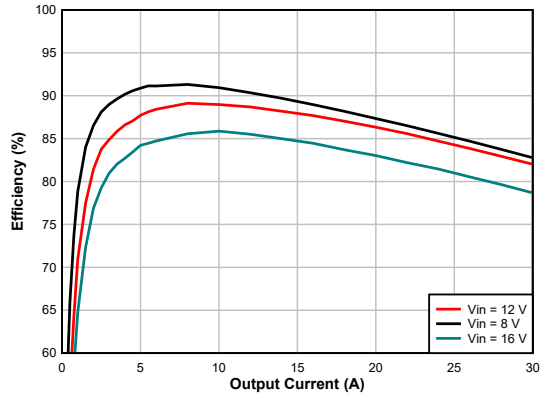

Figure 3-5. U2 Efficiency – FCCM

3.3 Output Voltage Regulation

Figure 3-6 and Figure 3-7 show the load and line regulation for U1. Figure 3-8 and Figure 3-9 show the load and line regulation for U2.

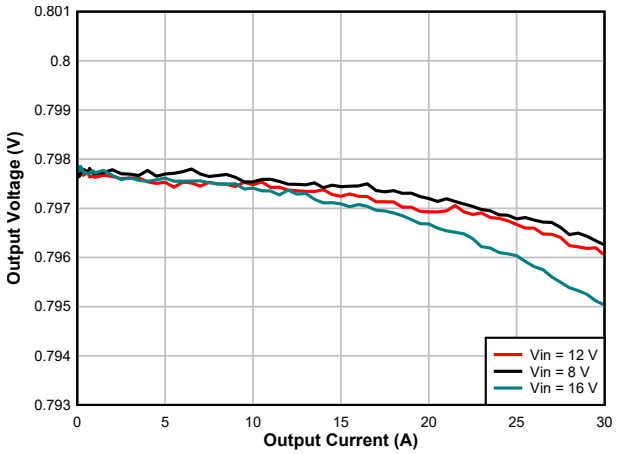

Figure 3-6. U1 Load Regulation

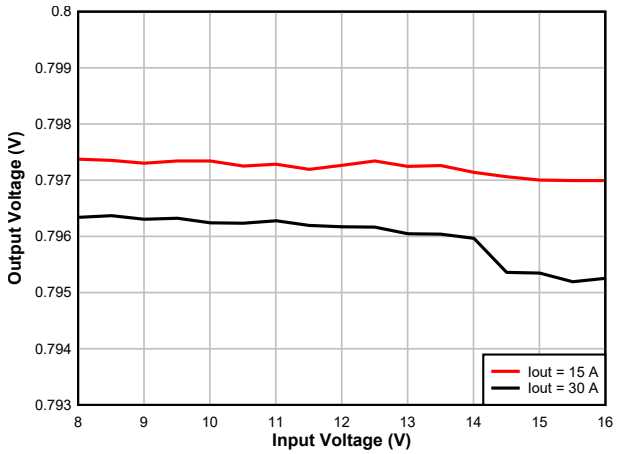

Figure 3-7. U1 Line Regulation

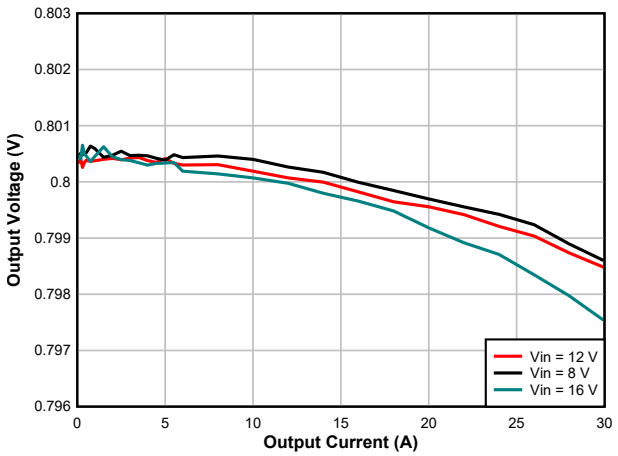

Figure 3-8. U2 Load Regulation

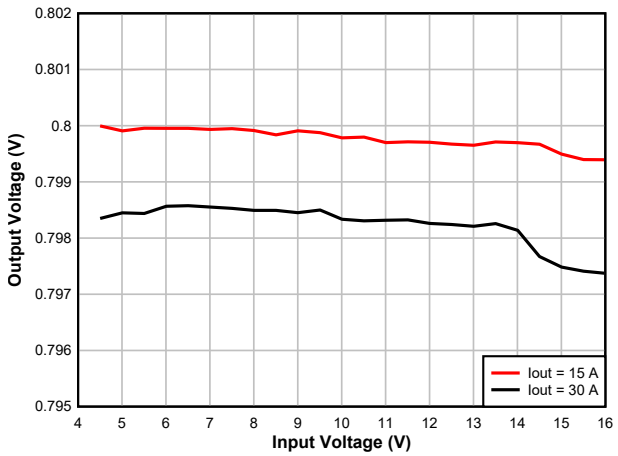

Figure 3-9. U2 Line Regulation

3.4 Load Transient and Loop Response

Figure 3-10 and Figure 3-11 show the response to load transients for both designs. The current step is from 5 A to 20 A and the current step slew rate is 1 A/µs. An electronic load is used to provide a DC 5-A load and the load transient circuit on the EVM is used to provide a 15-A step. The VOUT voltage is measured using TP11 for U1 and TP29 for U2.

Figure 3-12 and Figure 3-13 show the loop characteristics for both designs. Gain and phase plots are shown for V_{IN} voltage of 12 V and a 15-A load.

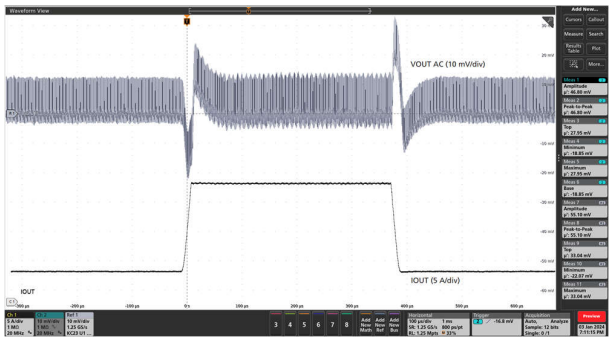

Figure 3-10. U1 Transient Response

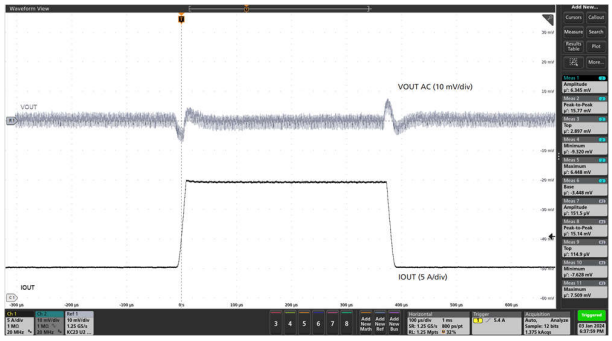

Figure 3-11. U2 Transient Response

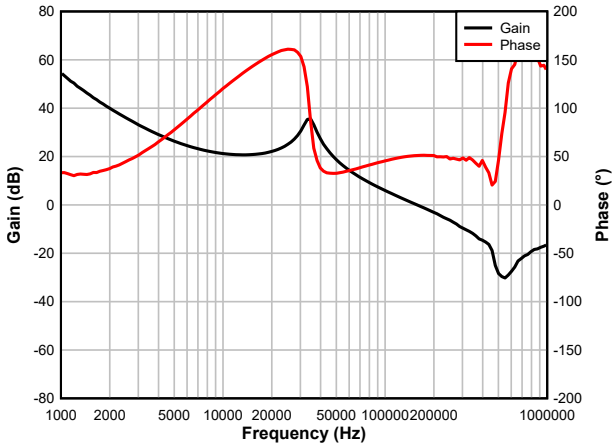

Figure 3-12. U1 Bode Plot – 15-A Load

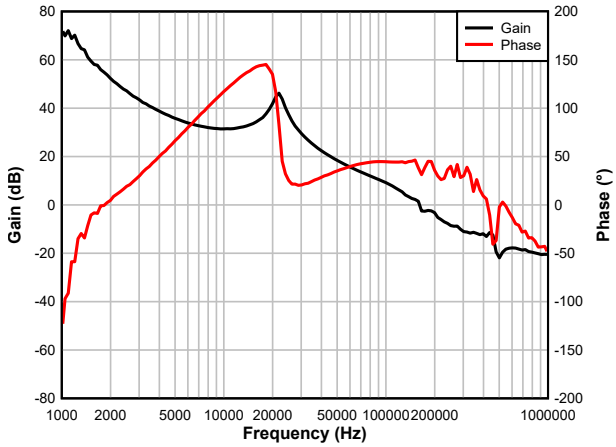

Figure 3-13. U2 Bode Plot – 15-A Load

3.5 Output Voltage Ripple

Figure 3-14 through Figure 3-17 show the TPS54KC23EVM output voltage ripple. The load currents are 10-mA and 30 A. V_{IN} = 12 V. The VOUT voltage is measured using TP11 for U1 and TP29 for U2.

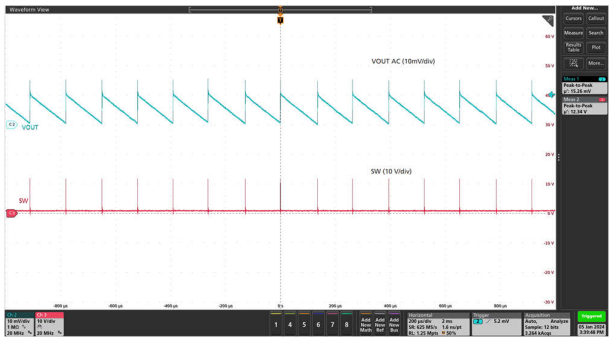

Figure 3-14. U1 Output Ripple – 10-mA Load, Skip-Mode

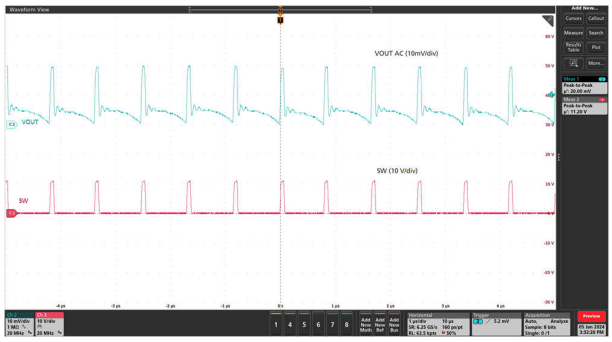

Figure 3-15. U1 Output Ripple – 30-A Load

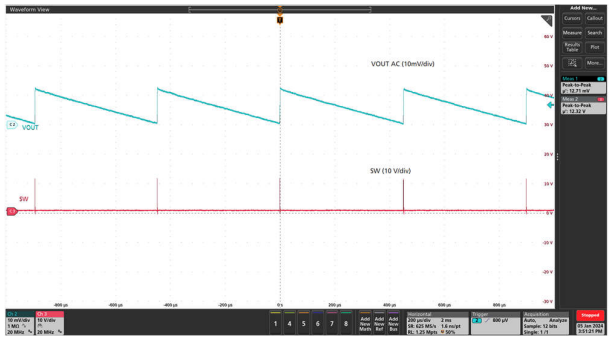

Figure 3-16. U2 Output Ripple – 10-mA Load, Skip-Mode

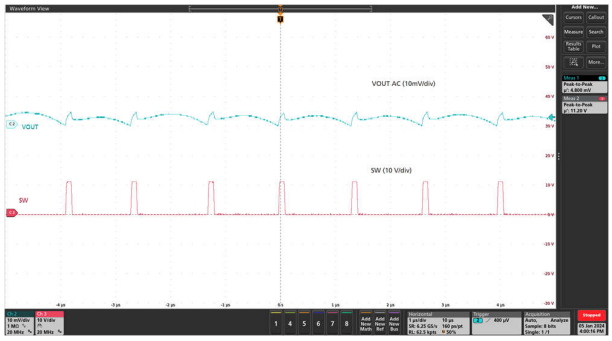

Figure 3-17. U2 Output Ripple – 30-A Load

3.6 Start-up and Shutdown with EN

Figure 3-18 and Figure 3-19 show the start-up and shutdown waveforms for U2 with EN. In Figure 3-18, the input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value. In Figure 3-19, the external function generator pulls EN to ground and the TPS54KC23 shuts down.

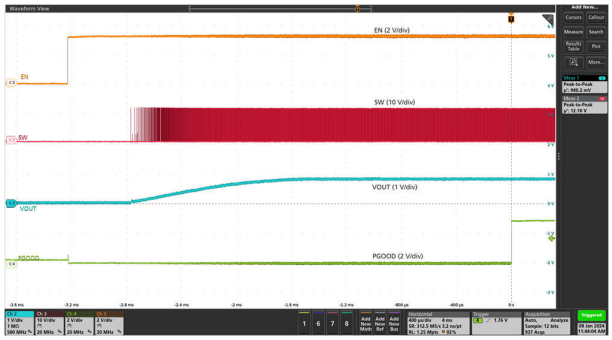

Figure 3-18. U2 Start-up with EN – 30-A Load

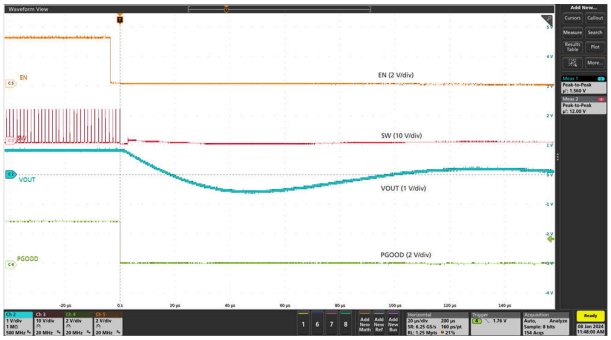

Figure 3-19. U2 Shutdown with EN – 30-A Load

3.7 Thermal Performance

Figure 3-20 through Figure 3-21 show the temperature rise of the TPS54KC23 ICs at full 30-A load. Figure 3-20 and Figure 3-21 have only one TPS54KC23 on and loaded. A minimum of 10 minutes for soak time was used before taking each measurement.

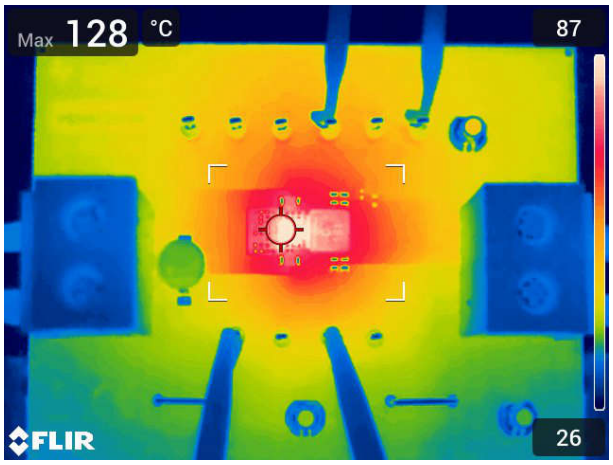

Figure 3-20. U1 Thermal Performance – 30-A Load and U2 off

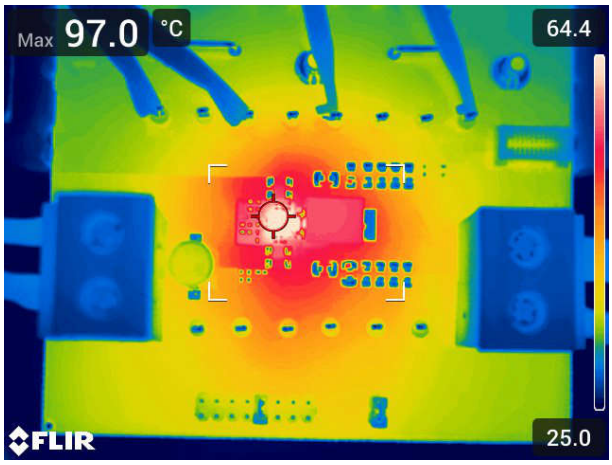

Figure 3-21. U2 Thermal Performance – 30-A Load and U1 off

4 Board Layout

This section provides a description of the TPS54KC23EVM board layout and layer illustrations.

4.1 Layout

The board layout for the TPS54KC23EVM is shown in Figure 4-1 through Figure 4-8. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. The small size U1 circuit takes up an area of only approximately 250 mm^2 as shown on the silkscreen.

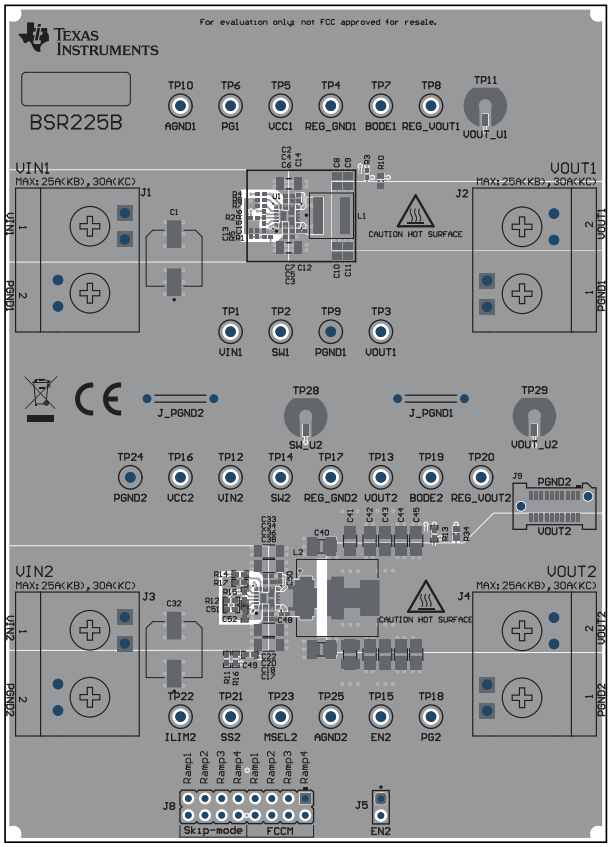

Figure 4-1. Top-Side Composite View

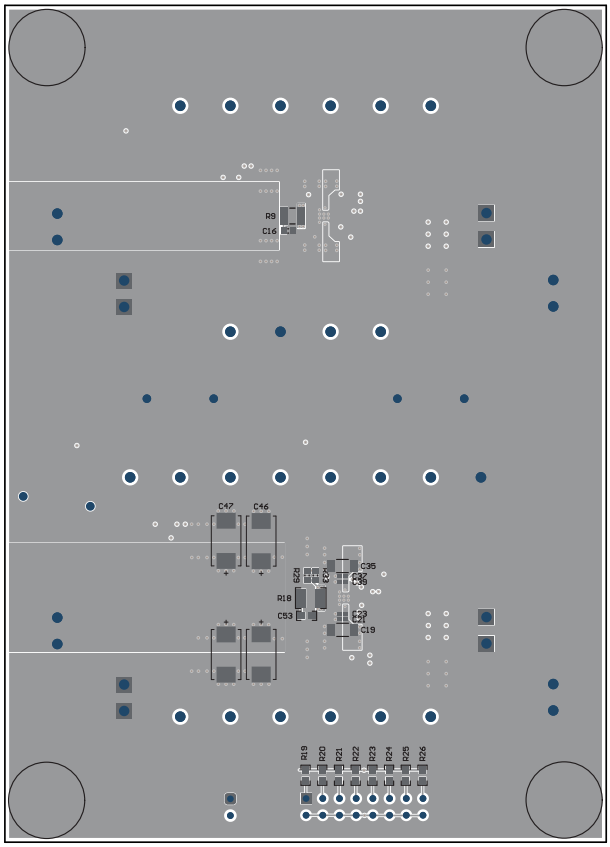

Figure 4-2. Bottom-Side Composite View (Viewed From Bottom)

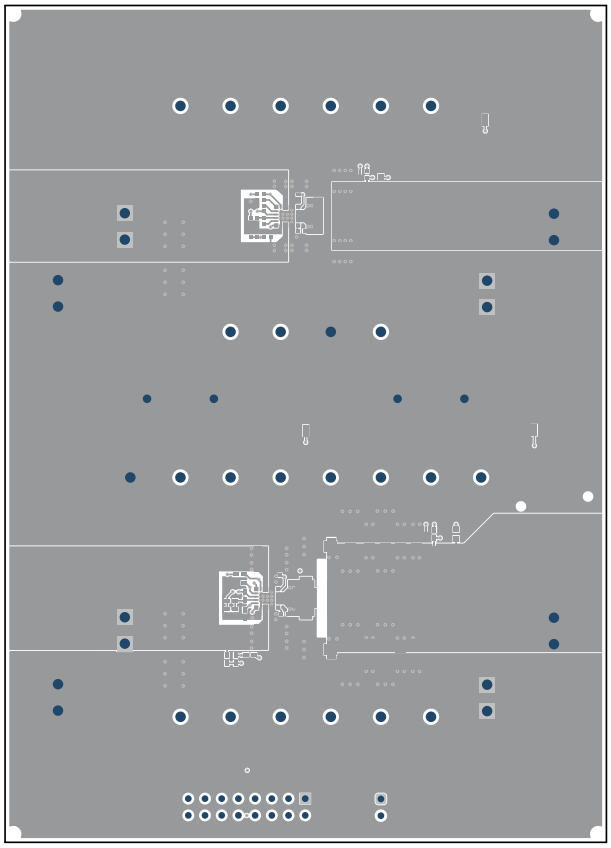

Figure 4-3. Top Layer Layout

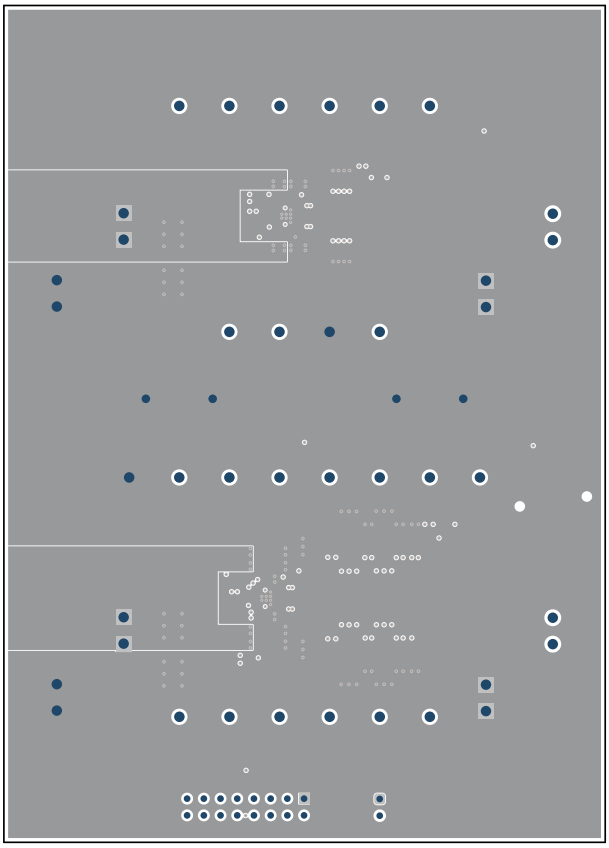

Figure 4-4. Mid Layer 1 Layout

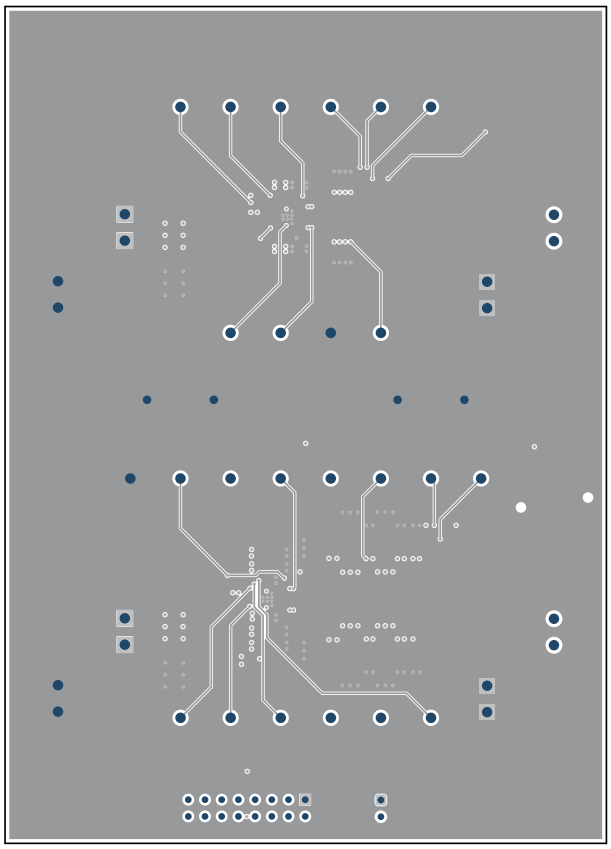

Figure 4-5. Mid Layer 2 Layout

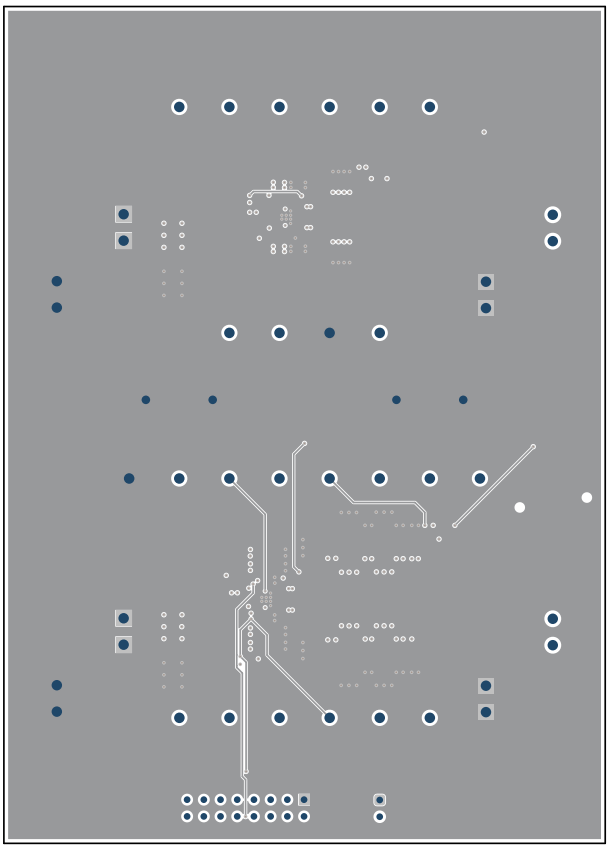

Figure 4-6. Mid Layer 3 Layout

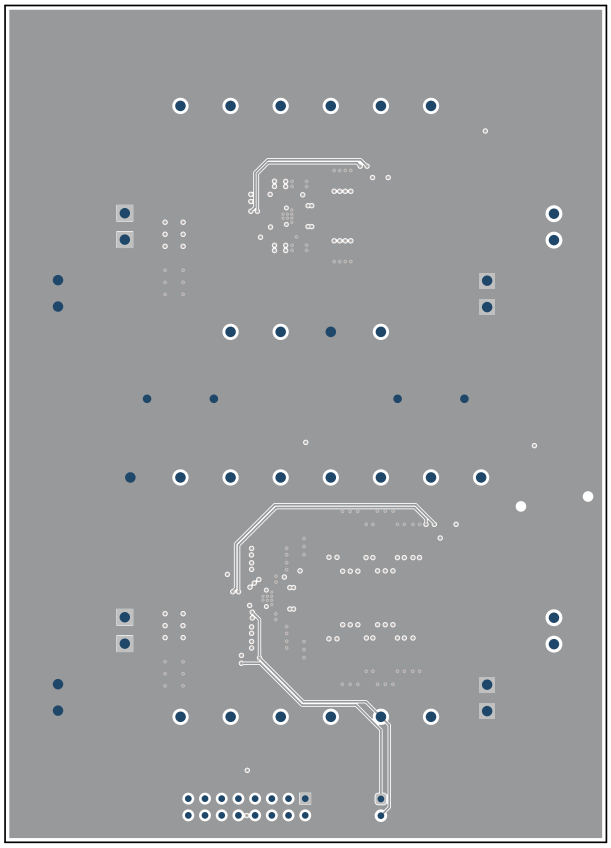

Figure 4-7. Mid Layer 4 Layout

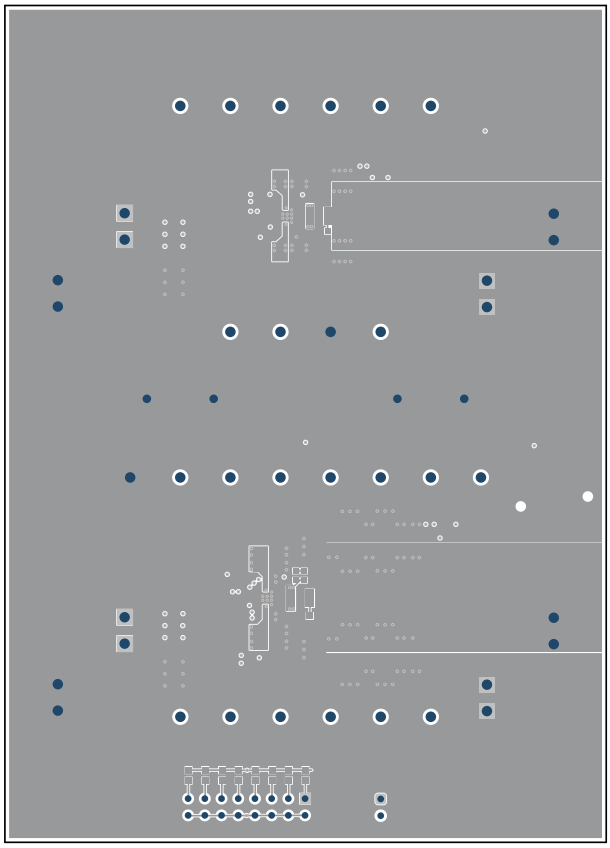

Figure 4-8. Bottom Layer Layout

5 Schematic and Bill of Materials

This section presents the TPS54KC23EVM schematic and bill of materials.

5.1 Schematic

Figure 5-1 is the schematic for U1. Figure 5-2 is the schematic for U2.

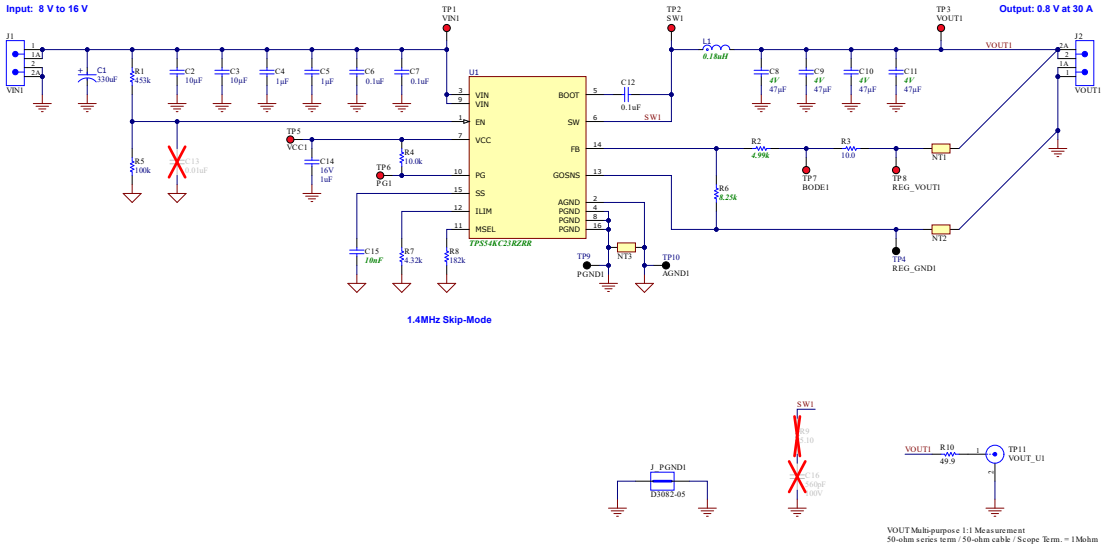

Figure 5-1. U1 Schematic

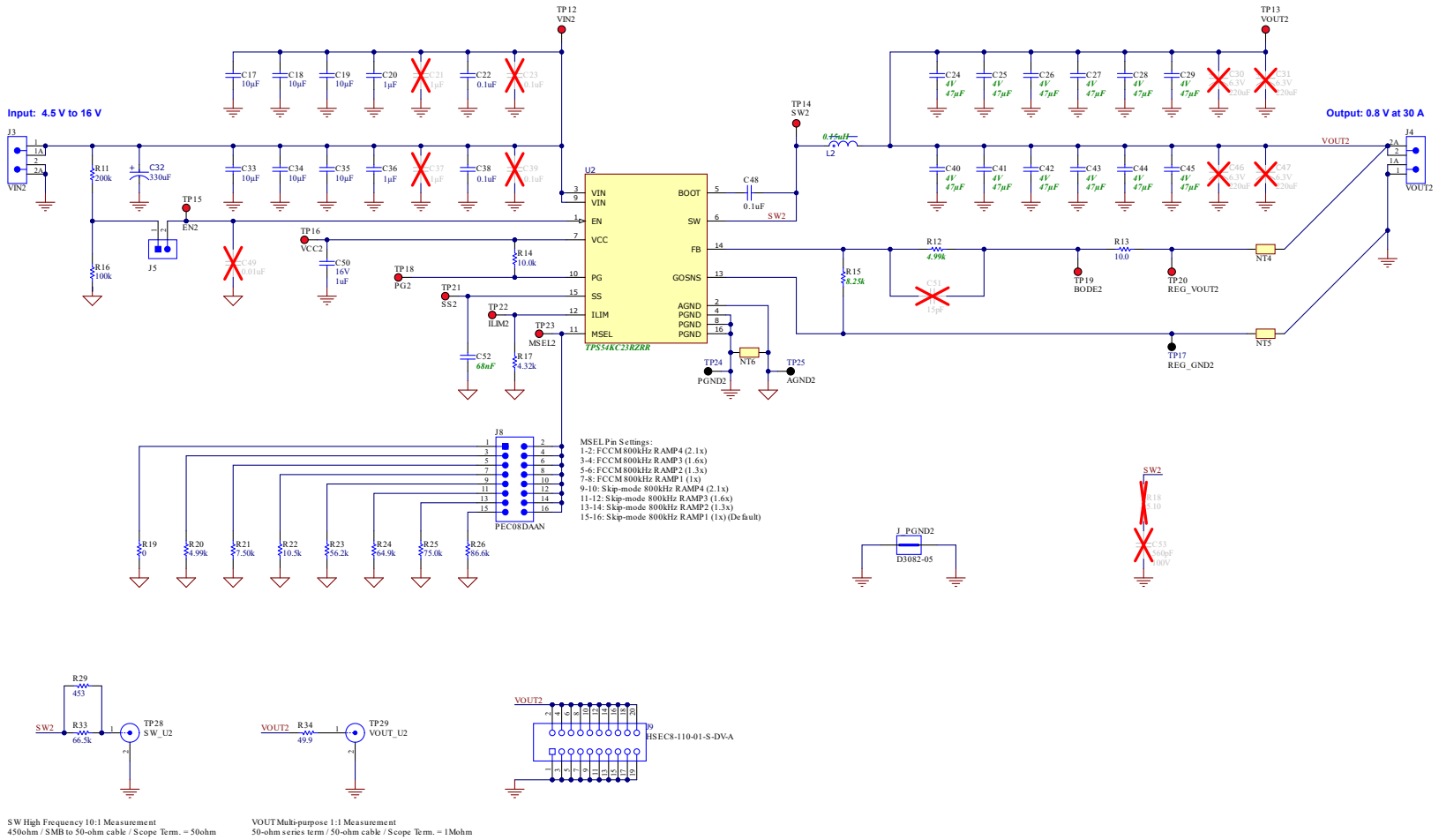

Figure 5-2. U2 Schematic

5.2 Bill of Materials

Table 5-1 details the bill of materials for the TPS54KC23EVM.

Table 5-1. TPS54KC23EVM Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		BSR225	Any
C1, C32	2	330µF	Cap Aluminum Polymer 330uF 25V 20% Solder Cylindrical 19m Ohm 2325mA 2000 hr 125°C T/R	SMT_CAP_8MM3_8MM3	A768KS337M1ELAE019	KEMET
C2, C3, C17, C18, C19, C33, C34, C35	8	10uF	CAP, CERM, 10 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	CGA5L1X7R1E106K160AE	TDK
C4, C5, C20, C36	4	1uF	CAP, CERM, 1 µF, 25 V,+/- 20%, X5R, 0402	402	GRM155R61E105MA12D	MuRata
C6, C7, C12, C22, C38, C48	6	0.1uF	CAP, CERM, 0.1 uF, 35 V, +/- 10%, X5R, 0402	402	GMK105BJ104KV-F	Taiyo Yuden
C8, C9, C10, C11, C24, C25, C26, C27, C28, C29, C40, C41, C42, C43, C44, C45	16	47uF	CAP, CERM, 47 µF, 4 V,+/- 20%, X6S, 0805	805	GRM21BC80G476ME15L	MuRata
C14, C50	2	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X6S, 0402	402	C1005X6S1C105K050BC	TDK
C15	1	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	402	GCM155R71E103KA37D	MuRata
C52	1	0.068uF	CAP, CERM, 0.068 uF, 10 V, +/- 10%, X7R, 0402	402	GRM155R71A683KA01D	MuRata
FID1, FID2, FID3, FID4	4		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4	4		Terminal Block, 60A, 10.16mm Pitch, 2-Pos, TH	21.8x30x19 mm	399100102	Molex
J5	1		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J8	1		Header, 2.54 mm, 8x2, Tin, Vertical, TH	Header, 2.54 mm, 8x2, TH	PEC08DAAN	Sullins Connector Solutions
J9	1		Card Edge Socket, 0.8mm, 10x2, SMT	Card Edge Socket, 0.8mm, 10x2, SMT	HSEC8-110-01-S-DV-A	Samtec
J_PGND1, J_PGND2	2		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
L1	1	0.18uH	180 nH Shielded Molded Inductor 25.3 A 1.2mOhm Max Nonstandard	SMT_IND_6MM51_6MM71	XGL6030-181MEC	Coilcraft
L2	1	0.15uH	150 nH Shielded Drum Core, Wirewound Inductor 65 A 0.15mOhm Nonstandard	SMT2_10MM2_8MM1	7443082015A	Wurth Electronics
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1	1	453k	RES, 453 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW0402453KFKED	Vishay-Dale
R2, R12	2	4.99k	RES, 4.99 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04024K99FKED	Vishay-Dale
R3, R13	2	10	RES, 10.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW040210R0FKED	Vishay-Dale
R4, R14	2	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	402	ERJ-2RKF1002X	Panasonic
R5, R16	2	100k	RES, 100 k, 1%, 0.1 W, 0402	402	ERJ-2RKF1003X	Panasonic
R6, R15	2	8.25k	RES, 8.25 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04028K25FKED	Vishay-Dale
R7, R17	2	4.32k	RES, 4.32 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04024K32FKED	Vishay-Dale
R8	1	182k	RES, 182 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW0402182KFKED	Vishay-Dale
R10, R34	2	49.9	RES, 49.9, 1%, 0.1 W, 0603	603	RC0603FR-0749R9L	Yageo
R11	1	200k	RES, 200 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW0402200KFKED	Vishay-Dale
R19	1	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale
R20	1	4.99k	RES, 4.99 k, 0.1%, 0.1 W, 0603	603	RT0603BRD074K99L	Yageo America
R21	1	7.50k	RES, 7.50 k, 1%, 0.1 W, 0603	603	ERJ-3EKF7501V	Panasonic
R22	1	10.5k	RES, 10.5 k, 0.1%, 0.1 W, 0603	603	RG1608P-1052-B-T5	Susumu Co Ltd
R23	1	56.2k	RES, 56.2 k, 1%, 0.1 W, 0603	603	RC0603FR-0756K2L	Yageo

Table 5-1. TPS54KC23EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R24	1	64.9k	RES, 64.9 k, 1%, 0.1 W, 0603	603	RC0603FR-0764K9L	Yageo
R25	1	75.0k	RES, 75.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0775KL	Yageo
R26	1	86.6k	RES, 86.6 k, 1%, 0.1 W, 0603	603	RC0603FR-0786K6L	Yageo
R29	1	453	RES, 453, 1%, 0.1 W, 0603	603	RC0603FR-07453RL	Yageo
R33	1	66.5k	RES, 66.5 k, 1%, 0.1 W, 0603	603	RC0603FR-0766K5L	Yageo
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP5, TP6, TP7, TP8, TP12, TP13, TP14, TP15, TP16, TP18, TP19, TP20, TP21, TP22, TP23	18		Test Point, Multipurpose, Red, TH	Red Multipurpose Test point	5010	Keystone
TP4, TP9, TP10, TP17, TP24, TP25	6		Test Point, Multipurpose, Black, TH	Black Multipurpose Test point	5011	Keystone Electronics
TP11, TP28, TP29	3		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
U1, U2	2		4-V to 16-V Input, 25-A, Remote Sense, D-CAP4 Synchronous Buck Converter	WQFN-FCRLF16	TPS54KC23RZRR	Texas Instruments
C13	0	0.01uF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X5R, 0402	402	GRM155R61C103KA01D	MuRata
C16, C53	0	560pF	CAP, CERM, 560 pF, 100 V, +/- 10%, X7R, 0603	603	GRM188R72A561KA01D	MuRata
C21, C37	0	1uF	CAP, CERM, 1 µF, 25 V,+/- 20%, X5R, 0402	402	GRM155R61E105MA12D	MuRata
C23, C39	0	0.1uF	CAP, CERM, 0.1 uF, 35 V, +/- 10%, X5R, 0402	402	GMK105BJ104KV-F	Taiyo Yuden
C30, C31, C46, C47	0	220µF	Molded Tantalum Polymer Capacitor 220uF 20% 6.3V life 1000Hours SMD 2917	2917	6TCF220M5L	Panasonic
C49	0	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	402	CGA2B3X7R1H103K050BB	TDK
C51	0	15pF	CAP, CERM, 15 pF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	402	CGA2B2C0G1H150J050BA	TDK
R9, R18	0	5.1	RES, 5.10, 1%, 0.5 W, 1210	1210	RC1210FR-075R1L	Yageo

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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