Downslope compensation for buck converters when the duty cycle exceeds 50%

By John Bottrill
Senior Applications Engineer

Current-mode control (CMC) in a pulse-width-modulated (PWM) buck converter with a duty cycle greater than 50% has the potential of going into sub-harmonic oscillations. Lloyd H Dixon, Jr., discusses this in detail in Reference 1. According to Dixon, the solution is to add to the current-sensing signal a ramp that is equal to the downslope of the output inductor current. This additional voltage needs to be added into the required calculation in order to select the current-sensing resistor.

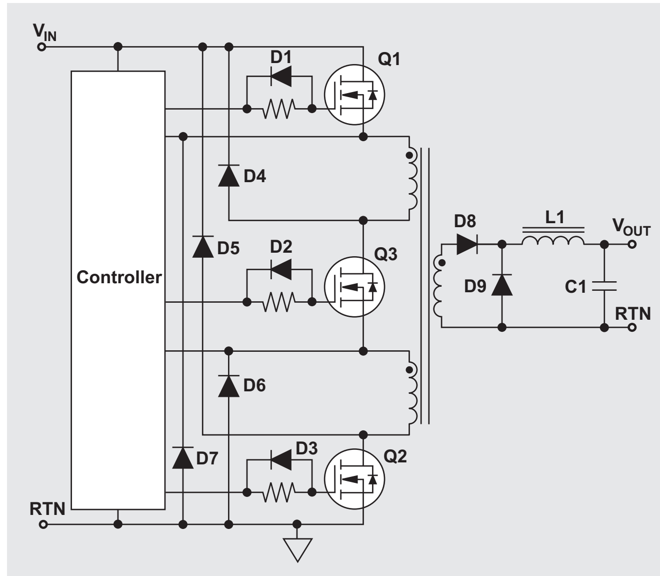
A push-pull converter, a phase-shifted full-bridge converter, or any forward converter with duty cycles greater than 50% at the output inductor are topologies that require this compensation. However, for demonstration purposes, the topology selected for this discussion is one that is relatively unknown: a three-switch forward converter. See a basic schematic of the power section in Figure 1. This topology, though patented by Texas Instruments (TI), is licensed to the public when a TI control IC is used in the circuit.

This topology has several advantages, particularly when the input-voltage range is that which is normally considered the telephone-battery range of 36 to 72 V. The topology limits the maximum duty cycle to 67%, which limits the design to a maximum duty cycle at a minimum input voltage of 67%. At the same time, the voltage on the main switches when they turn off is limited to the input voltage of the power rail. This means that low-voltage FETs can be used with their corresponding lower $R_{DS(on)}$ resistance. This topology also provides a means of recovering the magnetizing energy in the power transformer and in the primary-side leakage inductance, thereby removing the need for wasteful snubbers.

The converter design, in most other respects, is typical of any buck topology, with the exception that the duty cycle must be limited to 67% to avoid transformer saturation. This limit can be accomplished by selecting a control IC where the maximum duty cycle can be programmed, such as the UCC2807-1 (see Reference 2). Because this controller has the required duty-cycle-limiting feature, it is perfect for this application. Therefore, it was used in this study along with its characteristics for the analysis.

The following analysis assumes a theoretical switching supply with a 3.3-V output at 100 W. The supply has a maximum peak-to-peak ripple current through the output inductor equal to 10% of the maximum output DC load current of 30 A, and the input voltage is expected to be between 36 and 78 V. It is also assumed that synchronous rectifiers with a forward voltage drop, V_{fd}, of 0.5 V will be used for the output. The first step is to determine the turns ratio of the transformer. At the minimum input voltage, the duty cycle will be at the maximum limit (67%). The voltage needed at the output of the transformer can be determined by the equation

Figure 1. Three-switch forward topology



$$\frac{V_{OUT}+V_{fd}}{D_{max}}=\frac{3.3\text{ V}+0.5\text{ V}}{0.67}=5.672\text{ V}. \qquad (1)$$

If 36 V across the transformer primary windings is assumed, the turns ratio (N_p) will be 6.147, so a primary with six turns will be used. The primary is divided into two sections of three turns each (see Figure 1). As is standard practice, the secondary is sandwiched between the primary sections, and Q3 is placed between the two primary sections. With the input at 78 V, the transformer output voltage is 12.3 V, which will yield a minimum duty cycle, D_{min}, of about 31%. Therefore, the maximum OFF time equals

$$\frac{1-D_{min}}{f_{sw}},$$

where f_{sw} is the planned switching frequency of 200 kHz. The minimum output inductance (L1 in Figure 1) to achieve the desired peak-to-peak ripple current of 10% is thus defined as

$$L_{OUT}=\frac{(V_{OUT}+V_{fd})\times(1-D_{min})/f_{sw}}{I_{OUT}\times 0.1}. \qquad (2)$$

The output inductor in Equation 2 was determined to be 4.33 µH. For design purposes, 4.5 µH will be used. From this value, the current downslope, I_{ds}, of the output inductor can be calculated:

$$I_{ds} = \frac{V_{OUT} + V_{fd}}{L_{OUT}} \quad (3)$$

The inductor's downslope current (I_{ds}) is determined to be 0.844 A/µs.

It can also be determined that the peak current through the output inductor at maximum input voltage is

$$I_{OUT} + 0.5 \times (I_{OUT} \times 0.1),$$

because the maximum peak-to-peak ripple current was defined as being 10% of the output current, and that current is balanced about the nominal DC output. The peak current that results is 31.884 A.

For the minimum input voltage, it is possible to determine the differential voltage across L_{OUT}. From that, the rate of change in the output inductor can be determined to be 0.489 A/µs. Knowing the duty cycle and frequency permits calculation of the time that the current is increasing in the output inductor, making it possible to determine the ripple current under these conditions. Finally, the peak current under the minimum input voltage is found to be 31.122 A. The waveforms are shown in Figure 2. These values are almost equal, but if the downslope is added, they change—and in a surprising way. The downslope current that must be added to the peak current for the maximum input voltage is

$$\frac{I_{ds} \times D_{min}}{f_{sw}} = 1.306 \text{ A},$$

and the downslope current that needs to be added to the peak current for the minimum input voltage is

$$\frac{I_{ds} \times D_{max}}{f_{sw}} = 2.829 \text{ A}.$$

See Figure 3, where the effective downslope current is added to the currents shown in Figure 2. The result is that

Figure 2. Output inductor ripple at maximum load for $V_{IN(min)}$ and $V_{IN(max)}$

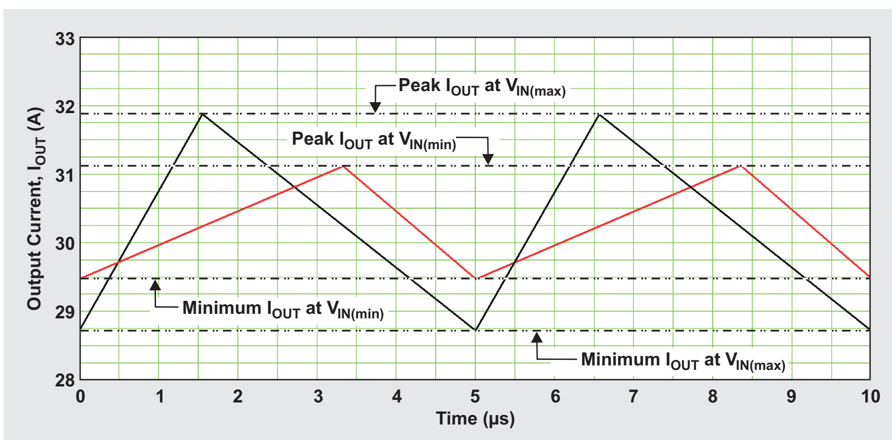


Figure 3. Secondary currents plus effective downslope current

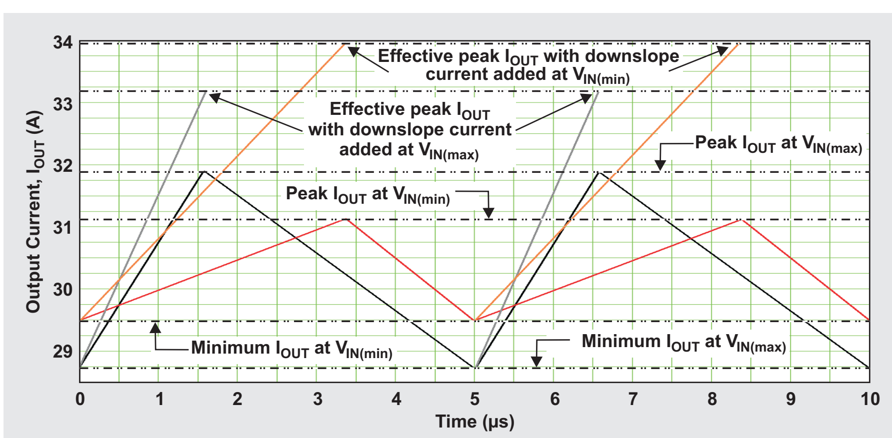
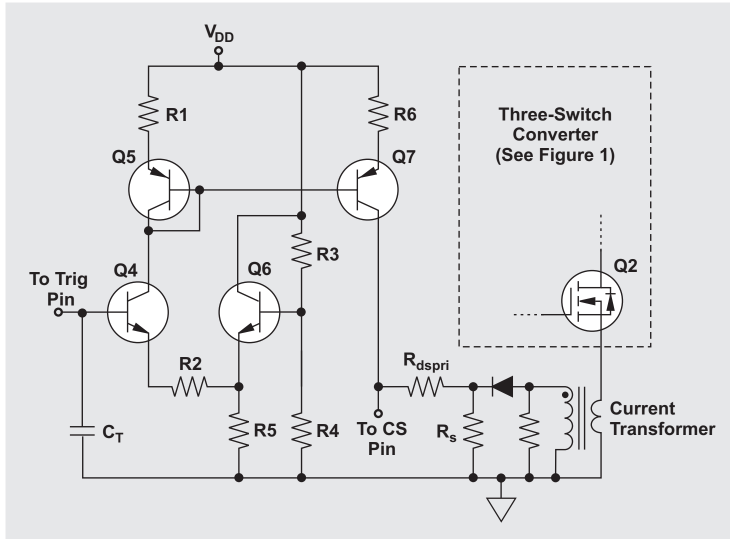


Figure 4. Circuit used to generate the desired current through R_{dspri}



the effective peak current for the minimum input voltage is higher than the effective peak current for the maximum input voltage, even though the real peaks were the reverse. The effective maximum current, including downslope at the minimum input voltage, has a peak of 33.9 A, which is the value that must be used to set the current-sensing resistor, Rs. This current, including the downslope current translated to the primary, is 5.658 A.

The IC chosen as the controller has a typical current-trip level of 1.0 V, but the tolerance is between 0.9 and 1.1 V. To make certain that all units can provide the required power, the lower limit is used, and the value of R_s is set so that the voltage across it at 5.658 A will be 95% of the 0.9-V minimum. This gives a 5% safety margin for transients and sets R_s at 0.15 Ω. Of course, there will be about 5 W of power loss, which most likely would be replaced by a current transformer. With a 100:1 transformer, R_s would increase to 15 Ω. The remaining discussion assumes that such a transformer is used.

In reality, the downslope current (I_{ds}) does not go through either the current transformer or the power transformer, but the effect needs to be accounted for and added to the voltage on resistor R_s. To do this, a resistor R_{dspri} is added between resistor R_s and the IC's current-sensing pin. At the IC's current-sensing pin, a current ramp is injected into the circuit. This current ramp is such that the ramp voltage developed across resistor R_{dspri} between the IC's current-sensing pin and resistor R_s is equivalent to the voltage that would be developed across resistor R_s by the I_{ds} translated to the primary. It is assumed that an equivalent downslope current is flowing through resistor R_s, taking into account both the power-transformer and the current-transformer winding ratios. For this case, resistor R_{dspri} is set at 1 kΩ for ease of calculation and because it is much larger than resistor R_s.

The next step is to determine the dv/dt required across R_{dspri}:

$$V_{dspri} = \frac{I_{ds} \times R_s}{N_p \times 100} = 21 \text{ V/ms} \quad (4)$$

From this result, the current ramp needed through the 1-kΩ resistor can be determined:

$$I_{dspri} = \frac{V_{dspri}}{R_{dspri}} = 21.1 \text{ µA/µs} \quad (5)$$

This current times the maximum ON time gives a peak current of 70.7 µA.

With a programmable, maximum-duty-cycle PWM controller like the UCC2807, it is relatively simple to set the maximum duty cycle to 67% by setting the two timing resistors to the same value, as shown in the datasheet. Also, the specification for the part states that the valley and peak voltages on the timing capacitor equal ⅓ V_{CC} and ⅔ V_{CC}, respectively. This gives a voltage-ramp amplitude of ⅓ V_{CC}. With this information, a circuit can now be designed to generate a ramp current that can be injected into the current-sensing circuit to provide the current downslope to the current signal.

A circuit to generate the desired current is shown in Figure 4. This circuit is based on the UCC2807-1 control IC, with V_{DD} set at 11 V. The valley and peak voltages of the Trig ramp are 3.667 V minimum and 7.33 V maximum, and the time from minimum to maximum is equal to the maximum ON time. In this circuit, R3 is equal to twice R4. This sets the voltage at the base of Q6 equal to ⅓ V_{CC}, which is the valley of the Trig voltage. As the voltage on the Trig pin swings from the valley to the peak (⅔ V_{CC}), the voltage across R2 goes from 0 to ⅓ V_{CC} in a linear manner. By choosing a value for R2 that gives a current of 70.7 µA with 3.667 V (51.8 kΩ) across it and then having the unity current mirror formed by Q5/R1 and Q7/R6, the designer can develop and add to the current-sensing signal the needed current with the correct shape and timing for the 1-kΩ resistor.

Conclusion

The three-switch forward converter offers unique advantages in energy recovery by returning the magnetizing energy and primary-side leakage energy to the source, preventing the need for snubbers and reducing the electromagnetic interference common with normal forward converters. It also offers the advantage over a two-switch forward topology of a duty cycle greater than 50%. This article has shown an example of the calculations necessary to determine the value of the current-sensing resistor and the impact of the downslope necessary for stability in a buck converter operating at a duty cycle greater than 50%. It has also shown a method of adding in the downslope in a converter.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

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1. Lloyd H. Dixon, Jr., "Current-mode control of switching power supplies," 1985 Texas Instruments Power Supply Design Seminar (SEM400) SLUP075
2. "Programmable maximum duty cycle PWM controller," UCC1807-x/2807-x/3807-x Datasheet SLUS163

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