

Design considerations for system-level ESD circuit protection

By Roger Liang

Systems Engineer

Introduction

As technology has evolved, mobile electronic devices have also evolved to become an integral part of people's lives and cultures. The advent of haptics for tablets and smartphones has encouraged increasing interaction with these devices. This creates the perfect environment for electrostatic discharge (ESD) hazards, or the discharge of static electricity from a body surface to a device. In the case of consumer electronics, for example, ESD can occur between a user's finger and a tablet's USB or HDMI connector and cause irreversible damage to the tablet, such as spiked standby current or permanent system failure.

This article explains the difference between system-level and device-level ESD phenomena and offers system-level design techniques that are targeted to protect against everyday ESD events.

System-level versus device-level ESD protection

ESD damage to ICs can occur at any time, from assembly to board-level soldering to end-user interactions. The incidence of ESD-related damage dates back to the dawn of semiconductors, but it didn't become a prevalent problem until the 1970s with the introduction of the microchip and thin-gate-oxide FETs for highly integrated ICs. All ICs have built-in device-level ESD structures that protect the IC against ESD events during the manufacturing phase. These events are simulated by three different device-level models: the human-body model (HBM), the machine model (MM), and the charged-device model (CDM). The HBM is intended to emulate ESD events caused by human handling, the MM to emulate ESD events caused by automated handling, and the CDM to emulate ESD events caused by product charging/discharging. These models are used for testing in the manufacturing environment, where assembly, final testing, and board-level soldering are performed in controlled ESD environments that limit the level of ESD stress to which the device is exposed. In the manufacturing environment, ICs are usually specified to survive ESD

strikes only to a 2-kV HBM, while lower-geometry devices have recently been specified to as low as 500 V.

While device-level models are usually sufficient for the controlled ESD environment of the factory floor, they are completely inadequate for system-level testing. The levels of ESD strikes from both voltages and currents can be much greater in the end-user environment. For this reason, the industry uses a different method for system-level ESD testing, defined by the IEC 61000-4-2 standard. Device-level HBM, MM, and CDM tests are intended to ensure only that ICs survive the manufacturing process; system-level tests specified by IEC 61000-4-2 are intended to simulate end-user ESD events in the real world.

There are two types of system-level tests specified by the IEC: contact discharge and air-gap discharge. In the contact-discharge method, the test-simulator electrode is held in contact with the device under test (DUT). In air-gap discharge, the charged electrode of the simulator approaches the DUT, and a spark to the DUT actuates the discharge.

The range of test levels specified in the IEC 61000-4-2 standard for each method is given in Table 1. It is important to note that the severity of each test level is not equivalent between the two methods. Stress levels are usually incrementally tested above level 4 (the highest official level for each method) until the point of failure.

Table 1. Test levels for contact-discharge and air-gap-discharge methods

CONTACT-DISCHARGE LEVEL	TEST VOLTAGE (± kV)	AIR-GAP-DISCHARGE LEVEL	TEST VOLTAGE (± kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 2. Comparison of device-level models and IEC system-level model

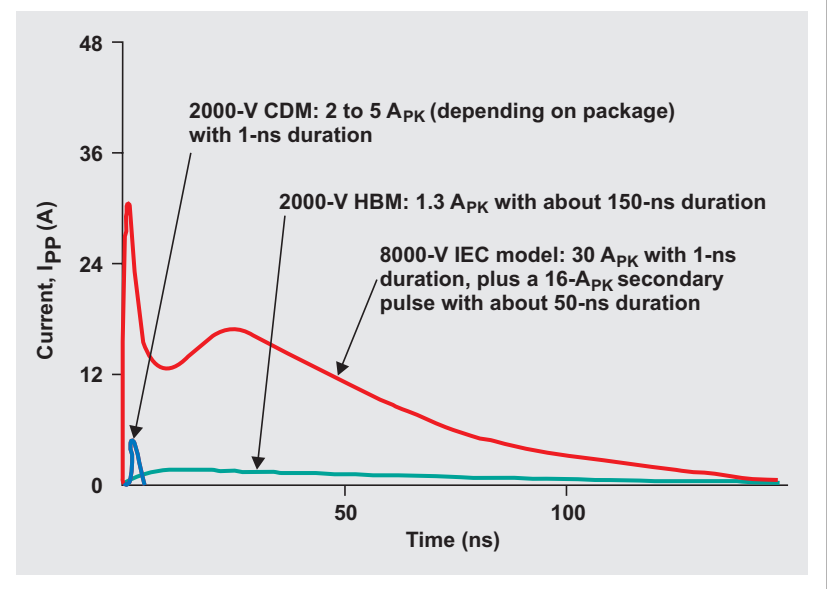
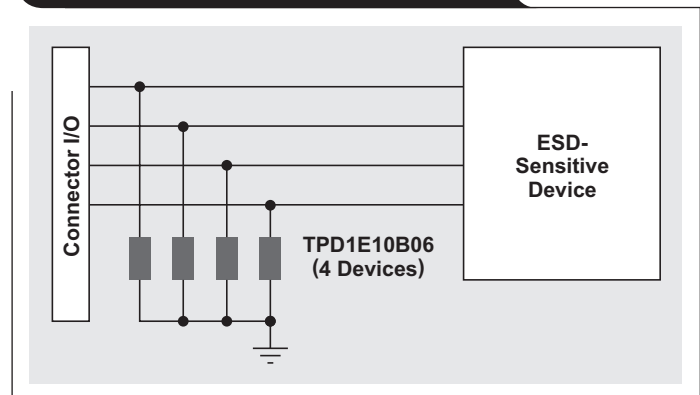
	HUMAN-BODY MODEL (HBM)	MACHINE MODEL (MM)	CHARGED-DEVICE MODEL (CDM)	IEC 61000-4-2 MODEL
Definition	Human body discharging accumulated static	Robotic arm discharging accumulated static	Charged device being grounded	Real-world ESD events
Test Levels (V)	500 to 2000	100 to 200	250 to 2000	2000 to 15000
Pulse Width (ns)	~150	~80	~1	~150
Peak Current at Applied 2 kV (A_{PK})	1.33	—	~5	7.5
Rise Time	25 ns	—	< 400 ps	< 1 ns
Number of Voltage Strikes	2	2	2	20

Device-level models and system-level models have some distinct differences, as highlighted in Table 2. The last three parameters in Table 2—current, rise time, and number of voltage strikes—are of particular concern:

- The difference in current is critical to whether the ESD-sensitive device survives an ESD strike. Because high current levels can cause junction damage and gate-oxide damage, it is possible that a chip protected by an 8-kV HBM (with a peak current of 5.33 A) can be destroyed by a strike to a 2-kV IEC model (with a peak current of 7.5 A). Thus, it is extremely important that system designers do not confuse HBM ratings with ratings for the IEC model.
- Another difference lies within the rise time of the voltage strikes. The rise time specified for an HBM is 25 ns. The pulse of the IEC model has a rise time of less than 1 ns and dissipates most of its energy in the first 30 ns. If an HBM-rated device takes 25 ns to respond, the device can be destroyed before its protection circuits are even activated.
- The number of strikes used during testing is different between the models. The HBM requires only a single positive and single negative strike to be tested, whereas the IEC model requires ten positive strikes and ten negative strikes. It is possible for a device to survive the first strike but fail on subsequent strikes due to damage sustained during the initial strike. Figure 1 shows example ESD waveforms for a CDM, an HBM, and the IEC model. It is apparent that the IEC model's pulse carries much more energy than the pulse of each device-level model.

How a TVS protects a system against ESD events

Instead of integrated structures for ESD protection, the model specified by the IEC 61000-4-2 standard usually uses discrete stand-alone transient-voltage-suppressant diodes, or transient-voltage suppressors (TVSs). Compared

Figure 1. ESD waveforms for device-level and IEC models**Figure 2. System-level TVS placement**

to ESD-protection structures integrated into a power-management or microcontroller unit, stand-alone TVSs are low in cost and can be placed close to the system's I/O connector, as shown in Figure 2.

There are two types of TVSs: bidirectional and unidirectional (see Figure 3). The Texas Instruments TPD1E10B06 is an example of a bidirectional TVS that can be placed on a general-purpose data line for system-level ESD protection. Both bidirectional and unidirectional TVSs are designed to be an open circuit during normal operating conditions, and a short to ground during an ESD event. In the case of a bidirectional TVS, a voltage signal on the I/O line can swing above and below ground as long as neither D1 nor D2 enters its breakdown region. When an ESD strike (positive or negative) hits the I/O line, one diode becomes forward-biased and the other breaks down, creating a path in which ESD energy is immediately dumped to ground. In the case of a unidirectional TVS, a voltage signal can swing above ground as long as neither D2 nor Z1 enters its breakdown region. When a positive ESD strike hits the I/O line, D1 becomes forward-biased and Z1 enters its breakdown region before D2 does; a path to ground is created through D1 and Z1 in which ESD energy is dissipated. When a negative ESD strike hits, D2 becomes forward-biased and ESD energy is dissipated through D2 to ground. Unidirectional diodes are implemented for high-speed applications because D1 and D2 can be sized smaller with less parasitic capacitance; D1 and D2 in turn “hide” the bigger Zener diode, Z1, which is sized bigger in order to handle more current in its breakdown region.

Key device parameters for system-level ESD protection

Figure 4 shows the characteristics of a TVS diode's current versus voltage. Even though a TVS is a simple structure, several important parameters should be considered in the design of system-level ESD protection. These include breakdown voltage, V_{BR} ; dynamic resistance, R_{DYN} ; clamping voltage, V_{CL} ; and capacitance.

Breakdown voltage

The first step in selecting the appropriate TVS is looking at the breakdown voltage (V_{BR}). For example, if the maximum working voltage, V_{RWM} , on the protected I/O line is 5 V, the TVS should not enter into its breakdown region before reaching this maximum. More often than not, a TVS datasheet includes V_{RWM} at a specific leakage current, which makes choosing the right TVS easy. If that is not the case, a TVS can be selected whose $V_{BR(min)}$ is a couple of volts higher than the V_{RWM} of the protected I/O line.

Figure 3. Bidirectional and unidirectional TVSs

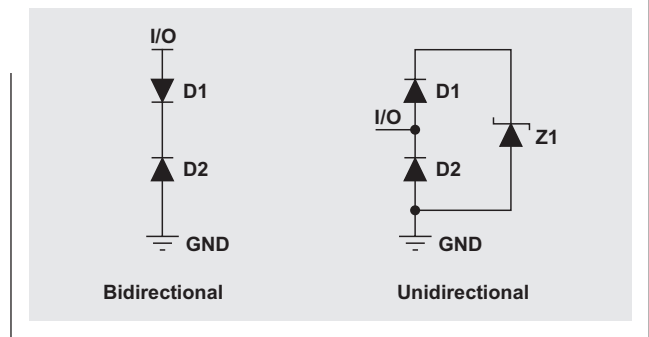


Figure 4. TVS diode's current versus voltage

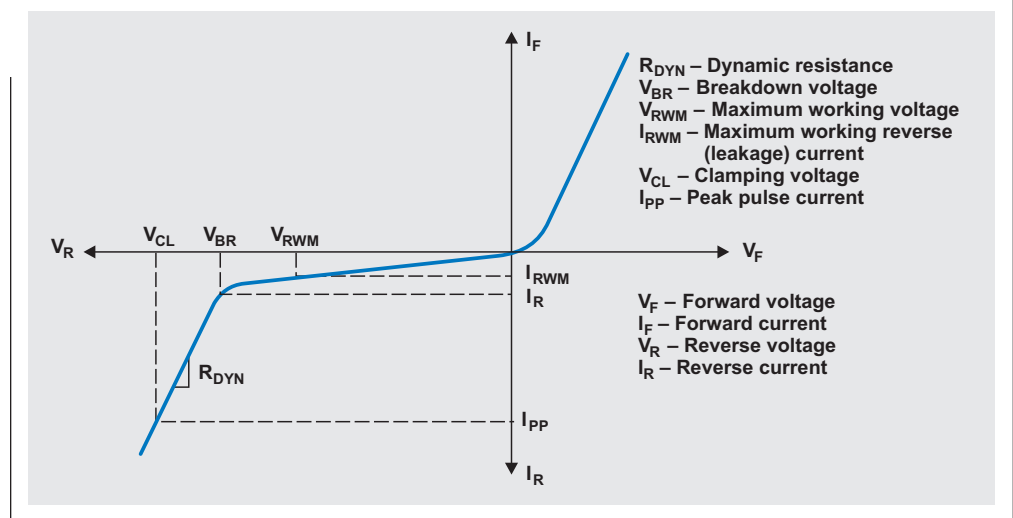
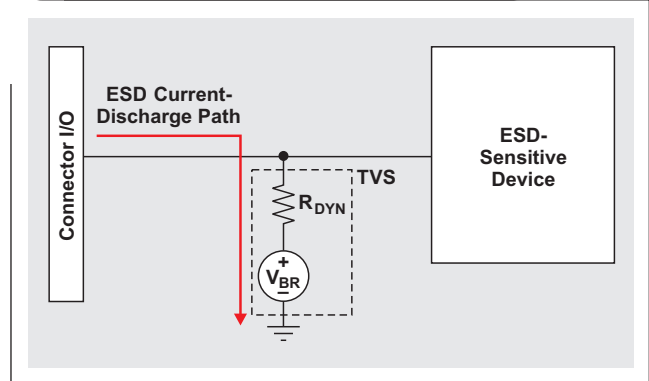


Figure 5. ESD current-discharge path



Dynamic resistance

An ESD is an ultrafast event in the range of nanoseconds. During such a short amount of time, the TVS conduction path to ground is not established instantaneously and there is some resistance in this path. This resistance, known as dynamic resistance (R_{DYN}), is shown in Figure 5.

Ideally, R_{DYN} should be zero so that voltage on the I/O line can be clamped as close to the V_{BR} as possible; however, that is never the case. The industry's current standard value for R_{DYN} is 1 Ω or less. R_{DYN} can be captured by using transmission-line pulse-measurement techniques, where a charged voltage is discharged through the TVS and a corresponding current is measured. After many data points with different charged voltages have been taken, an IV curve like the one in Figure 6 can be drawn, and the slope is R_{DYN} . Figure 6 shows the TPD1E10B06's R_{DYN} , which has a typical value of $\sim 0.3 \Omega$.

Clamping voltage

Since an ESD is an ultrafast transient event, the voltage on the I/O line is not clamped instantaneously. As shown in Figure 7, thousands of volts are clamped to tens of volts according to the IEC 61000-4-2 standard. As indicated by Equation 1, the lower R_{DYN} is, the better the clamping performance will be:

$$V_{CL} \approx V_{BR} + I_{PP} \times R_{DYN} + I_{Parasitic} \times \frac{dI_{PP}}{dt}, \quad (1)$$

where I_{PP} is the peak pulse current during an ESD event, and $I_{Parasitic}$ is the parasitic inductance of the trace from the connector through the TVS to ground.

Imagine the area under the clamping-voltage waveform as energy. The better the clamping performance is, the less likely it is that an ESD-sensitive device under protection will be damaged during an ESD event. Due to poor clamping voltage, some TVSs survive an IEC model's 8-kV contact discharge, but the "protected" device is destroyed.

Capacitance

During normal operating conditions, the TVS acts as an open circuit and has a parasitic-capacitance shunt to ground. It is important for the designer to take this capacitance into account in the signal chain's bandwidth budget.

Conclusion

As IC process-technology nodes continue to become smaller, they become increasingly more susceptible to ESD damage, both during the manufacturing process and in the end-user environment. Device-level ESD protection is not enough to protect ICs on a system level. Stand-alone TVSs should be used in a system-level design. When selecting a TVS, the designer should pay careful attention to parameters such as V_{BR} , R_{DYN} , V_{CL} , and capacitance.

Reference

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/litnumber and replace "litnumber" with the **TI Lit. #** for the materials listed below.

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1. "System-level ESD/EMI protection guide". . . SSZB130B

Related Web sites

www.ti.com/esd

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Figure 6. IV characteristic of TPD1E10B06

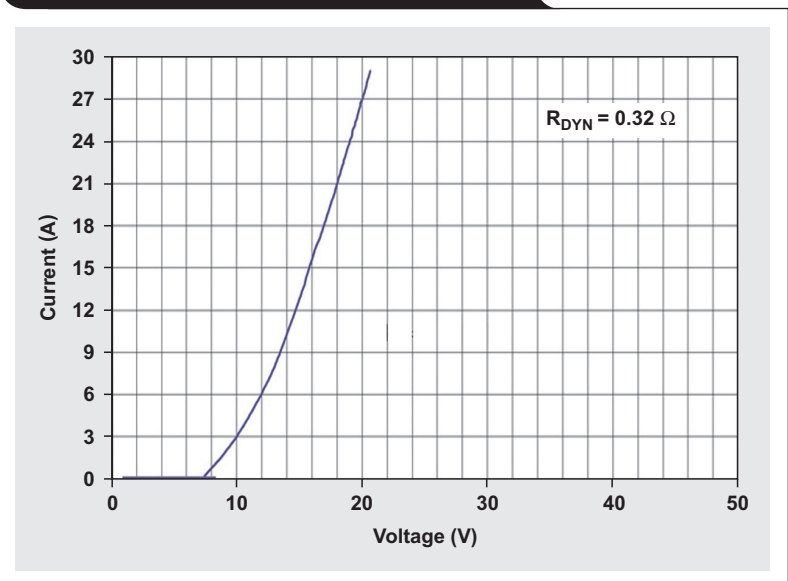
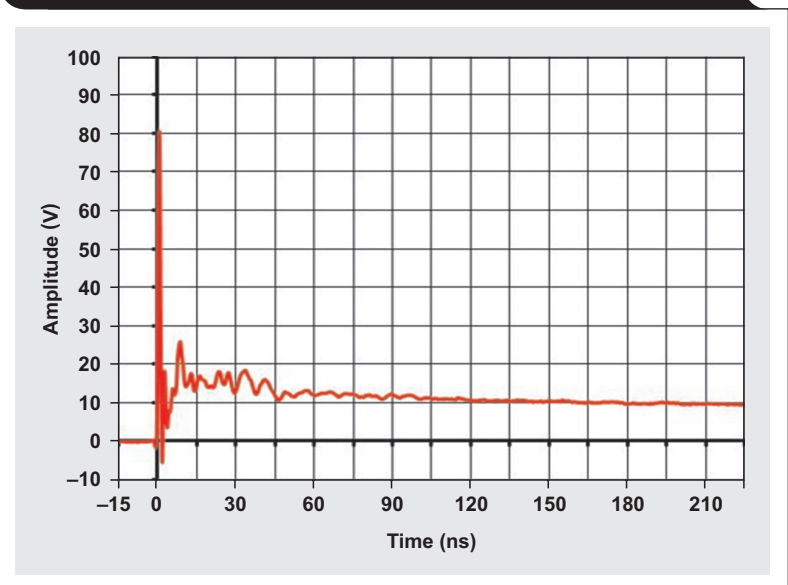


Figure 7. ESD-event clamping with 8-kV contact discharge



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