Advanced linear equalization in multi-gigabit systems

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Introduction

While today's widespread need for signal equalization in electronics may seem to be a recent phenomenon, there are examples of linear equalization in telecommunications dating back well over a century. In fact, continuous time linear equalization (CTLE) is just part of a signal conditioning ecosystem designed to aid in the transmission and reception of high-speed digital signals. This compensation or conditioning of the digital signals is usually called emphasis in the transmit domain and equalization in the receive domain.

What is linear equalization and why it is it needed?

Equalization is a process or technique used to restore balance between the various frequency components which together make up an electronic signal. In an simple analogy, audio equalizers are often used to help boost signal components which speakers have difficulty reproducing, or our old ears can no longer hear efficiently. Moving from audio speakers to signals on a PCB or in a cable, a similar issue is encountered. As high-speed signals pass through the transmission media, high-frequency signal components are quickly attenuated due to the physical properties of the conductor and the surrounding dielectric.

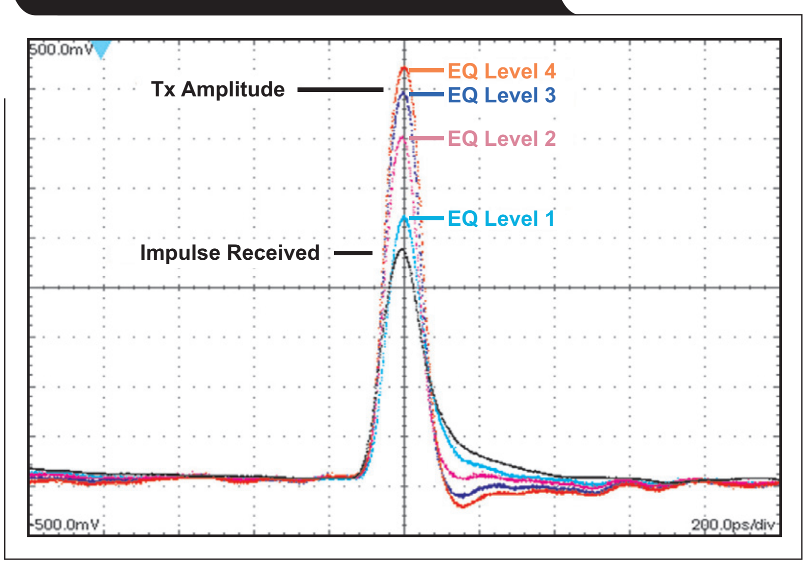
CTLE performance

Modern telecommunication standards must embrace and specify faster data rates to help satisfy the increasing appetite for instantaneous information around the globe. This almost ensures that CTLE will continue to be specified in serial data standards under development now and in the future. At an overview level, the linear gain or high-pass boost by CTLE circuitry helps to expand the incoming signal envelope. CTLE, in combination with digital equalization strategies like decision feedback equalization (DFE), can enable robust signal reception across media with levels of signal attenuation not possible with DFE alone. A more in-dept view is provided by time-domain waveforms and frequency-domain plots to highlight common CTLE characteristics and how they impact an actual eye diagram.

In Figure 1, the received time-domain impulse is initially launched into a 10-inch length of FR4 transmission media with an output differential voltage of 800 mV_{pp}. After traversing the FR4 transmission media, the received impulse amplitude is reduced by half and the trailing-edge energy has spread well past the original bit width or unit interval (UI) boundary. In this example, a DS125BR820 equalizer from Texas Instruments was attached at the far end of the 10-inch trace to demonstrate the CTLE function and its effectiveness for reducing jitter due to channel losses. As the CTLE level is gradually increased to match the channel loss, it is able to restore the impulse amplitude and adjacent bit interference. Looking at the amplitude and timing features on the impulse response provides insight into system response to a pseudo-random binary sequence (PRBS) pattern. This method simply time shifts and sums each of the PRBS transitions as an impulse. In the strict mathematical sense, the impulse in Figure 1 does not have infinite amplitude and zero width, but it is still a good intuitive way to look at CTLE performance.

Without CTLE, even a simple data pattern clearly shows the effect of reduced amplitude and pulse-spreading for the single-bit transitions within the eye diagram. The addition of CTLE reduces these effects by equalizing the amplitude of all transitions in the data pattern and minimizing the pulse spreading across bit boundaries. In

Figure 1. Impulse response after 10-inch FR4, with and without CTLE



eliminating the interaction between bits, inter-symbol interference (ISI) is minimized and the eye opening is improved. This can be seen in Figure 2 by comparing the eye diagrams.

Frequency domain

Another way to examine CTLE is in the frequency domain. The FR4 used in the time domain experiment can be measured to determine its frequency domain characteristics. The same measurement tool is also used to measure the CTLE characteristics. Typically, the optimum eye-diagram results are achieved when the attenuation of the transmission media is matched by the CTLE gains out to a frequency close to the Nyquist frequency across a wide range of frequencies. The example shown in Figure 3 shows the transmission loss and CTLE gain associated with a 12-Gbps serial data rate. For a 12-Gbps signal, a repeating pattern of 101010 binary symbols produces a 6-GHz fundamental frequency. This combination results in a total system response of the media + CTLE that is ideally zero or flat.

Taking this technique to extreme levels of attenuation and high-frequency gain uncovers a CTLE limitation. As the frequency domain plot shows, a CTLE circuit can provide considerable boost to the high-frequency signal components. Internally, the CTLE is designed to minimize any random jitter (RJ) additions to the high-speed signal. Externally, it is impossible for the CTLE gain to discriminate between signal and system noise. Therefore, all aspects of the incoming data receive a boost, and this effect is made more apparent at higher CTLE boost.

Figure 2. Eye diagrams without CTLE (top) and with CTLE (bottom)

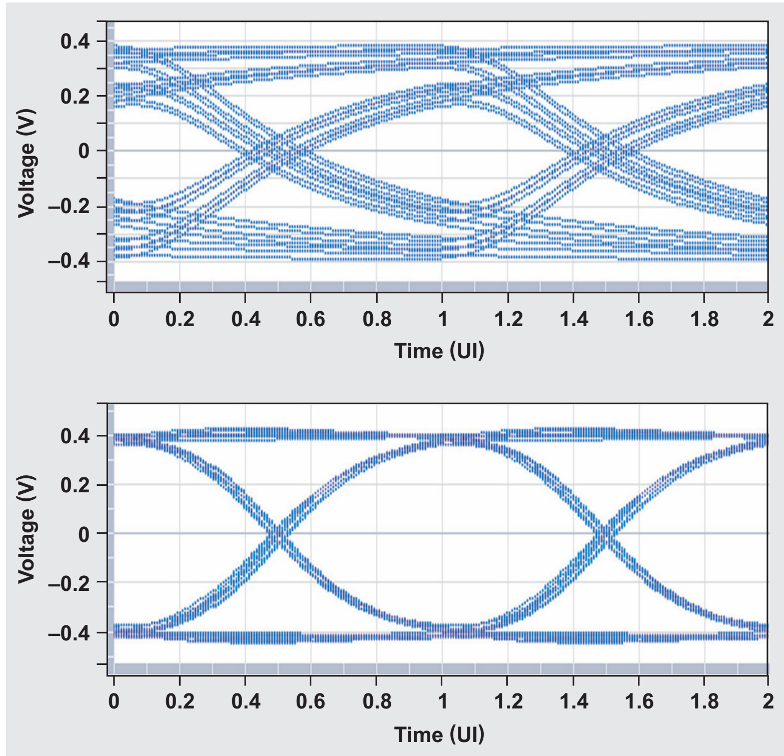


Figure 3. FR4 attenuation and idealized CTLE gain

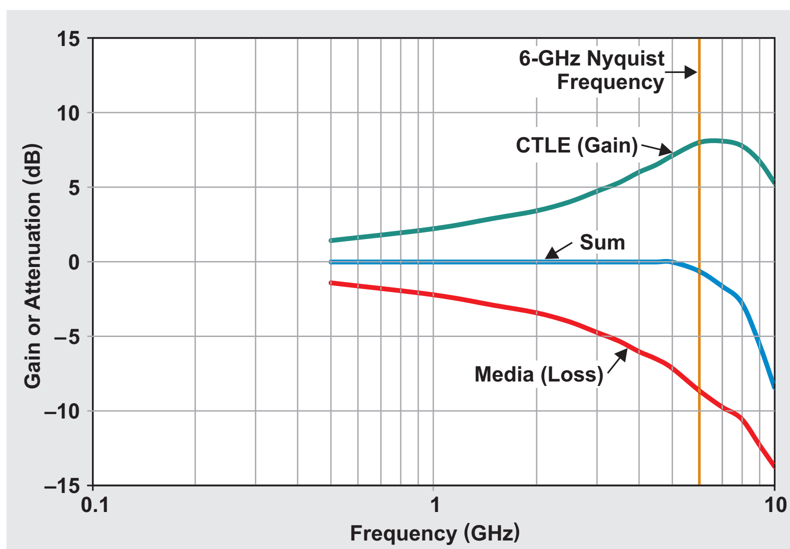
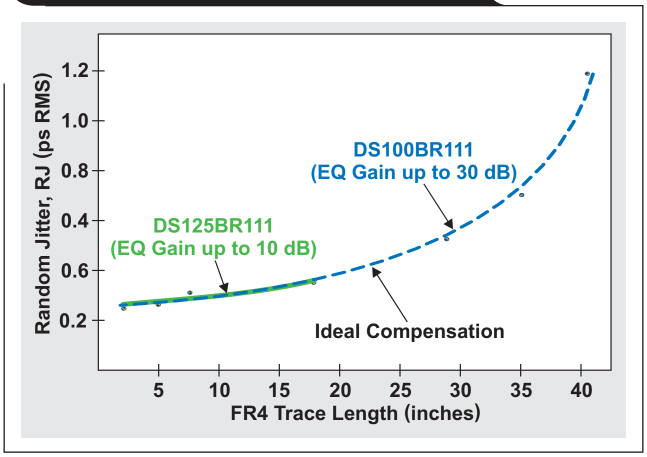


Figure 4. CTLE gain vs. additional RJ



As shown in Figure 4, when higher levels of CTLE gain are required to compensate for transmission losses, jitter-decomposition software recognizes the increased levels of RJ. High levels of RJ can result in bit errors. Fortunately, CTLE in a low-to-medium dose can be applied without significant increases in measured RJ. In fact, CTLE solutions continue to be specified and used for media compensation at data rates above 25 Gbps. Currently, 25-Gbps interfaces are limited to a very small portion of the total interface market. Most designers still have the opportunity to come up to speed in standards like PCI Express® (PCIe), 10-gigabit Ethernet (10GbE), and serial attached SCSI (SAS), which range from 8 to 12 Gbps.

Link training

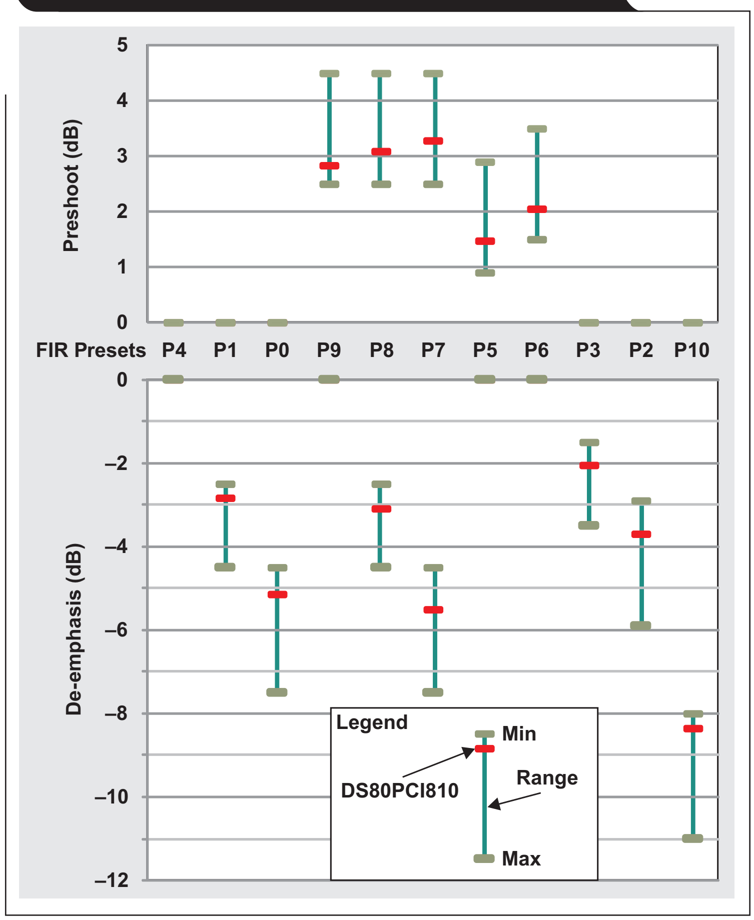
One thing all these standards have in common is the concept of link training and adaptive signal conditioning. Although the specifics and algorithms will vary, all incorporate methods that allow receivers (Rx) to feedback or recommend finite impulse response (FIR) coefficient changes to the transmit (Tx) device. Working through this process enables the Rx/Tx pair to arrive at a total channel solution for signal compensation without external intervention. A linear equalizer inserted into a lossy channel designed to use link training must maintain and preserve the linearity of the channel while providing sufficient gain to effectively turn a long channel into a shorter, less lossy channel. The DS125BR820 exhibits sufficient bandwidth and dynamic range to accommodate maximum-amplitude signals from industry-standard transmitters.

In PCIe applications, a linear equalizer can be placed adjacent to an add-in-card (AIC) connector. Standards-based software testing is used to exercise the host transmitter to sequence through the full range of Tx preset values with varied amounts of FIR energy. A comparison in both Table 1 and Figure 5 shows how an equalizer can

Table 1. Ideal and measured PCIe transmit preset values

PCIE Tx Preset	Preset Binary Value	Ideal Vb	Measured Vb	Ideal Post Cursor	Ideal Pre Cursor	Measured Post Cursor	Measured Pre Cursor
P4	0100'b	1000	1070	0	0	0	0
P1	0001'b	668	772	–3.5	0	–2.8	0
P0	0000'b	500	592	–6	0	–5.1	0
P9	1001'b	668	772	0	3.5	0	2.8
P8	1000'b	501	592	–3.5	3.5	–3.1	3.1
P7	0111'b	402	479	–6	3.5	–5.5	3.3
P5	0101'b	803	903	0	2	0	1.5
P6	0110'b	750	845	0	2.5	0	2.1
P3	0011'b	750	845	–2.5	0	–2.1	0
P2	0010'b	603	699	–4.5	0	–3.7	0
P10	1010'b	335	409	–9.5	0	–8.4	0

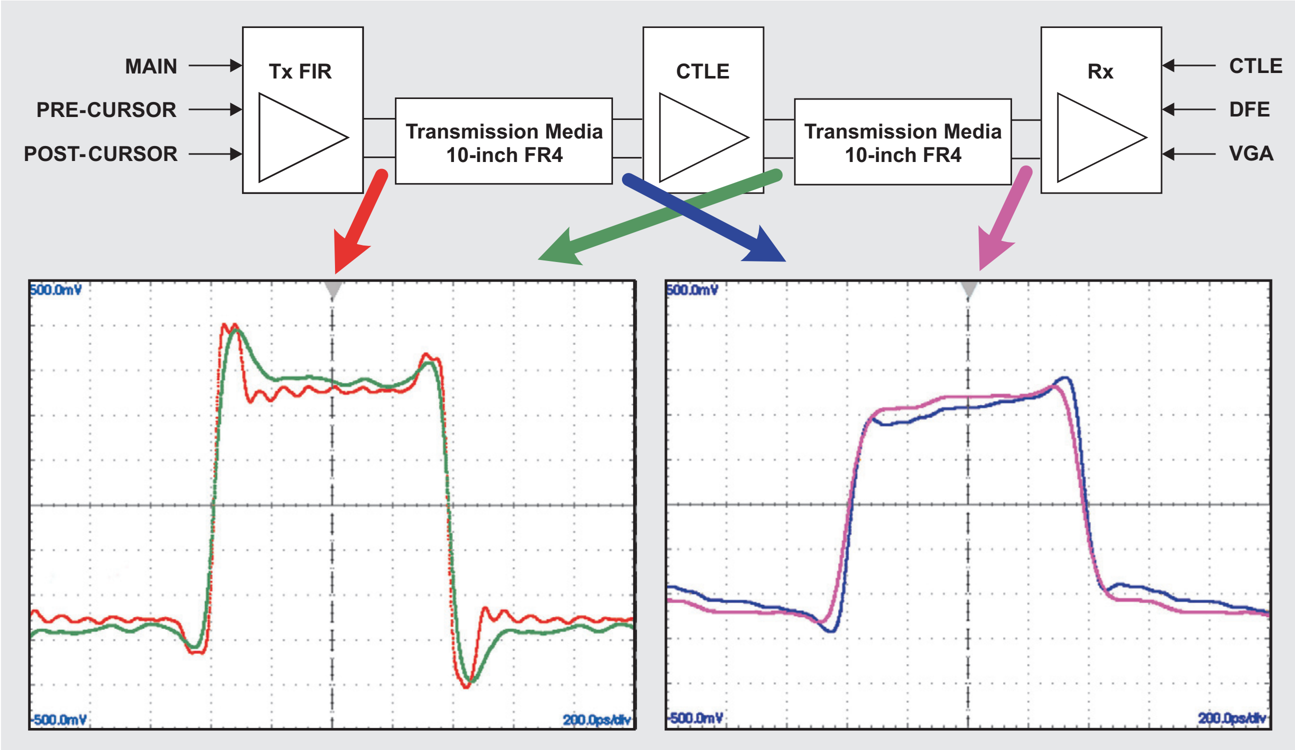
Figure 5. Graphical representation of measured PCIe Tx preset values



preserve the pre-cursor and post-cursor energy within the allowed PCIe standard margins.

The combination of linear equalization and output drive creates a high level of FIR transparency. This enables the equalizer to reproduce and successfully pass on all

Figure 6. Restored TX FIR energy using linear equalization



PCIe 3.0 Tx preset values at the AIC connector. PCIe 3.0 performance of the DS80PCI810 from Texas Instruments has been verified at a recent PCI-SIG Compliance Workshop. As of this article's publication, it is the only linear equalizer currently listed on the PCIe 3.0 Integrator's List. PCIe Tx presets are tested using a specific compliance pattern and oscilloscope software to extract and calculate the measurement values. This testing helps to ensure robust operation in PCIe-compliant channels.

While a system integrator looks at this type of specification and measured data with a very critical eye, a more intuitive feel for the CTLE performance is easier to generate with waveforms captured at the full bit rate or speed. In a modern digital system, it is important to understand the waveform characteristics at several locations within the transmission channel. The waveform sequence in Figure 6 shows a 10GbE waveform at several points (match arrow color to waveform color) along the channel.

Modern methods of adapting Tx and Rx equalization easily allow for 20- to 30-inch links at the 10-Gbps data rate. The additional linear equalizer may not always be a requirement at this distance, but it is a good length to show how a linear equalization scheme can effectively reduce the equalization requirements of other system-level components. As seen in Figure 6, a linear equalizer can restore lost amplitude to the high-frequency components embedded in the waveform transitions while simultaneously preserving the low-frequency amplitude characteristics. By placing the CTLE midway through the 20-inch channel, it allows the waveforms to be paired up to show equivalent waveforms at the CTLE input and Rx input. Inserting the CTLE has reduced the effective channel length by 10 inches or almost 9 dB.

Conclusion

Using linear equalization adds mere picoseconds of latency and minimal additive jitter to the serial link. This increases the effective solution space for transmission and reception of high-speed signals. It is clear that digital-signal processing and communication will continue to dominate the infrastructure of new communication standards. However, the use of linear equalization in the analog domain still plays an important support role in the realm of high-speed signal conditioning, thereby ensuring robust error-free operation across a broad spectrum of serial protocols, including 10GbE Ethernet, PCIe and SAS.

Related Web sites

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