Thermal design concerns for buck converters in high-power automotive applications

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Introduction

Automotive designs increasingly require higher-performance electronic components with reduced printed circuit board (PCB) cost. This trend has resulted in an uptick in signal-processing operating speeds (and density) on a single board. The increase in operating speeds has in turn raised demand for more compact power supplies to provide room for component routing. While high-performance, high-density power supplies save PCB space, they also generate heat and reduce the heat-dissipation capabilities of surrounding mounted devices, which drives the need for lower-loss power converters that enable a higher thermal margin of neighboring devices.

In recent years, improvements in semiconductor design and layout have enabled the development of more efficient converters that support higher-power applications. Greater converter efficiency also enabled faster switching frequencies, which in turn allowed design engineers to shrink the power-supply solution size and decrease cost by reducing component size and count.

Improved converter control schemes have further reduced passive component counts (**Figure 1**) without impacting noise or transient performance, and freed up room around the converter for routing devices or to allow for thermal management improvements.

USB Type-C™ is an automotive use case where 2-MHz converter operation allows for extra room in the board layers for additional charging diagnostics. Improved converter efficiency means less heat generation, making it possible to house the power solution in a plastic enclosure that has little airflow. Furthermore, an increase in the integrated circuit's (IC) maximum operating temperature to 150°C (or above) furthers converter capabilities in applications requiring 105°C or higher ambient temperature ratings.

Managing Thermals with Flip-chip Packages

No matter how efficient a buck converter is, losses will occur in the power stage. Power converter losses cause the device junction temperature to rise and prevent safe operation at higher ambient temperatures. Converter design for high ambient temperatures requires proper thermal management to ensure that the converter's recommended maximum rated junction temperature is not exceeded, and to prevent the converter from heating up neighboring devices.

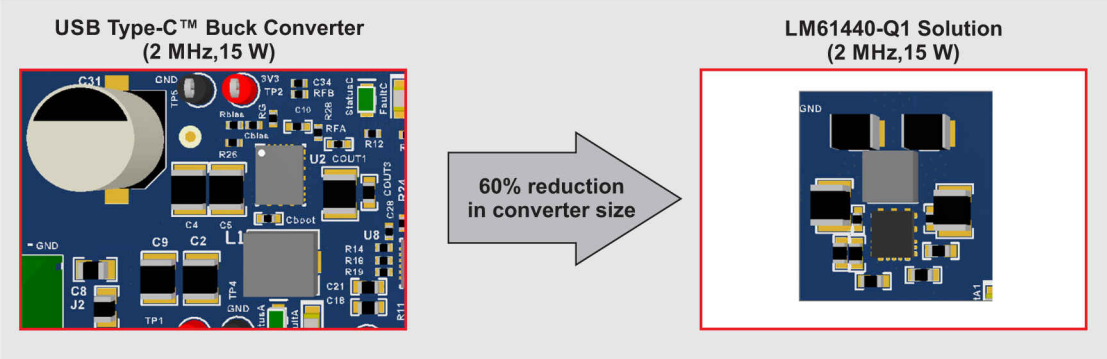

Figure 1. *Reduced Solution Area with the LM61440-Q1 Buck Converter*

Many semiconductor manufacturers are implementing converters in a flip-chip package design. A flip-chip device often has a quad flat no-lead (QFN) package, with low-inductance connections made from the semiconductor die to the leadframe. This strikes a good balance between thermal and noise performance. However, the package may lack a thermal pad on its bottom side, which reduces its thermal effectiveness. Nevertheless, with flip-chip devices, efficient heat conduction can occur through the die-to-leadframe copper connections (**Figure 2** and **Figure 3**).

To avoid excessive temperature rise, it makes sense to provide a high thermal conductivity path from the landing pad away from the device. Wide traces to the device landing pads can allow for heat dissipation in the component layer. Dense PCB layouts prevent effective heat dissipation in the component layer, especially with inefficient (hot) neighboring devices. As shown in **Figure 3**, heat sinking in the inner layers is often more effective than heat dissipation in the component layers. Connecting thermal vias to copper that is connected to the device power or return pins will achieve heat sinking. These vias will then connect to copper planes underneath the IC, increasing the effective copper area for heat sinking. It's important to place the vias in a way that minimizes thermal bottlenecks, while providing the highest via count with the lowest thermal resistivity to power pins (**Figure 2**).

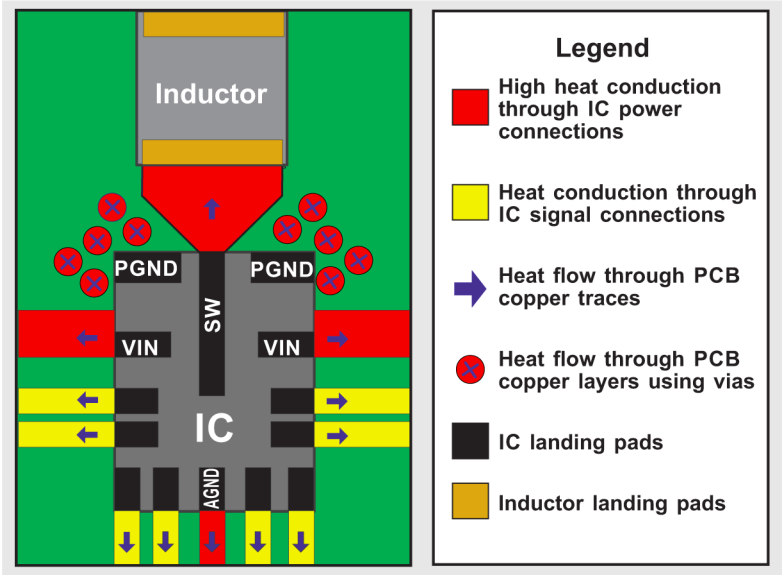

Figure 2. *Top View of Flip-chip Die-to-package Heat-conduction Path for PCB Layer Heat Sinking*

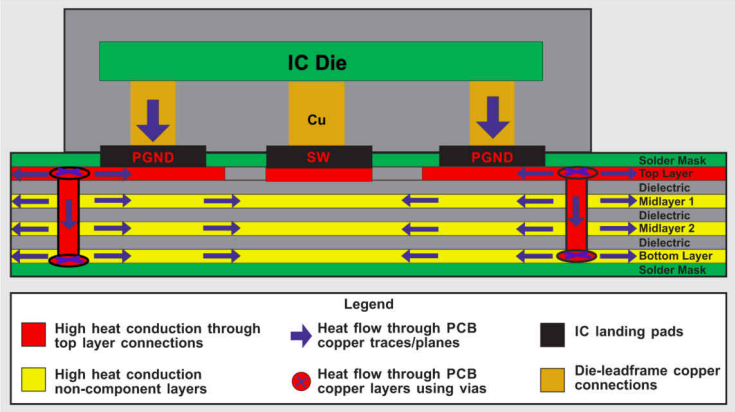

Figure 3. *Board Layer View of Flip-chip Die-to-package Heat-conduction Paths*

Board Construction Influence

Thermal vias will get heat away from devices mounted on the PCB. Filling vias with conductive material will reduce their thermal resistivity. If via filling is not possible, balancing via copper area and count will allow for effective heat flow.[1]

Making the layer directly underneath the IC as thick and as close to the component layer—by maximizing copper thickness and minimizing dielectric separation—will conduct heat and reduce electromagnetic interference (EMI) most effectively. The total board size must often be a certain height, so the board stackup may need to change.

The copper thickness will benefit the board's thermal performance (**Figure 4**), which can be quantized by the converter's effective junction-to-ambient thermal impedance, $R_{\theta JA}$.

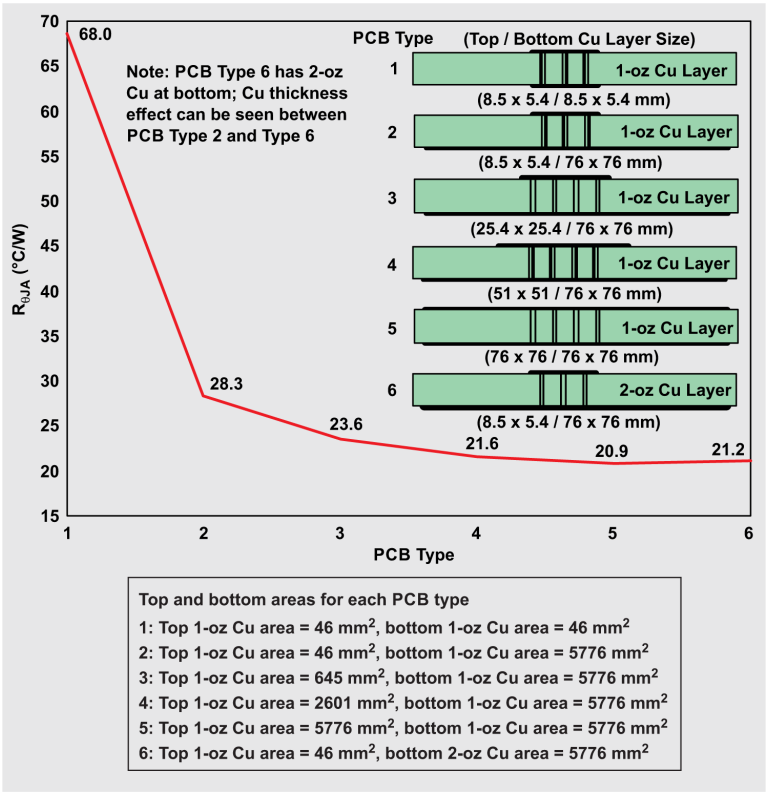

Figure 4. *Demonstrating the Thermal Impact between 1- and 2-Oz PCB Copper-layer Weights*

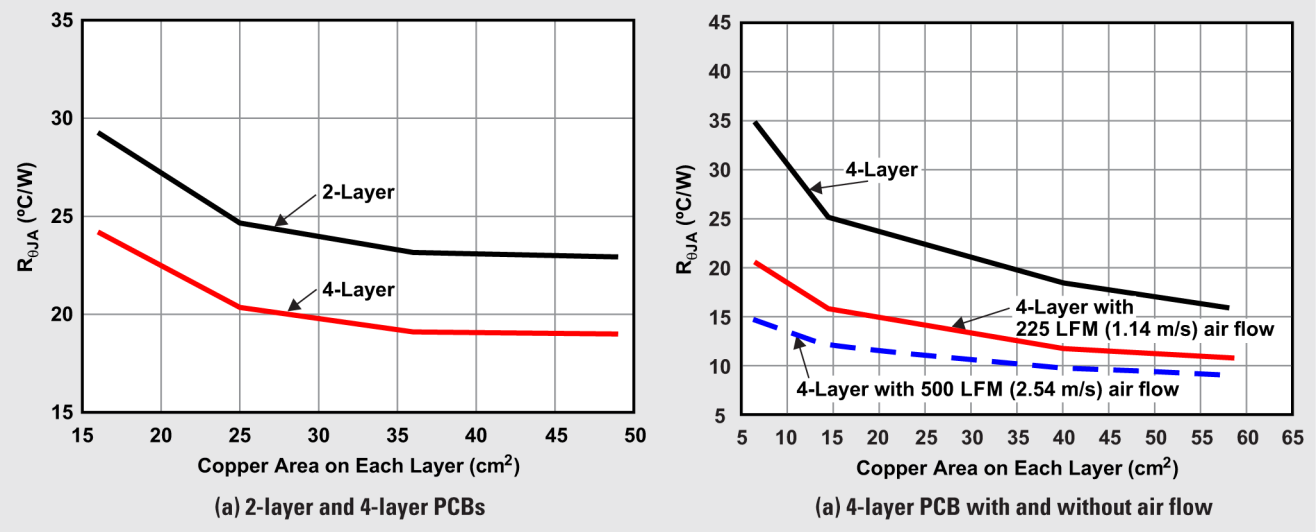

Figure 5. *Effects of Copper Area on Thermal Performance, $R_{\theta JA}$*

Copper Area and Thermals

PCB layout is the biggest influencer on power-converter thermal performance, with package thermal metrics close behind. The $R_{\theta JA}$ metric describes a board's thermal performance. It quantizes the thermal resistance between the ambient air and a semiconductor p-n junction on the converter's die. A primary influencer on $R_{\theta JA}$ is the effective copper area available for heat sinking.

Figure 5 demonstrates the impact of available copper area on $R_{\theta JA}$, with data collected by reducing the copper area of the two- and four-layer PCBs equally for each $R_{\theta JA}$ measurement. The data can determine the effect of having more copper area on thermal performance. The measured device $R_{\theta JA}$ can provide an estimate for the ambient temperature at which the device will be able to operate.

Estimating a Converter's Junction Temperature

The simulated $R_{\theta JA}$ from a Joint Electron Device Engineering Council (JEDEC) standard board is found in a converter's data sheet. JEDEC boards often have very small traces that are not ideal for thermal conductivity (**Figure 6**). Landing pad-to-trace or copper-plane connections allow for heat conduction. In practice, the connections will be made to large copper areas in the mid layers, making the simulated $R_{\theta JA}$ too conservative.

To estimate a board's $R_{\theta JA}$ experimentally, note the rise in IC case temperature (ΔT) at a given power condition. A preferable power condition would be one where low loss would occur in a buck converter's output inductor, but high-enough power loss exists to establish a gradient with a thermal camera for measurement. Even with proper mounting, a thermocouple can often give an inaccurate temperature measurement of the top case because of its heat sinking tendency. From the measured efficiency, η, (at the same ambient temperature), **Equation 1** calculates the power loss (ΔP) in the converter and board $R_{\theta JA}$ as:

$$R_{\theta JA} = \frac{\Delta T}{\Delta P} \simeq \frac{T_{Case} - T_{Amb}}{(1-\eta) \times P_{IN}} \quad (1)$$

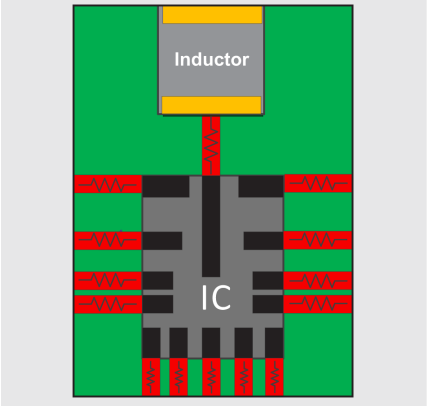

Figure 6. *A High Thermal-resistance JEDEC Board Used for Characterizing a Device's $R_{\theta JA}$*

While the efficiency calculation does include inductor losses (which do not lead to a direct rise in the IC temperature), heat sharing does occur between the inductor and IC. The converter is not the only source of heat. The $R_{\theta JA}$ approximation becomes more accurate with inductors that have lower losses or lower bias current. An exercise to further improve this estimate could entail forward-biasing either of the power stage's body diodes to heat up the IC, eliminating inductor influence. The diode's voltage drop and bias current would then be used for power loss (ΔP).

It is critical to consider the converter's FET temperature coefficient in the calculations. The FET's drain-to-source on-resistance [RDS(on)] will be worst at the design's maximum ambient temperature (TA_max). Increased FET RDS(on) causes efficiency to degrade at a high ambient temperature (η_H). **Equation 2** expresses the converter power loss ΔP_H at the design's maximum rated ambient temperature:

$$\Delta P_H = (1 - \eta_H) \times P_{IN} \quad (2)$$

Equation 3 estimates the worst-case junction temperature at the maximum ambient temperature, TA_max

$$T_J = T_{A\_max} + R_{\theta JA} \times \Delta P_H \quad (3)$$

Challenges with Measuring Converter Junction Temperature

It can be difficult to measure the converter junction temperature in an enclosed temperature chamber. Using a thermocouple can be ineffective, as it can remove heat from the package topside. This leaves a current or voltage measurement as an alternative way to determine the converter's junction temperature.

Converters have an electrostatic discharge diode on each pin to protect the device from static discharge. Additionally, some pins may have a FET between them; for example, the PGOOD pin has an open-drain FET from PGOOD and ground. Characterizing the voltage drop on the body diode of this FET allows for an approximation of the junction temperature.[2] Unfortunately, due to switched waveforms in the IC (and sometimes the IC layout), characterizing a diode in the IC is not always a clear-cut process. Additionally, the diode measurement must not influence the normal operation of the device.

Further Thermal Optimization at the IC Level

Issues may arise with the thermal performance of the power converter due to cooling limitations. These issues often occur late in the prototype stage. Fortunately, it is possible to change the switching frequency of many converters. A prototype build could allow for the larger or additional component place-holders required for a slower frequency converter.

The switching frequency can heavily impact a converter's power losses. If a design approaches the maximum recommending operating conditions, a switching frequency adjustment can provide a quick fix to resolve this issue. Reducing the switching frequency will reduce AC losses (switching losses) in the converter, as these losses are directly related to parasitic FET capacitances in the converter and the switching frequency at which they charge and discharge. Additionally, losses in the inductor will drop,[4] although the inductor core material will dictate by how much.

Figure 7 shows the inability of a faster-frequency converter to operate at the same ambient temperature and output power of a slower-frequency converter. Selecting the switching frequency should balance device performance and overall cost for the given application.[5]

One other simple design change to improve thermal performance of the design is proper inductor selection. Changing the inductor to one with lower losses will increase converter design efficiency. The specific losses, AC and DC, are contingent on inductor construction and power conditions. Inductor losses and how they vary with converter specifications can be determined by looking at an inductor's data sheet.

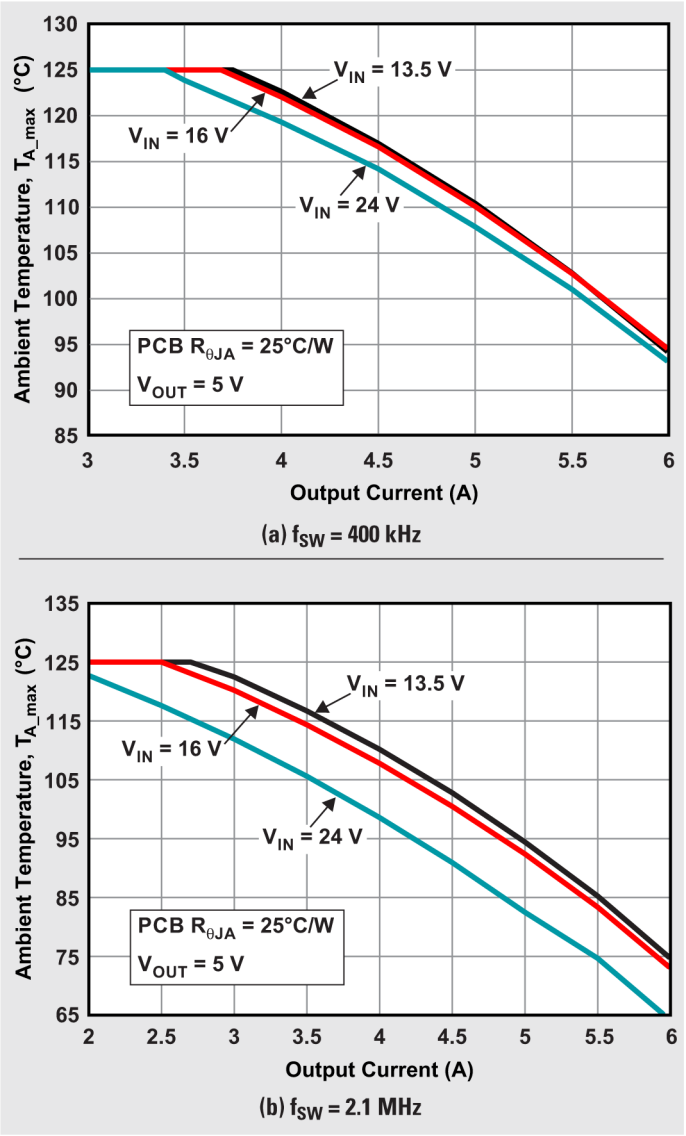

Figure 7. *Output Power Derating Curves of the LM61460-Q1 Converter*

In addition to inductor selection, inductor placement is also a factor in board thermal performance. Sometimes the selected inductor will minimize the solution size and improve the EMI performance of the power supply. Often that inductor will have a very small physical size and a higher DC resistance. This will cause the inductor to heat up, especially at high buck-converter output currents. This can be an issue with designs that have a small switch-node area, as the inductor is crowding the converter and saturating it with heat.

A converter design should balance EMI noise and thermal performance. Having an inductor with a reasonable DC resistance and switch-node area—to allow for heat conduction out of the inductor—will reduce the converter's $R_{\theta JA}$. As EMI standards become more stringent, it is important to carefully consider how large to make the switch-node area because its size will directly impact the radiated noise signature of a buck converter, whose energy will often fall in the most stringent area of the EMI sweep—the FM band.

Conclusion

Following the techniques in this article, a converter design's thermal performance can be estimated before building the first prototype board. This will enable faster-to-market project builds and avoid thermal issues down the road. In designs where thermal performance is an issue, the techniques outlined in this article can be used to further improve thermal performance and finish the PCB project.

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Product Information:

LM61460-Q1

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