Understanding the Foundations of Quiescent Current in Linear Power Systems

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Minimizing power consumption is an important design consideration. One way to do this is by selecting devices that minimize their ground or quiescent current (I_Q), such as a linear regulators or low-dropout regulators (LDOs), and to understand how I_Q affects the use of LDOs in battery-powered systems.

At a glance

This paper addresses the fundamentals of I_Q in linear-power systems and explains how to extend battery life without compromising system performance.

1 What is I_Q in an LDO?

Know the differences between similar parameters to help optimize overall power consumption.

2 How I_Q affects LDOs

Understand the relationship between I_Q and the overall power consumption of the system.

3 I_Q and dropout conditions

Predict typical LDO I_Q behavior in dropout conditions

4 I_Q and transient response

Enhance power and signal integrity with LDOs that can maintain minimal disturbance to the output voltage during the load transient response.

Introduction

With many portable medical devices, consumer electronics and building automation products now relying exclusively on battery power, design engineers are increasingly looking to minimize power consumption in order to extend battery life.

Figure 1 depicts some of the most common applications for which power consumption is a challenge, including portable blood glucose monitors, wireless smoke detectors and smart water meters. To minimize power consumption, these products must spend a majority of time in standby mode. One way to reduce overall system power consumption is to select a device that minimizes its ground or quiescent current (I_Q). In this paper, I will go over one of the most common power-management devices for minimizing current – linear regulators or low-dropout regulators (LDOs) – and explain how I_Q affects the use of LDOs in battery-powered systems.
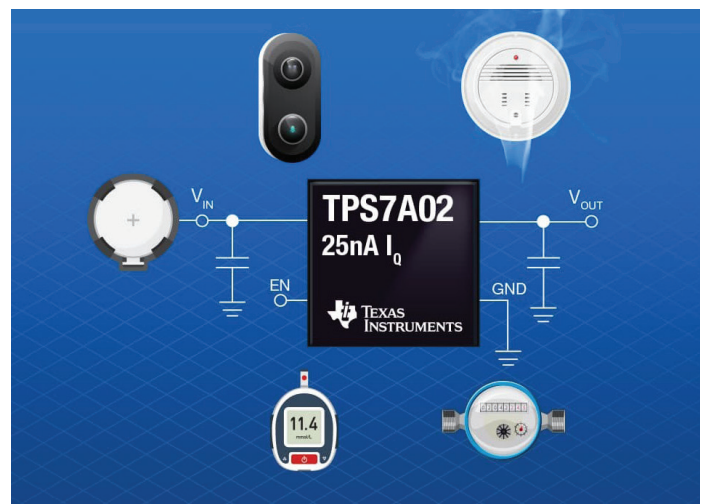

Figure 1. Common battery-powered applications that use LDOs.

What is an LDO?

An LDO is responsible for managing power by converting a higher-voltage supply down to a stable lower voltage. When compared to other power-management devices such as traditional DC/DC converters, LDOs are easy to use and are often placed after a DC/DC converter as a post-regulator or connected direct-to-battery to ensure a noise-free voltage supply.

At a fundamental level, the P-channel metal-oxide semiconductor (PMOS) LDO architecture shown in **Figure 2** consists of a pass device such as a PMOS field-effect transistor (FET), a voltage reference to provide an accurate voltage, an error amplifier to control the negative feedback loop to match the voltage reference, feedback resistors to determine the output voltage, and an output capacitor for stability.
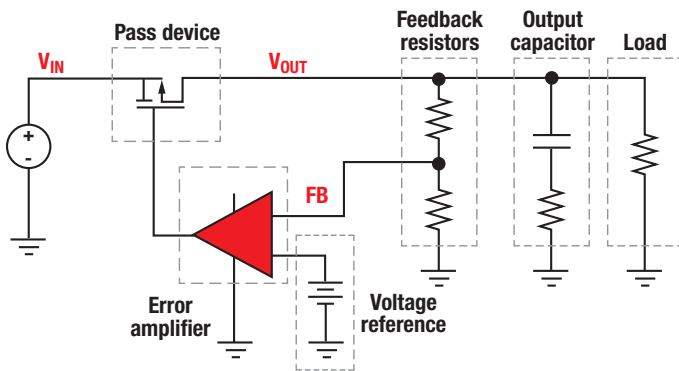

Figure 2. A PMOS LDO.

What is I_Q in a LDO?

LDO data sheets list three parameters that resemble one another:

- I_Q refers to the current drawn by the LDO in an enabled and no-load condition. For LDOs, the main contributors of I_Q are the voltage reference and error amplifier.
- Ground current (I_{GND}) is often interchangeable with I_Q and refers to the same current consumed by the LDO; when the LDO is in a low-load state, this consumption is typically in the microampere range.
- Shutdown current (I_{SHDN}) is the current drawn when a LDO is in a non-enabled condition, with the battery still connected to the system.

Most data sheets refer to these parameters because most systems have three states of operation:

- Active mode is when the expected load of an application is actively performing a function or operation.
- Low-power mode will be a low load, typically in the range of microamperes to nanoamperes, instead of an ideal no-load condition.
- Off is off; the only power consumption in this state is the leakage current of the battery and system itself.

Knowing the differences between the three parameters and three states of operation enables designers to optimize their power architectures depending on the application.

How I_Q affects LDOs – the basics

When optimizing your system for I_Q, your first consideration is the actual value of I_Q for an LDO. You must select devices that minimize the amount of total I_Q consumed by the system in order to extend battery life. Fortunately, with LDOs, calculating how much I_Q contributes to a system's power loss can be fairly straightforward. **Equation 1** dictates the relationship between I_Q and the overall power consumption of the system, PD:

$$(V_{IN} - V_{OUT}) \times I_{OUT} + (V_{IN} \times I_{GND}) = P_D \qquad (1)$$

Let's say that you used the Texas Instruments TPS7A05 LDO to regulate power to a 1.8-V wireless microcontroller from a 3-V CR2032 coin-cell battery with a capacity of 235 mAh. If the microcontroller requires an output current of 100 µA in active mode, and the TPS7A05 has 1.3 µA of I_{GND} at that load, plugging those values into Equation 1 results in:

$$(3 - 1.8) \times 0.0001 + (3 \times 0.0000013) = 123.9 \ \mu W$$

When the application switches to low-power mode, I_Q plays a much greater role in power dissipation. Continuing the previous example, if the system goes into low-power mode and I_{OUT} becomes significantly lower – 2 µA – using the same LDO (I_{GND} will go down to 1 µA at that load) results in a P_D of:

$$(3 - 1.8) \times 0.0000002 + (3 \times 0.000001) = 5.4 \ \mu W$$

In this example, I_Q represents 56% of the total power dissipated. This becomes an important design parameter for applications that spend a majority of their time in low-power modes, such as smart meters, heat and smoke detectors, thermostats, and smartwatches.

But what about situations when the product is off? As I mentioned earlier, the only power consumption to consider is from the battery leakage and devices within the system. Since the LDO and other power-management devices would be non-enabled, engineers need to use I_{SHDN} when determining power consumption in this state in place of I_Q. A product's power consumption in this state is dominated by a combination of I_{SHDN}, battery leakage (dependent on battery type and chemistry) and output capacitor leakage (which varies based on manufacturer and external conditions).

In order to minimize this power consumption, designers have implemented a simple solution in the form of a battery isolation tab, which prevents the system from consuming any power. This tab results in excellent shelf-life of low-drain products such as clocks or thermostats. Products that require the use of a high-drain rechargeable battery such as smartphones and wearables will never come out of the box 100% fully charged due to this power-consumption phenomena. That's why manufacturers recommend fully charging such devices before first-time use.

How I_Q affects a LDO – dropout conditions

Another way that I_Q affects LDOs is how I_Q behaves when introduced to a dropout condition. Dropout, or more specifically the dropout voltage, refers to the minimum differential that the input voltage must maintain above the output voltage for proper regulation. Dropout determines how efficiently an LDO operates while still maintaining output voltage regulation. A decrease in the input/output voltage to near-dropout brings the drive voltage of the FET gate in the LDO and various other circuits to their operating limits. In dropout, when all of these internal circuits are saturated, there is often a large rise in I_Q similar to that shown in **Figure 3**. Modern LDOs use a more balanced, differential drive circuitry to maintain reasonable I_Q, even in dropout.
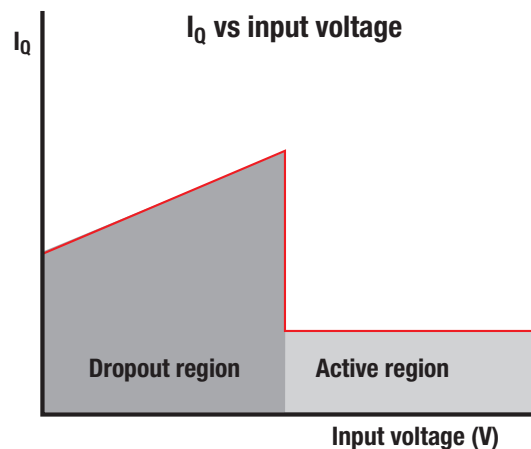

Figure 3. *Typical LDO I_Q behavior in dropout conditions.*

LDOs have a reputation as inefficient power devices because their efficiency can be determined by the output power divided by the input power (**Equation 2**):

$$\text{Efficiency} = \frac{V_{OUT}\ I_{OUT}}{V_{IN}\ I_{IN}} \times 100\% \qquad (2)$$

It is also possible to define I_Q as the difference between the input and output current (**Equation 3**):

$$I_{IN} = I_{OUT} + I_Q \qquad (3)$$

By replacing the input current in equation 2 with equation 3, you can see the importance of minimizing both the dropout and I_Q in order to increase efficiency. If the input voltage and output voltage are predetermined in the system, efficiency will result in **Equation 4**, current efficiency:

$$\text{Current efficiency} = \frac{I_{OUT}}{I_{OUT} + I_Q} \times 100\% \qquad (4)$$

In order to achieve the highest current efficiency, having the lowest I_Q possible is absolutely critical for optimizing power consumption.

Returning to the previous example, the [TPS7A05](#) will have an overall power efficiency of 59% in active mode and a much lower efficiency of 40% in low-power mode, as shown in **Table 1** on the next page (I_{GND} in place of I_Q because there is a load current). Selecting a device with minimal I_{GND} will maximize current efficiency in both modes, which will help increase overall efficiency and allow you to meet a stricter power budget. If the previous example had

used the **TPS7A02** instead, which has an inherent I_Q of 25 nA, and I_{GND} of 250 nA then low-power mode efficiency would increase by 19% to 59%, driven by the increase in current efficiency due to the predetermined input and output voltages. This further confirms that while I_{GND} isn't as meaningful of a parameter when in active mode, it is absolutely critical to consider it in low-power-mode situations. You will also see an improvement in shelf life given the I_{SHDN} of 3 nA compared to the 100 nA of the TPS7A05.

	TPS7A05 active mode	TPS7A05 low-power mode	TPS7A02 active mode	TPS7A02 low-power mode
I_{OUT} (µA)	100	2	100	2
I_{GND} (µA)	1.3	1	0.25	0.003
I_Q (µA)	1		0.0025	
I_{SHDN} (µA)	100		3	
Power efficiency	59%	40%	60%	59%
Current efficiency	99%	67%	100%	99%

Table 1. *Power efficiency comparison.*

How I_Q affects an LDO – transient response

Your final consideration when designing with low I_Q devices is dynamic performance, which refers to the device's load or line transient performance. Traditionally, low-I_Q LDOs have had fairly slow response times, leading to larger disturbances from load and line voltage transients. As a general rule, low-I_Q LDOs will have slower transient response times than high-I_Q LDOs because it takes current to charge and discharge the internal nodes when a transient occurs. The less current flowing through the internal nodes, the more time it takes to charge the parasitic capacitances internal to the LDO.

When comparing LDOs with small differences in I_Q, you cannot assume that different LDO designs will have better or worse transient response, since they will also have different internal structures that may lead to faster or slower response times. An LDO with an I_Q of 1 mA will most

certainly have a faster transient response than an LDO with an I_Q of 1 µA. Having the output voltage respond quickly to changes in load or line voltage with minimal deviation is critical when powering sensitive analog and digital loads such as smart meters, portable medical devices, Internet of Things nodes or smartwatches. These applications spend a majority of their time in low-power mode, which means that the system must shift quickly into active mode and back into low-power mode.

The load transient response is the change in output voltage when there is a change in the load current. Depending on the LDO, the load transient response may differ. **Figure 4** shows the load transient response of the TPS7A02 when the device experiences a change in load current from 1 mA to 200 mA in 1 µs. The output voltage drops approximately 145 mV, but then settles back to the nominal output voltage in less than 5 µs. In Figure 4, notice the overshoot during the other side of the load transient; this type of behavior is common for LDOs, since unlike a switching regulator, LDOs do not have a low-side FET capable of pulling the output lower when it rises too high. The LDO's response time determines the magnitude of the overshoot, but how long the output voltage takes to come back to regulation is determined by the load, which has to discharge the output capacitor.
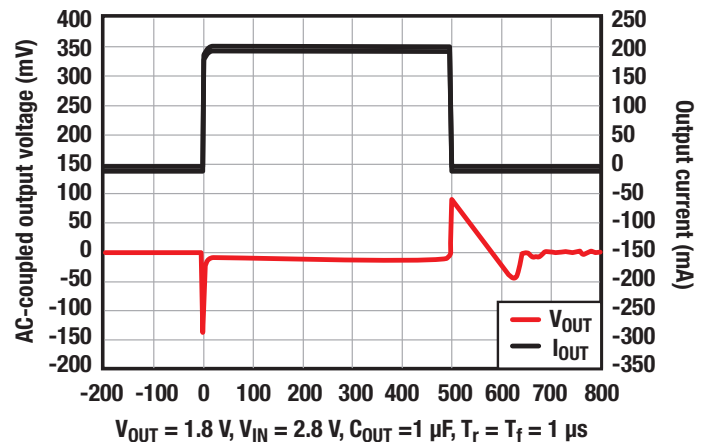

Figure 4. *TPS7A02 load transient response.*

The line transient response is the change in output voltage when there is a change in the input voltage. **Figure 5** shows the line transient response of the TPS7A02 when the device experiences a change in input voltage from 2.8 V to 4.8 V at a 1-V/μs slew rate. Line transients will differ depending on the application, but what is important is the slew rate driving the input voltage. Generally, the slower the slew rate, the less the output voltage deviation. This response is fairly important in applications that can experience any type of input voltage change, such as motor drives in drones.

V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} =1 μF, slew rate = 1 V/μs
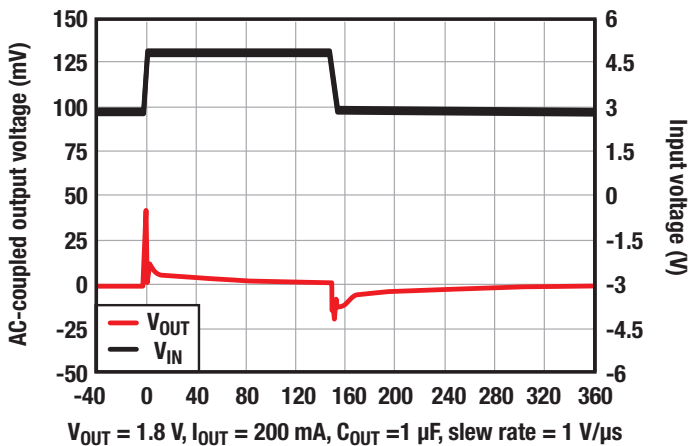
Figure 5. TPS7A02 line transient response.

Conclusion

Understanding how I_Q and dynamic performance affect an LDO will help you select power-management devices for battery-powered systems. The first step when selecting a power-management device is to determine whether it can perform the regulation based on the input and output voltage, the load current and the target I_Q. Once you know these parameters, you can get a basic idea of the load profile based on the use cases of the system and begin comparing, starting with data-sheet graphs. If you need additional bench measurements, actual devices and evaluation modules will ultimately validate whether or not the device is suitable for your application. There are many misconceptions about LDOs, and knowing these differences will help you optimize your device selection and ultimately simplify the LDO design process.

To learn more about low I_Q, go to: **ti.com/lowiq**.

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