The Impact of Various PLL Parameters on System Performance

TEXAS
INSTRUMENTS

Literature Number: SNAA109

The Impact of Various PLL Parameters on System Performance

BY: Dean Banerjee, Wireless Applications

Introduction

This article investigates the impact of various PLL parameters, such as lock time, reference spurs, and phase noise, and reference spurs on general system performance of a typical receiver. Although the impact of the PLL performance on the transmitter is not discussed, there are many similar issues.
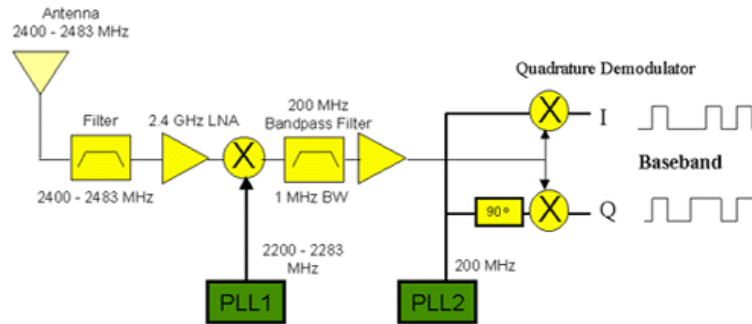

Figure 1 Typical Receiver Architecture

In this example there are 79 channels with center frequencies starting at 2.402 GHZ and ending at 2.480 GHz, which are spaced 1 MHz apart. QPSK modulation is used, which means that there is actually 2 MB/s of information in each 1 MHz channel. In this example, suppose a channel with frequency 2.450 GHz is to be received. This signal goes through the preselection filter and the first PLL (PLL1) is tuned to 2.250 GHz, exactly 200 MHz below the signal value to be received. This difference frequency of 200 MHz as well as the sum of the frequencies at 2650 MHz enter the bandpass filter. Only the 200 MHz signal passes through the filter and LNA to the second PLL. The second PLL is always tuned at 200 MHz, and recovers the demodulated data, which is sent to the baseband processing.

Impact of Lock Time on System Performance

The lock time is the time that it takes the PLL to switch from one frequency to another for a given frequency change to a given frequency tolerance. For many cellular and cordless phones, this is typically in the order of several hundred microseconds. In cable TV applications, this requirement can be much longer in the order of 100 mS. The difference in these requirements is because the cellular phone needs to be able to switch frequencies much more often, while the cable TV application needs to only switch when the user decides to change the channel, and does not really matter unless it can be sensed by human perception.

In the time that the PLL takes to switch frequencies, no data can be transmitted, so having a lock time that is too long can reduce the data rate of the system. For example, the Bluetooth standard described at www.bluetooth.com says that a system can hop up to 1600 hops/second. In this case, the PLL can stay on a channel only 625 uS, which means that the PLL lock time can be only a fraction of this, or else the system will be waiting too long for the PLL to switch frequencies and the data rate will be too slow.

In the example above, PLL2 is tuned to a fixed frequency, so the lock time would most likely not be an issue. Since this lock time requirement is typically not very stringent, it allows for the loop bandwidth of the PLL system to be chosen relatively narrow, which leads lower RMS phase error and lower spurious emissions.

For PLL1, the lock time requirements are typically more because this PLL is usually tunable. Changing frequencies is necessary if the frequency the user is on becomes faded or there is interference on that channel. Certain frequency-hopping standards, dictate that the device needs to change channels at a constant rate to avoid causing narrowband interference and to reduce Rayleigh fading.

Impact of Reference Spurs on System Performance

Reference spurs are spurious emissions that occur from the carrier frequency at an offset equal to the channel spacing. These are usually caused by leakage and mismatch in the charge pump of a PLL. Although the reference spurs usually occur outside of the band of interest, they can enter the mixers and be translated back onto the band of interest. In this particular receiver, consider what happens in addition to producing the desired 2.250 GHz carrier, PLL1 produces spurious sidebands that are spaced at a 1 MHz offset from the carrier. These sidebands would be at 2.224 MHz and 2.226 MHz. Now suppose that in addition to the desired carrier to be received at 2450 MHz, there is another user on the system at who is receiving a signal at 2451 MHz, and this signal at 2451 MHz is much stronger than the signal at 2450 MHz. The other user's signal at 2451 MHz can mix with the spur at 2226 MHz, and produce a frequency of 200 MHz, which will interfere with the desired signal. This is just one possible way that reference spur can cause a problem. In a transmitter, reference spurs can cause interference in a similar way.

For PLL2, the loop bandwidth is often chosen to minimize RMS phase error. Although this optimal RMS phase error loop bandwidth is application specific, it is typically on the order of a KHz or so. Now the channel spacing for PLL2 may not be intuitively obvious in this example, but should be chosen equal to the greatest common multiple of the output frequency/frequencies and the crystal reference frequency used. This channel spacing is typically much larger than the loop bandwidth, therefore making reference spurs much less challenging for PLL2. This is perhaps the one reason for why it is getting more popular to integrate the functionality of PLL2 in ASICs.

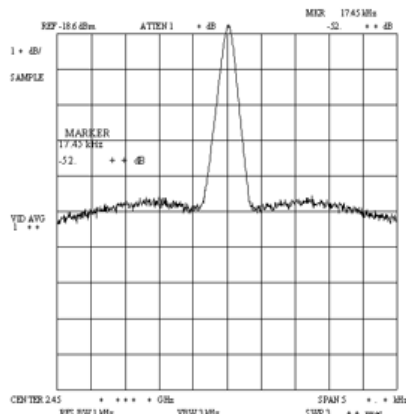### Impact of Phase Noise on System Performance

Figure 2 Typical Phase Noise spectrum

The phase noise spectral density of a PLL system refers to the noise power of the PLL versus the offset frequency. Close to the carrier, within the loop bandwidth of the PLL, this noise is commonly dominated by the phase detector of the PLL, and farther out, it is typically dominated by the VCO (Voltage Controlled Oscillator).

There are a few reasons why the phase noise is relevant to the system. If the carrier signal has phase noise around it, then the carrier from an undesired user in the system can mix with this noise and produce an unwanted spur at the desired carrier frequency. This is why standards often dictate a spectral mask requirement, which gives the maximum phase versus frequency offset for the carrier.

Another way that the phase noise of the PLL can contribute is the RMS phase error contribution. For a noisy sine wave, the zero crossings of the signal will not always occur at the reference period of the signal, but will actually statistically vary from this with a mean of zero and a standard deviation equal to the RMS phase error. If the RMS phase error is sufficiently large, then it can cause the symbol that is sent to be misinterpreted as a different symbol. This will now be discussed in greater detail.

The constellation diagram shows the relative phases of the I (in phase) and Q (in quadrature -- 90 degrees phase shift) signals. Each point on the constellation diagram corresponds to a different symbol, which could represent multiple bits. Below is a constellation diagram for QPSK.
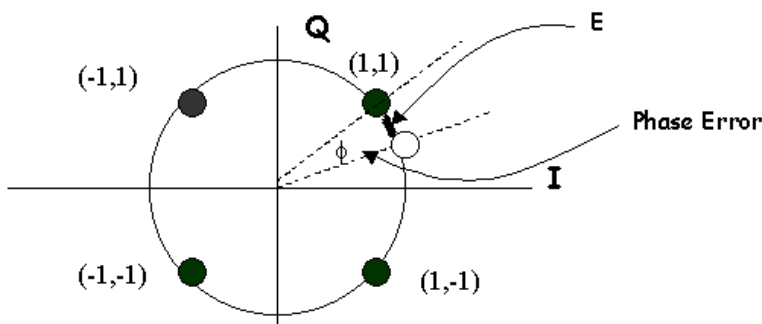
Figure 3 Impact of RMS phase Error Seen on a Constellation Diagram

Consider an ideal system in which the only noise-producing component is the PLL in the receiver. In this example, the symbol corresponding to the bits (1,1) is the intended message indicated by the darkened circle. However, because the PLL has a non-zero RMS phase error contribution, the received signal is actually the non-filled circle. If this experiment was repeated, then it would be found that the phase error between the received and intended signal was normally distributed with a standard deviation equal to the RMS phase error. It should be clear that if the RMS phase error of the system was too large, it could actually cause a the message to be interpreted as (-1, 1) or (1,-1). It should also be clear from this constellation diagram interpretation of RMS phase error that higher order modulation schemes are more subject to the RMS phase error of the PLL.

$$ RMS\ Phase\ Error = \frac{180}{\pi} \bullet \sqrt{\int_{0}^{\infty} L(f) \bullet df} $$

In the above formula, the phase noise, L(f), is proportional to the voltage noise squared. By integrating this voltage noise over the frequency band of interest and applying the square root, this is converting this into a root mean square error for the zero crossings of the voltage signal. This is then converted from radians into degrees. Recall also that the standard deviation by any random variable is given by: s = E{ (x - m)2 }

The phase noise of PLL1 tends to be more critical and challenging to meet than the phase noise of PLL2. The reason for this is that PLL1 must tune over all 79 channels, while PLL2 only has to tune to a single frequency. Sometimes, PLL2 is adjusted to compensate for different FCC requirements in different countries, but it is not changed once this is done. For these reasons, the loop bandwidth of PLL1 is typically wider than that for PLL2, and therefore there is a larger RMS error contribution. In this case, the bandwidth of interest could be from 0 to 500 KHz. This corresponds to a 1 MHz channel spacing.

Concluding Remarks
This paper has explained some of the reasons why phase noise, spurs, and lock time of a PLL can be relevant factors in a receiver. The exact requirements for these parameters are seldom directly dictated by the communication standard itself, but are usually implied indirectly. Although this article has only discussed a typical receiver, many of the issues in a typical transmitter regarding lock time, reference spurs, and phase noise are very similar. Some of the other PLL factors that can also be relevant are current consumption, which is most relevant in battery powered application, frequency of operation, and features, such as lock detect.

Current Edition   Archives

Site Map | About "Cookies" | National is ISO/TS16949 Certified | Privacy/Security Statement | Contact Us/Feedback | RSS Feed | Site Terms & Conditions of Use

IMPORTANT NOTICE