ADC08B200,LMH6552,LMH6555

Adaptive Speed Control for Automotive Systems

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No. 112

Adaptive Speed Control for Automotive Systems

— By Nicholas Gray, Applications Engineer

Electronic systems for distance ranging (measuring distance) include SOund Navigation And Ranging (SONAR), RAdio Direction And Ranging (RADAR), and LIght Detection And Ranging (LIDAR). These systems all use the same general principles to determine the distance to an object (the target). They all consist of an energy source and a method of detecting the reflected signal and examining it to determine various things about that object. One of the most common of these applications is determining the distance, or range, to a target.

RADAR is commonly used to detect and monitor relatively large objects, such as aircraft and automobiles. SONAR is commonly used to detect and monitor underwater objects, such as submarine craft and fish. LIDAR, a relatively new technology, has a number of uses, such as distance measurement for surveying and construction, military range finding, vehicle detection at toll booths and the distance between vehicles.

One of the newest applications of LIDAR is Adaptive Speed Control for automobiles. In this application the cruise control is set by the driver to the speed he or she wishes to travel, just as in other cruise control systems. However, as the vehicle approaches a slower moving vehicle, the adaptive speed control reduces the vehicle's speed to match that of the vehicle ahead while maintaining a safe distance.

This article discusses the principles and design of the front end of an automotive adaptive speed control circuit.

System Alternatives

The possible methods used by such a system include the use of Continuous Wave (CW) signals or pulsed signals.

CW systems operate on the principle that the target reflects a phase shifted version of the transmitted signal. A phase comparator in the receiver compares the phase shifted version of the received signal with the original signal. The phase difference between the transmitted and received signals and the rate of change of this difference can be used to determine distance and rate of change of distance, or rate of closure.

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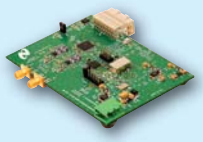
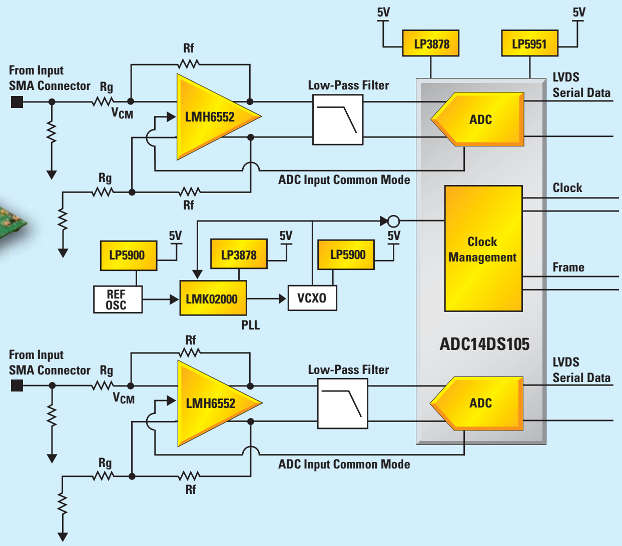


Low IF Receiver Subsystem



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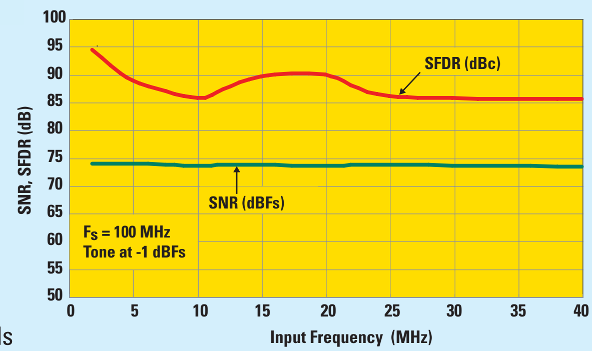

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Adaptive Speed Control for Automotive Systems

In a pulsed laser system, short light pulses are sent and received. The Time Of Flight (TOF) and its rate of change are used to determine the range of (distance to) the target and the rate of closure.

These systems all require the use of an electrical signal source, a power amplifier and a transmitter to send out a signal and a receiving sensor, amplifier, signal conditioner, and a high-speed Analog-to-Digital Converter (ADC) to deliver a digitized version of the received signal to memory, from which a DSP, FPGA, or microcontroller recovers the data at a lower-rate for processing.

A major disadvantage of CW systems in automotive applications is the system cost. A LIDAR system using a pulsed laser provides a much more cost-effective solution, so it tends to be the architecture of choice.

System Requirements

The distance that can be measured depends upon several factors, including the peak power of the transmitted signal, the signal divergence and dispersion, the transmittance of the medium through which the signal travels, target reflectivity, and the receiver sensitivity.

The range or maximum measurable distance to a target depends upon the laser output power, the optical sensitivity of the receiver, how well the atmosphere transmits optical energy, and how much the laser beam diverges from a perfectly straight path.

There are three basic detector choices for picking up low light levels in the receiver: the silicon PIN detector, the silicon avalanche photo diode (APD), and the photomultiplier tube. APDs are widely used in many applications because they offer a combination of high speed and high sensitivity that is unmatched by other detectors.

The receiver APD converts the received light pulses to electrical currents proportional to the amount of light that falls upon it. A transimpedance amplifier is then used to convert this current to a voltage.

As is always the case in analog systems, low noise requires the best noise performance in the earlier stages of the signal path, requiring the use of low-noise, high-gain components in that area.

A good transimpedance amplifier should have high gain, high-input impedance, ultra-low voltage and current noise, and low-input capacitance. The output of the transimpedance amplifier is amplified and may need further signal conditioning before being presented to an ADC for digitization.

The received signal is usually a fairly weak one for a more distant target as compared with nearby objects. The receiver, then, needs to be sensitive enough to adequately detect very strong signals and very weak ones, meaning a very wide system dynamic range is required. A system dynamic range requirement in the range of 100 dB is not unusual and is commonly achieved with an analog Variable Gain Amplifier (VGA) or a Digital Variable Gain Amplifier (DVGA) prior to the ADC.

If the ADC has a differential input, a single-ended to differential converter is needed. This can be accomplished with National Semiconductor's LMH655x family of products. The last stage prior to the ADC is a voltage amplifier for those cases where the single-ended converter can not provide enough gain with the required bandwidth. For differential circuits, the LMH655x family of products can also fill this need.

The key analog components in the receive signal path of these systems is the ADC used to digitize the energy reflected from the target.

A simplified typical block diagram for the receiver is shown in ***Figure 1***. The FIFO may be incorporated into an FPGA, but it would be nice if it were on the same die as the ADC.

8-Bit, 200-MSPS ADC with 1K FIFO Buffer and Integrated PLL

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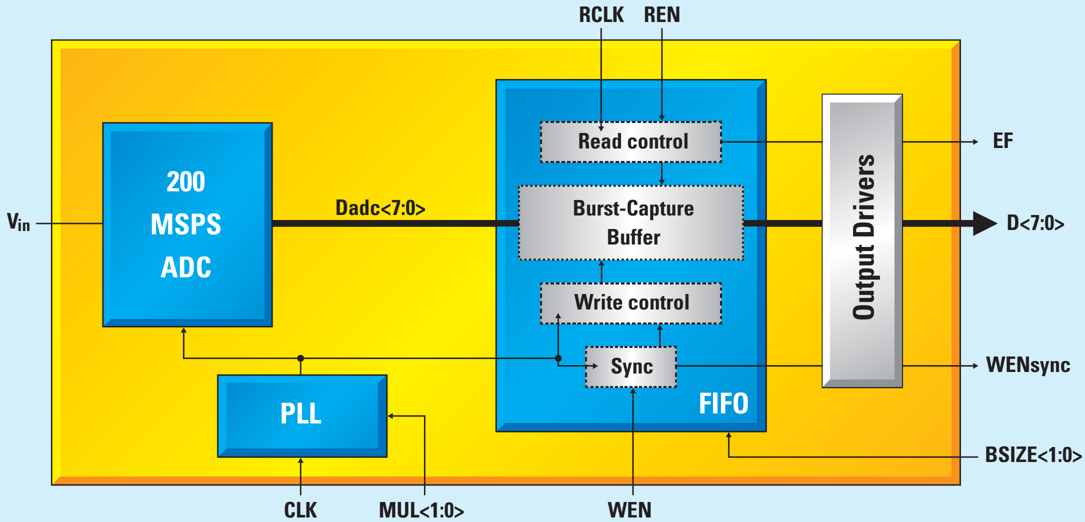

ADC08B200 Features

- Selectable buffer size up to 1k bytes for flexibility
- On-chip PLL provides option to multiply input clock signal frequency by 2, 4, or 8 times to full sample rate, reducing clocking component cost and complexity
- Direct access to internal reference ladder allows for flexibility in input voltage ranges
- Power consumption scales linearly with sampling rate
- Digital Output Test pattern for system debug

Product ID	Sampling Rate	Power	ENOB (Bits)	SNR (dB)	SFDR (dB)	THD (dBc)	FIN (MHz)	Packaging
ADC08B200	200 MSPS	2 mW/MSPS	7.4	47	56	-55	10	TQFP-48
ADC08200	200 MSPS	1.05 mW/MSPS	7.4	46	58	-58	10	TSSOP-24
ADC08100	100 MSPS	1.3 mW/MSPS	7.5	47	60	-60	10	TSSOP-24

Applications

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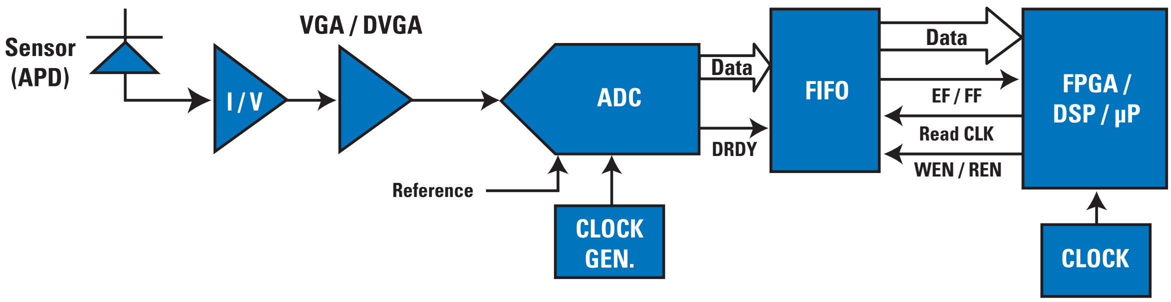

Figure 1. Ranging System Block Diagram

ADC Requirements

The accuracy of TOF measurements, the range measurement, depends upon the pulse width of the laser and the speed and accuracy of the ADC used, so the ADC used to digitize the pulses reflected from the target is the key analog component in the receive signal path.

We find the minimum ADC sample rate to be:

Min f_S = (c / res) samples per second

where:

f_S = ADC sample rate
c = speed of light
res = distance resolution

In the above equation "c" and "res" must be in compatible units. That is, if "res" is in feet, then "c" must be in feet per second.

For automotive LIDAR systems, the accuracy requirement for distance measurements might be on the order of ±3 feet. Since the distance measured is a round trip TOF, the measurement resolution needed is twice 3 feet, or 6 feet. Considering that the speed of light is 299,792,458 meters per second (generally rounded to 3 x 10^8 meters per second) or 9.84 x 10^8 feet/second, we find the minimum ADC sample rate to be:

Min f_S = (c / res) samples per second
= (9.84 x 10^8 ft/sec) / 6ft
= 163.9 Megasample per second

As a sanity check we determine that the sample interval is

Sample interval = 1 / f_S
= 1 / 1.639E8
= 6.1ns

The round trip distance traveled in a given time is

Distance = Signal Speed x TOF

Since this is the round trip distance, the one way distance is half of this and is the same as the distance resolution.

The signal speed (that of light) is 9.84 x 10^8 ft/sec and the time of flight is 6.1 ns:

Resolution = 9.84 x 10^8 ft/sec x 6.1 x10-9 sec /2
= 3 feet

As mentioned before, it would be nice to have an ADC with an on-chip buffer. The ADC08B200 is a 200 MSPS ADC with a 1 kilobyte on-chip buffer, and also contains an on-chip clock multiplier so that 200 MSPS can be obtained with an external clock rate as low as 25 MHz.

Using the ADC08B200 at 200 MSPS provides a round trip distance resolution of:

Resolution = c / f_S / 2

Resolution = 9.84 x 10^8 ft/sec / 2 x 10^8 sec / 2
= 2.46 feet

Adaptive Speed Control for Automotive Systems

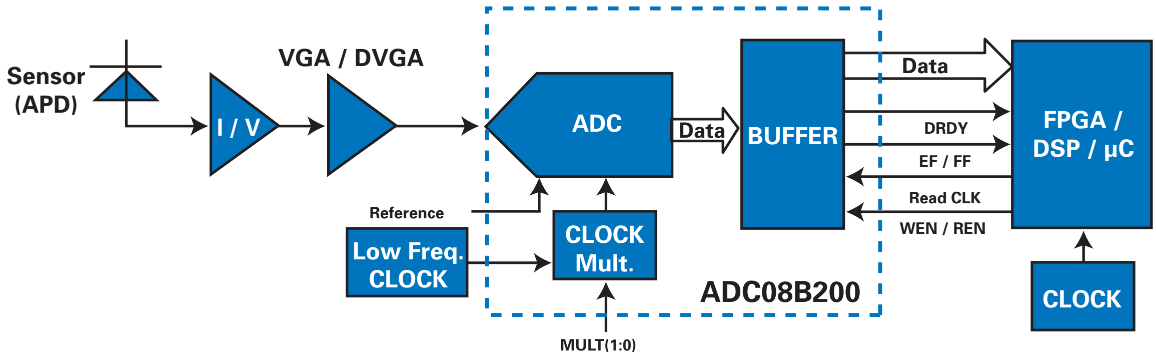

Figure 2. Ranging circuit using the ADC08B200

Incorporating the buffer within the ADC means that the FPGA or DSP can be smaller than it would have to be if the buffer must be incorporated into it, and eliminates any need for a stand-along FIFO.

All of this makes the ADC08B200 an ideal product for use in an automotive LIDAR adaptive speed control system.

ADC Circuit for LIDAR Systems

At the very heart of the automotive LIDAR receiver design lies the ADC08B200, which simplifies the receiver design, as shown in the system block diagram of ***Figure 2***. In addition to containing the A/D converter, the ADC08B200 has a clock multiplier that allows the use of a low-frequency clock oscillator and a 1 kilobyte buffer that relaxes the speed and complexity requirements of the FPGA, DSP, or microcontroller.

The clock multiplier can multiply the input clock frequency by 1, 2, 4, or 8. This permits the use of a clock source as low as 25 MHz to obtain 200 MSPS operation. If desired, the external clock source for the ADC08B200 may be the same as the clock for the FPGA / DSP / microcontroller.

The buffer can be read at any desired rate up 200 MHz. The buffer can also be bypassed, in which case the data is continuously streamed out at the ADC sample rate.

To minimize average power consumption, the ADC core of the ADC08B200 may be powered down while the buffer is being read. It is also possible to power down the entire ADC08B200, including the buffer, when it is desired to maintain system power but not use the data converter.

ADC08B200 Circuit

The design of the circuit around the ADC08B200 is shown in ***Figure 3*** and is straight forward. Very good performance may be obtained with reference voltages as low as 1 volt. Keeping the reference voltage low eases the gain requirements of the signal from the APD, so this design uses the 1.2V LM4041-1.2 shunt reference to provide the ADC08B200 top reference, and the bottom reference is at ground. Of course, if the minimum output from the amplifier, VGA, or DVGA does not go to ground, the bottom reference may be raised above ground to accomodate that.

With a 1.2V reference and the minimum ADC reference ladder resistance of 145Ω, the maximum reference current is about 8.3 mA. The maximum current for the LM4041-1.2 is specied at 15 mA. The design should prevent more than 15 mA from flowing through the LM4041-1.2 if the ADC08B200 were not in place, so the reference pull-up resistor has a minimum value of:

(3.6V - 1.2V) / 15 mA = 240Ω

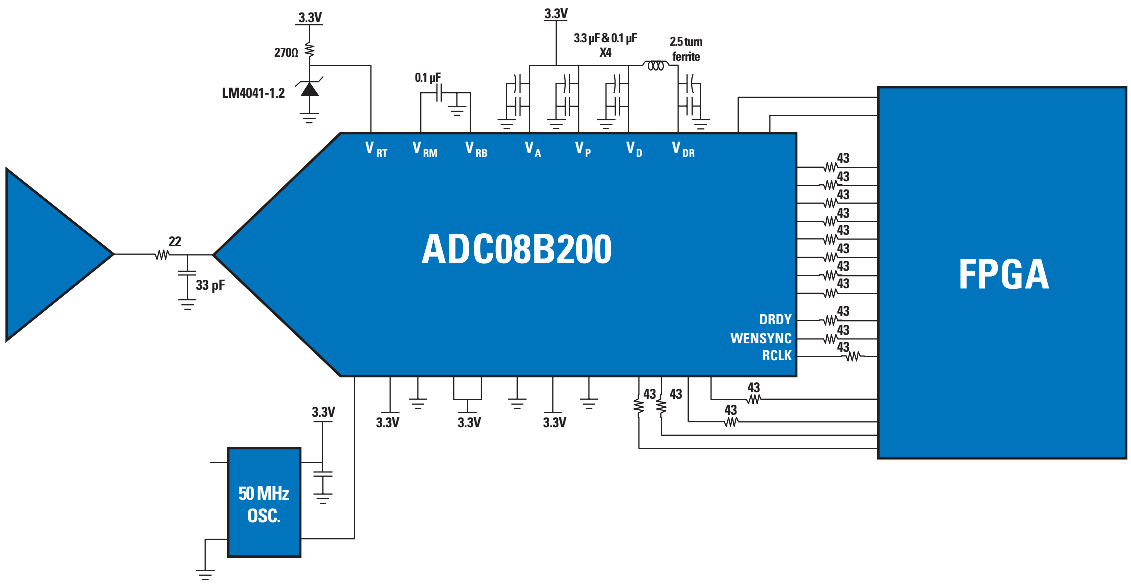

Figure 3. ADC circuit solution

The 3.6V is the high-end tolerance of the 3.3V supply. Using a 270Ω resistor will allow a 5% tolerance.

The MULT1 input of the ADC08B200 is high and the MULT0 input is low to multiply the 50 MHz CLK input by 4 and obtain 200 MSPS. Since BSIZE0 and BSIZE1 are both high, the maximum buffer size of 1024 bytes is used. See the ADC08B200 data sheet for more information on using these pins.

The read clock, RCLK, is driven by the FPGA and is used to read the data from the ADC08B200 buffer and the DRDY signal from the ADC08B200 is used to latch the data into the FGPA.

The ADC08B200 is never completely powered down, so the PD pin is grounded. However, it is desired to minimize power consumption, so the quantizer is powered down with the PDADC pin under control of the FPGA. When the PDADC pin is high, the ADC itself is powered down, but the buffer remains active so that it may be read.

Summary

As challenging as the design of distance ranging systems may be, National's ADC08B200 enables minimization of circuitry and cost while removing some of the burden of the design of these systems. ■

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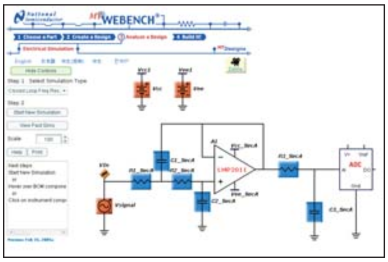

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