Radiation Report

LMK04832-SP TID RLAT Report V009FOGX Wafer 21

ABSTRACT

LMK04832-SP, 5962R1723701VXC, wafer #21 from wafer lot V009FOGX was put through radiation lot acceptance testing (RLAT) and passed at 100 krad(Si) for application environments with dose rates of 0.57 rad(Si)/s or less. The wafer fab process used by this product was previously shown not to exhibit Enhanced Low Dose Rate Sensitivity (ELDRS) and is ELDRS-free.

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Trademarks

1 Overview

The LMK04832-SP, 5962R1723701VXC(1), uses the BiCMOS8B+ process which has been shown not to exhibit Enhanced Low Dose Rate Sensitivity (ELDRS)(2). Per MIL-STD-883 Test Method 1019(3), if an analog product is on a process that has been shown to be ELDRS-free, Total Ionizing Dose (TID) Radiation Lot Acceptance Testing (RLAT) may be done at high dose rate (HDR). In the case of BiCMOS8B+, HDR testing is the worst case condition and covers low dose rate (LDR) applications.

For RLAT of a single wafer, the sample size is 2 units for products with over 4,000 transistors per MIL-PRF-38535(4).

When tested at HDR, it is possible that one parameter might drift outside the electrical test limit at 100 krad(Si). Per TM1019, if this occurs, the units that have readings outside a test limit are put on a room temperature anneal (RTA). If after the RTA all tests recover and all readings are within the test limits, the lot is qualified for 100 krad but only for lower dose rates. The maximum dose rate is calculated by dividing the TID rating by how long the DUT was on RTA before it recovered. For more details and validation of the RTA test method on TI processes, see SNAA156.

2 Test Method

The devices under test (DUTs) were put through a 240-hour burn-in with the units biased and operational at 125°C ambient prior to the radiation testing.

Irradiation and electrical testing were done at Texas Instruments Radiation Test Facility in Santa Clara, California.

The DUTs were placed in socketed bias boards, powered up and programmed using Texas Instruments USB2ANY module and TICS Pro software prior to irradiation(5). The supply voltage was set to 3.4 V as measured on the DUT boards. The DUTs were configured so that the PLL2 loop was active and the signal to the Divider and Delay blocks was at 3.2 GHz. Different delays and frequency dividers were used on the different outputs to exercise the different components of the control circuits. The outputs were configured so that at all of the output configurations options, CML, LVPECL, LCPECL, HSDS, LVDS, and 2xLVCMOS were exercised on at least one output each.

DUT #3 went through 48-hour RTA with the DUT in the bias board and powered and configured to the same conditions as during the irradiation.

The DUTs were electrically tested at 0, 50 and 100 krad(Si) and DUT #3 was tested after the 48-hour RTA. All specified data sheet and SMD parameters were tested. In addition to the specified parameters, the test program tests many other parameters to ensure the proper operation of the device. Limits are set using a six sigma baseline. Tests are performed with the supply voltage at 3.135, 3.3 and 3.465 V. There are over 7000 parameters tested.

Table 2-1. RLAT Conditions

Wafer lot	V009FOGX
Wafer number	21
DUT serial numbers	3, 4
Test Location	Texas Instruments, Santa Clara, CA
Bias board schematic	291CR17
Bias board edge number	6609056A
Supply voltage	3.4 V
Supply current	570 mA
TICS Pro program	Single Loop-CLKin1=1MHz-8_Outputs_VCO1=3200MHz_rev2.txt
VCO and PLL frequency	3.2 GHz
Test programs	GCR4832HB, GQR4832HB
Electrical test supply voltage	3.135 V, 3.3 V, 3.465 V
Dose Rate	61.5 rad(Si)/s
Test points	0, 50, 100 krad(Si)
RTA	48 hours
Test dates	October 28 and 30, 2020

3 Results

DUT #4 passed all tests at 100 krad(Si). On DUT #3, one test, VTUNE reset pin voltage, was outside the test limit at 100 krad(Si). This is not a datasheet or SMD test but an internal functional test to ensure optimum calibration of the VCO over temperature. DUT #3 was put through a 48-hour RTA and retested. After the 48-hour RTA, DUT #3 recovered, all tests passed and the VTUNE reset pin voltage returned to a value close to the pre irradiation value. Per TM1019, this wafer is qualified for 100 krad(Si) for application dose rates of 0.57 rad(Si)/s or less.

Over 7000 parameters were tested. Appendix A shows the results, statistics and plots for select representative tests. The first test shown is the VTUNE reset voltage test in which DUT #3 was outside the limit after 100 krad(Si) but recovered after RTA.

4 References

1. Texas Instruments , Dallas, TX, “LMK04832-SP Space Grade Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner,” Nov. 2020, https://www.ti.com/lit/ds/symlink/lmk04832-sp.pdf
2. Texas Instruments , Dallas, TX, “LMK04832-SP ELDRS Characterization Report,” Nov. 2020 https://www.ti.com/seclit/rr/slvk054/slvk054.pdf
3. Test Method Standard, Microcircuits, MIL-STD-883, Dept. Defense, DLA Land and Maritime, Columbus, OH, https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-STD-883/std883-1.pdf
4. Performance Specification, Integrated Circuits (Microcircuits) Manufacturting, MIL-PRF-38535, Depart. Defence DLA Land and Maritime, Columbus OH, https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-PRF-38535/prf38535.pdf
5. Texas Instruments , Dallas, TX, “LMK04832-SP Space Grade Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner,” Nov. 2020, https://www.ti.com/lit/ds/symlink/lmk04832-sp.pdf

A RLAT Data and Plots

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