

# BIG3GIG EVALUATION BOARD

## ADC083000, ADC08B3000

## MANUFACTURING KIT / REFERENCE DESIGN

National Semiconductor GHz 8 bit ADC + XILINX Virtex 4

### SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.

#### Print Instructions:

- To create a readable printout, we recommend to use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.


### SYSTEM CONFIGURATION

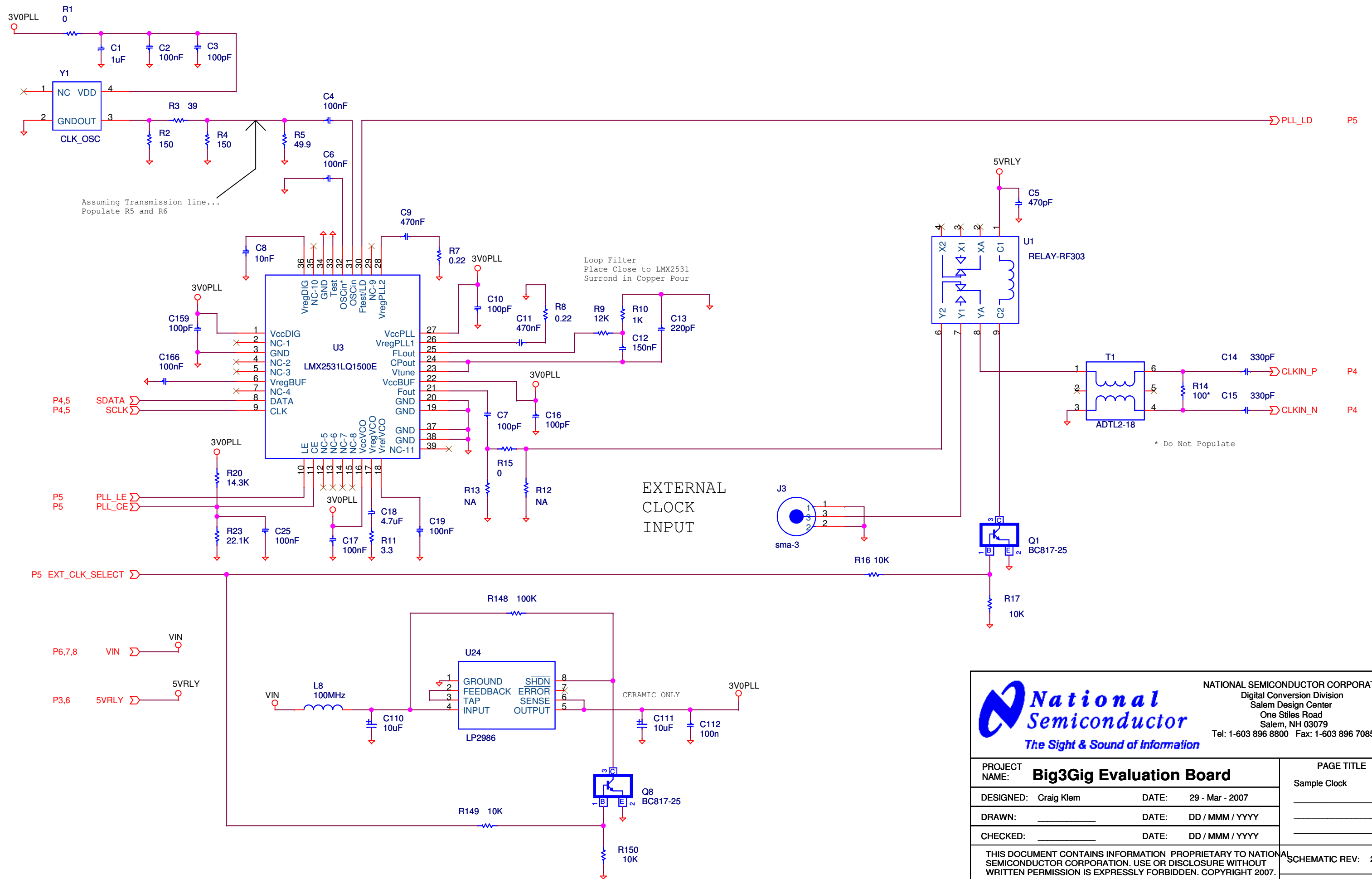
Module	Configuration	Description
FRONT END	1 channel DIFF. / SINGLE ENDED	AC AND DC COUPLING OF SIGNAL PATH
CLOCK SOURCE	SINGLE ENDED	LMX2531LQ1500E
FPGA		XC4VLX15-10SFG363C - 363 PIN BGA
USB I/F		CY7C68013A EZ USB

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# PRELIMINARY

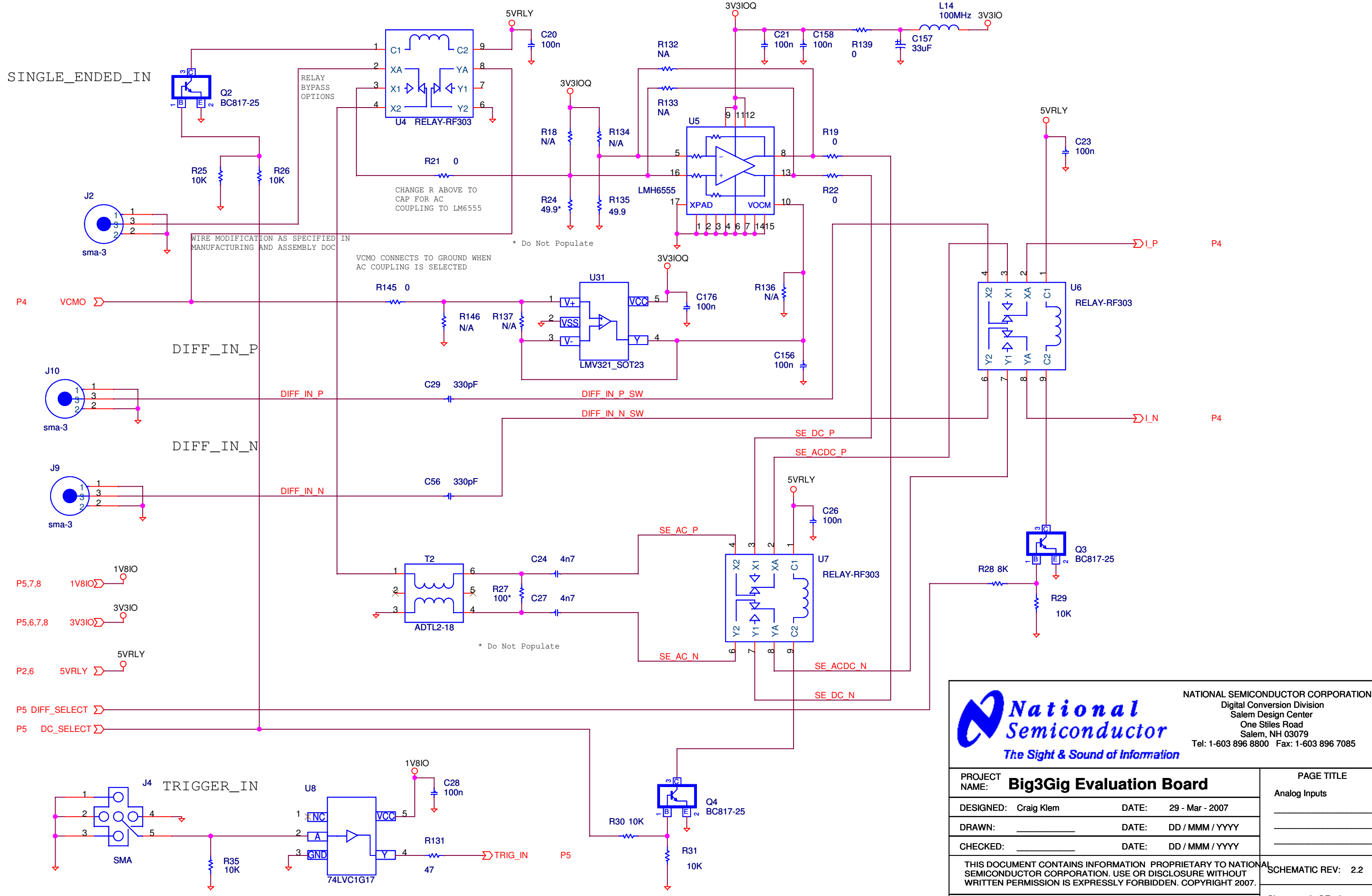
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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		
DESIGNED: Craig Klem	DATE: 29 - Mar - 2007	LAYOUT JOB#: _____
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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE Sample Clock
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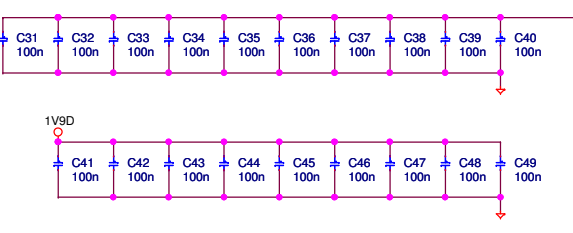
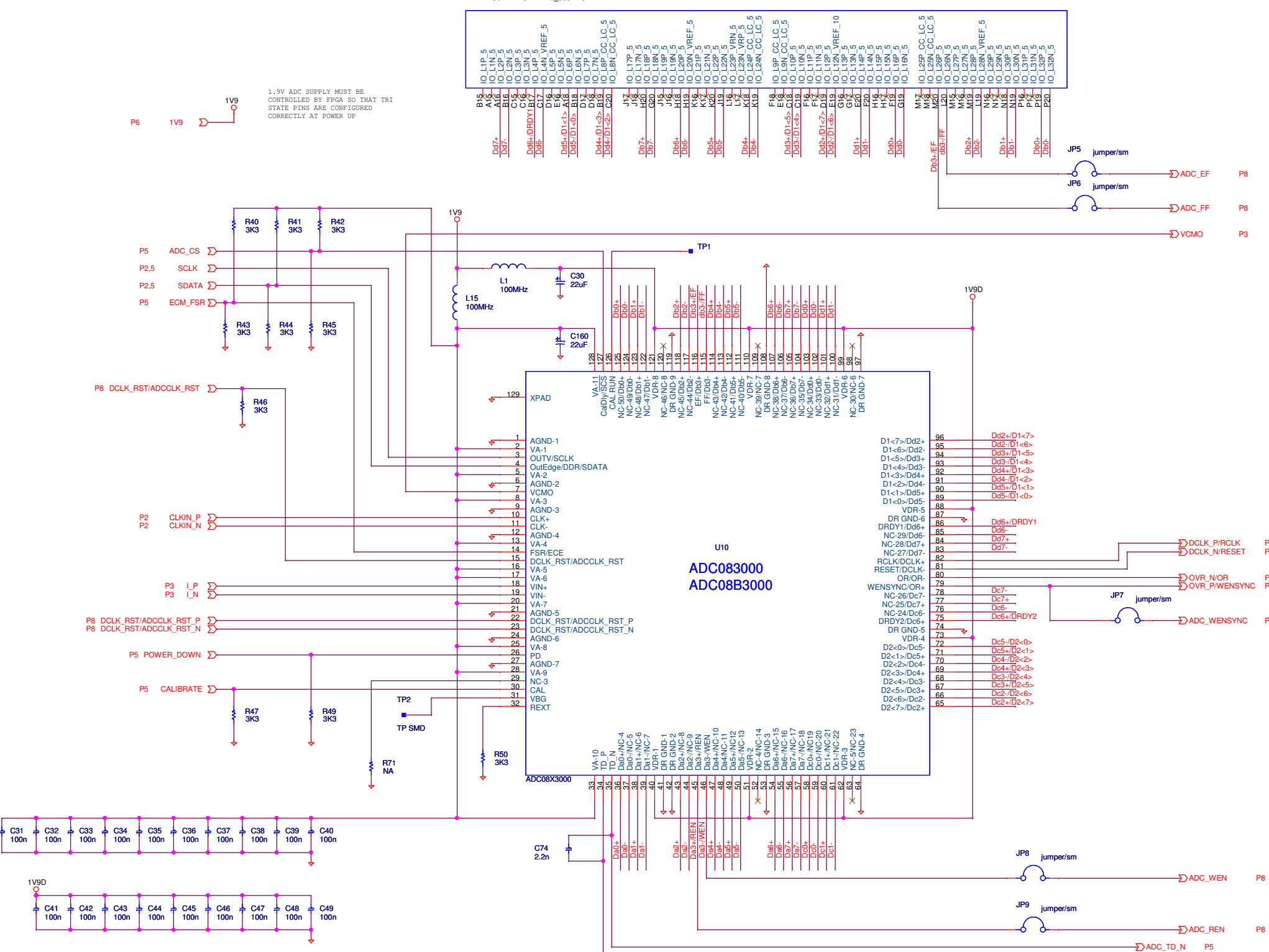


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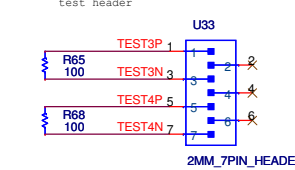
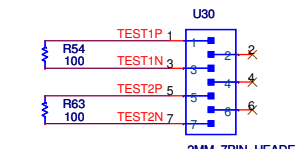
PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE
DESIGNED: Craig Klem		Analog Inputs
DATE: 29 - Mar - 2007		_____
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1.9V ADC SUPPLY MUST BE CONTROLLED BY FPGA SO THAT TRI STATE PINS ARE CONFIGURED CORRECTLY AT POWER UP



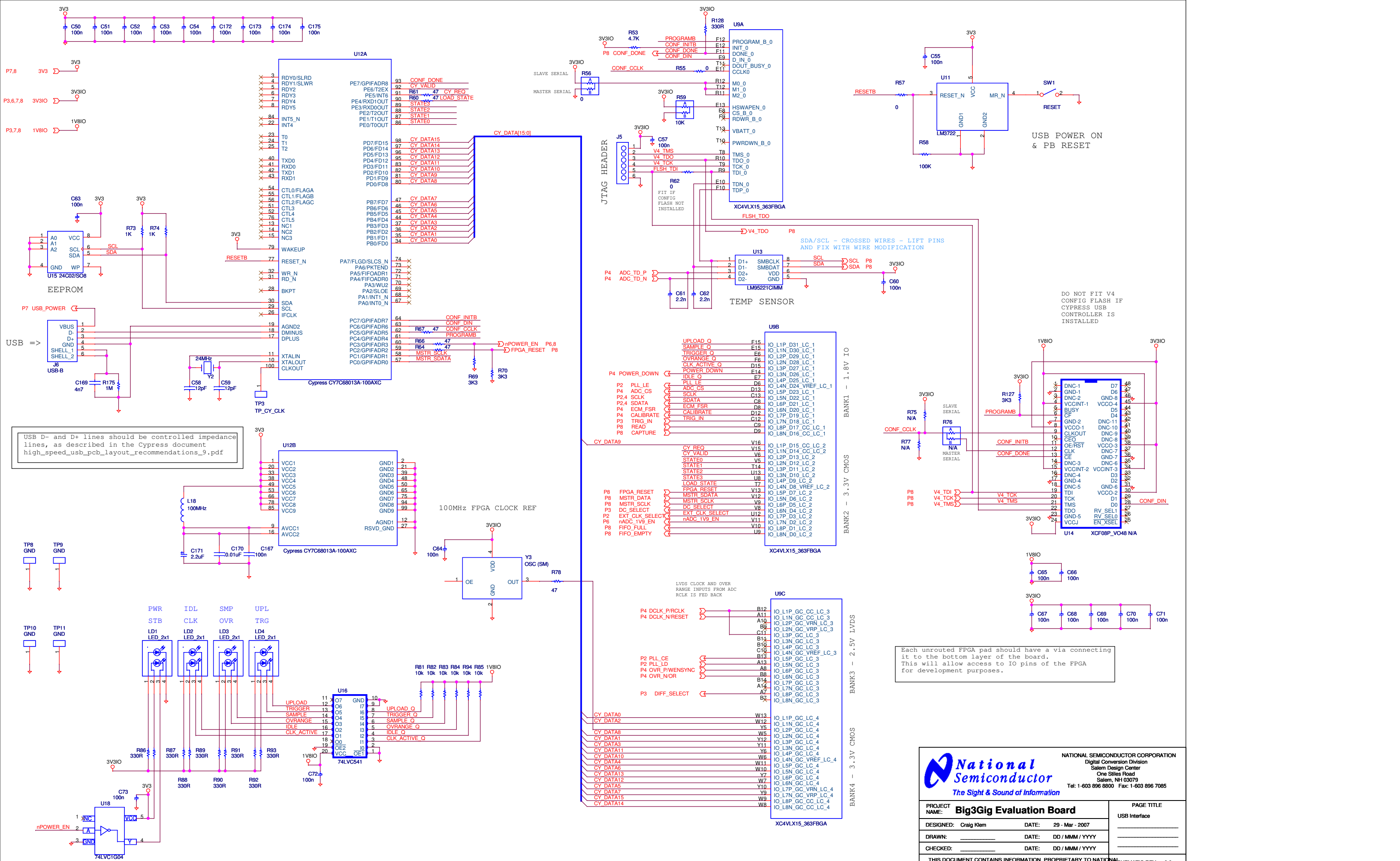
B15	IO_L1P_5
A15	IO_L1N_5
D07-	IO_L2P_5
D07+	IO_L2N_5
C18	IO_L3P_5
C19	IO_L3N_5
D16	IO_L4N_VREF_5
D17	IO_L5P_5
D18	IO_L5N_5
D19	IO_L6P_5
D20	IO_L6N_5
D21	IO_L7N_5
D22	IO_L7P_5
D23	IO_L8N_CC_LC_5
D24	IO_L8P_CC_LC_5
D25	IO_L8N_VREF_5
D26	IO_L17P_5
D27	IO_L17N_5
D28	IO_L18P_5
D29	IO_L18N_5
D30	IO_L19P_5
D31	IO_L19N_5
D32	IO_L20N_VREF_5
D33	IO_L21P_5
D34	IO_L21N_5
D35	IO_L22P_5
D36	IO_L22N_VREF_5
D37	IO_L23N_VREF_5
D38	IO_L24P_CC_LC_5
D39	IO_L24N_CC_LC_5
D40	IO_L19P_CC_LC_5
D41	IO_L19N_CC_LC_5
D42	IO_L10P_5
D43	IO_L10N_5
D44	IO_L11P_5
D45	IO_L11N_5
D46	IO_L12P_5
D47	IO_L12N_VREF_10
D48	IO_L13P_5
D49	IO_L13N_5
D50	IO_L14P_5
D51	IO_L14N_5
D52	IO_L15P_5
D53	IO_L15N_5
D54	IO_L16P_5
D55	IO_L16N_5
D56	IO_L25P_CC_LC_5
D57	IO_L25N_CC_LC_5
D58	IO_L28N_5
D59	IO_L27P_5
D60	IO_L27N_5
D61	IO_L28P_5
D62	IO_L28N_VREF_5
D63	IO_L29N_5
D64	IO_L30P_5
D65	IO_L30N_5
D66	IO_L31P_5
D67	IO_L31N_5
D68	IO_L32P_5
D69	IO_L32N_5

B6	IO_L1P_6
A6	IO_L1N_6
D07-	IO_L2P_6
D07+	IO_L2N_6
C18	IO_L3P_6
C19	IO_L3N_6
D16	IO_L4N_VREF_6
D17	IO_L5P_6
D18	IO_L5N_6
D19	IO_L6P_6
D20	IO_L6N_6
D21	IO_L7N_6
D22	IO_L7P_6
D23	IO_L8N_CC_LC_6
D24	IO_L8P_CC_LC_6
D25	IO_L8N_VREF_6
D26	IO_L17P_6
D27	IO_L17N_6
D28	IO_L18P_6
D29	IO_L18N_6
D30	IO_L19P_6
D31	IO_L19N_6
D32	IO_L20N_VREF_6
D33	IO_L21P_6
D34	IO_L21N_6
D35	IO_L22P_6
D36	IO_L22N_VREF_6
D37	IO_L23N_VREF_6
D38	IO_L24P_CC_LC_6
D39	IO_L24N_CC_LC_6
D40	IO_L19P_CC_LC_6
D41	IO_L19N_CC_LC_6
D42	IO_L10P_6
D43	IO_L10N_6
D44	IO_L11P_6
D45	IO_L11N_6
D46	IO_L12P_6
D47	IO_L12N_VREF_6
D48	IO_L13P_6
D49	IO_L13N_6
D50	IO_L14P_6
D51	IO_L14N_6
D52	IO_L15P_6
D53	IO_L15N_6
D54	IO_L16P_6
D55	IO_L16N_6
D56	IO_L25P_CC_LC_6
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D62	IO_L28N_VREF_6
D63	IO_L29N_6
D64	IO_L30P_6
D65	IO_L30N_6
D66	IO_L31P_6
D67	IO_L31N_6
D68	IO_L32P_6
D69	IO_L32N_6




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PROJECT NAME:	<b>Big3Gig Evaluation Board</b>	PAGE TITLE	ADC08x3000 + Virtex 4
DESIGNED:	Craig Klem	DATE:	29 - Mar - 2007
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USB D- and D+ lines should be controlled impedance lines, as described in the Cypress document [high\\_speed\\_usb\\_pcb\\_layout\\_recommendations\\_9.pdf](#)

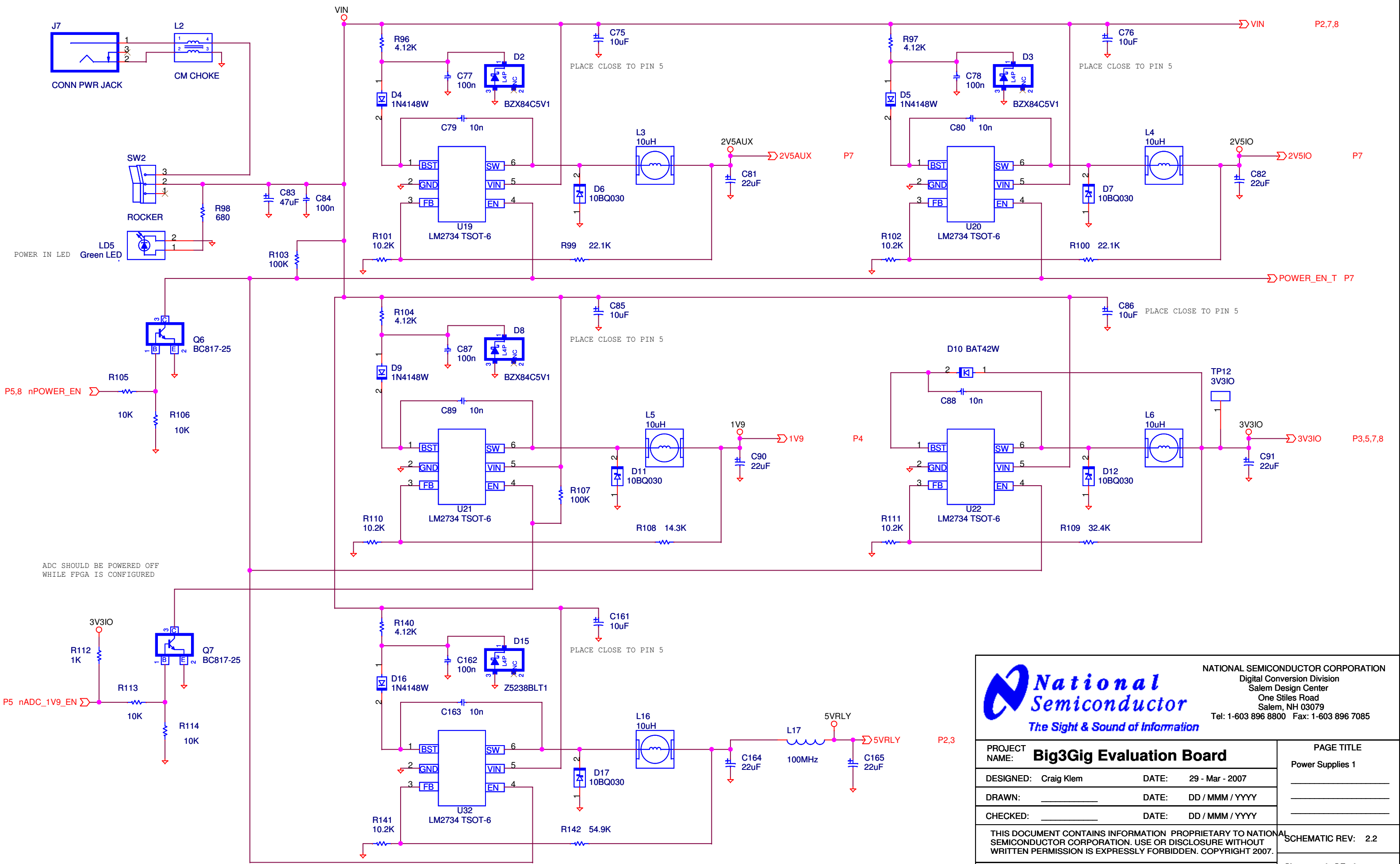
Each unrouted FPGA pad should have a via connecting it to the bottom layer of the board. This will allow access to IO pins of the FPGA for development purposes.



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nPOWER\_EN = 1 - SWITCH REGS SHUTDOWN (STANDBY)  
nPOWER\_EN = 0 - SWITCH REGS ARE ON

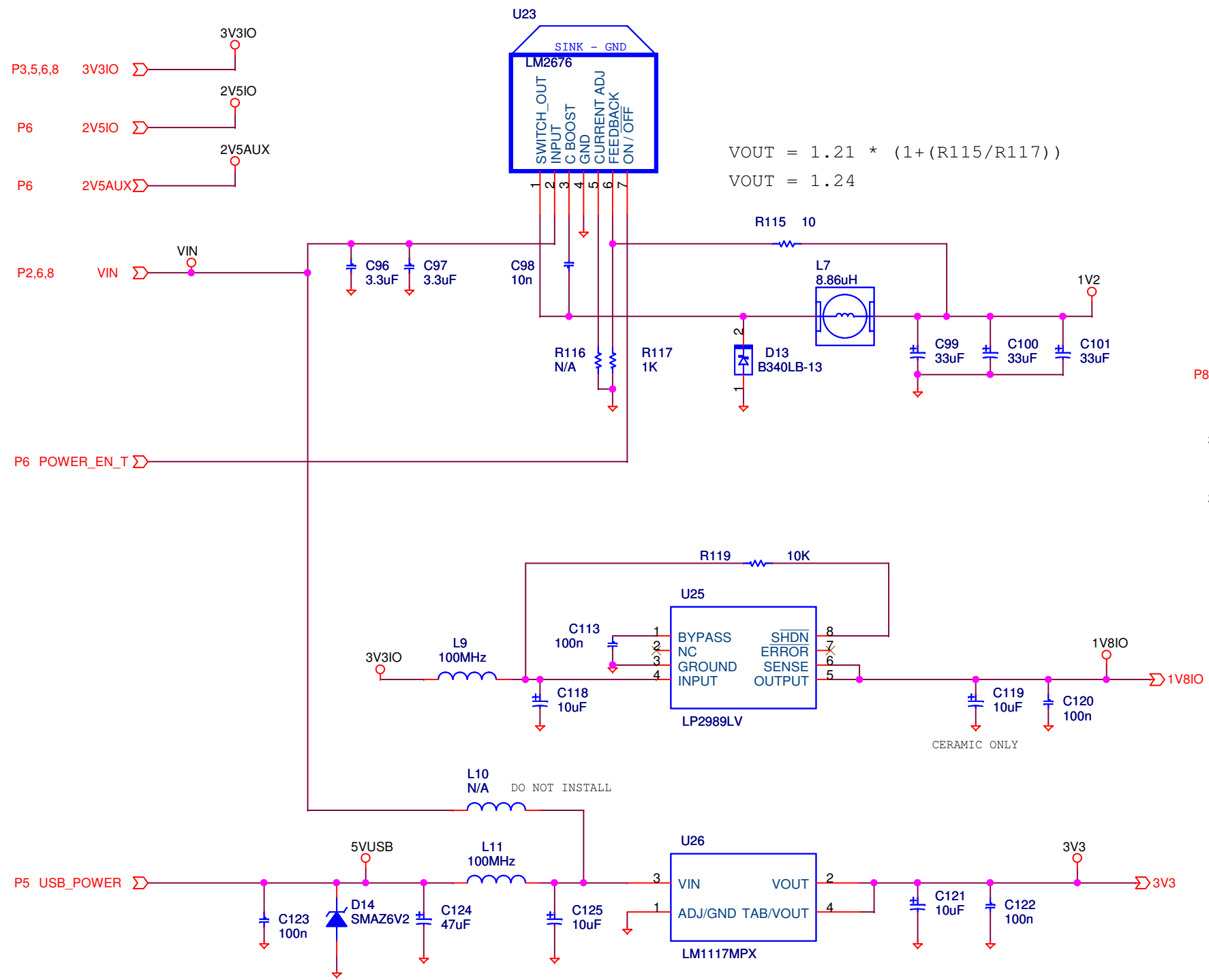


ADC SHOULD BE POWERED OFF WHILE FPGA IS CONFIGURED

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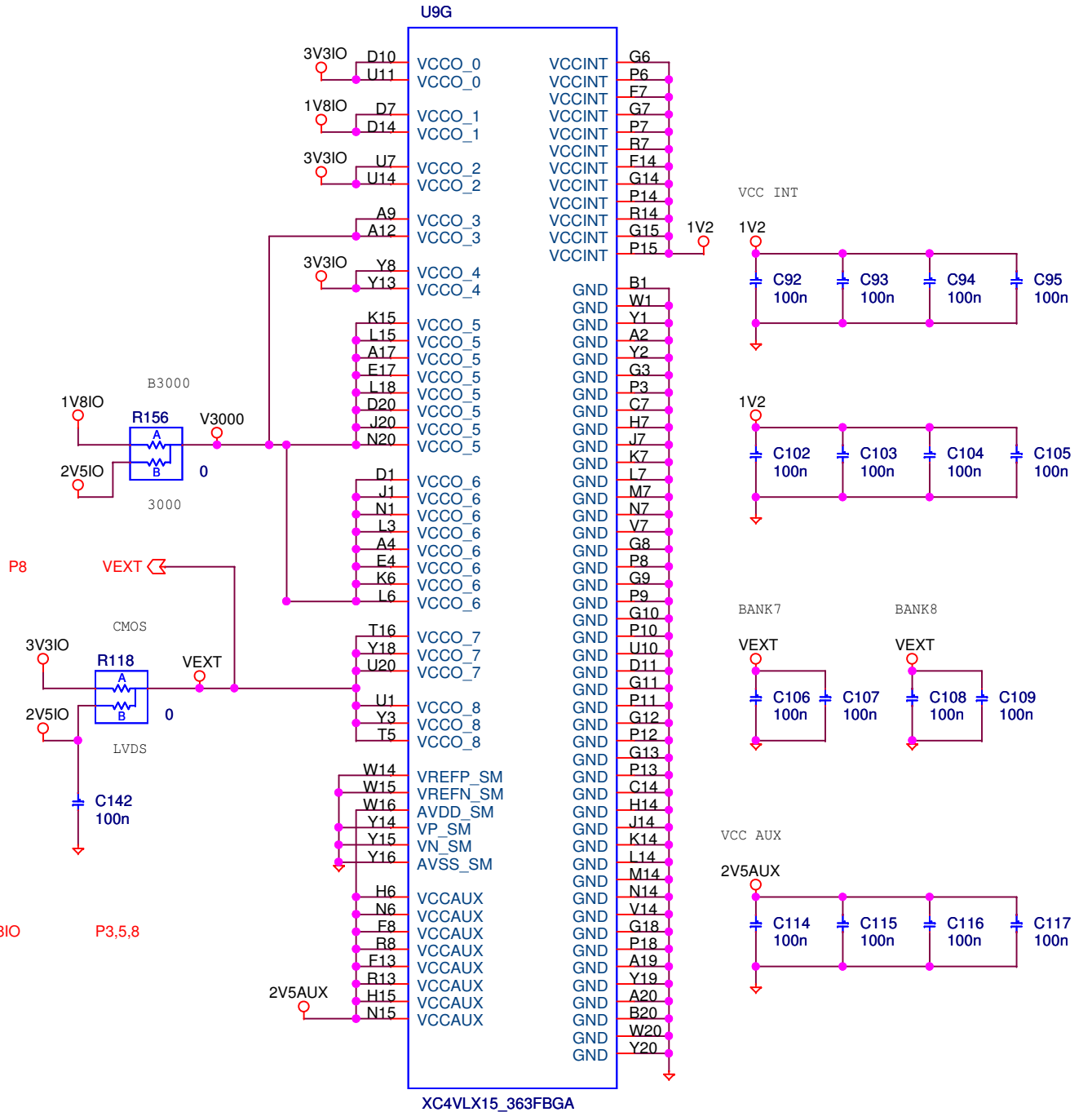
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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE Power Supplies 1
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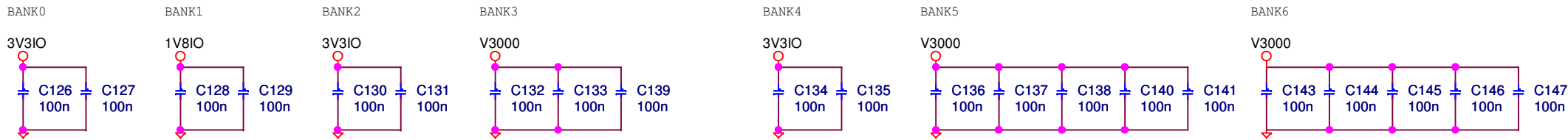


$$V_{OUT} = 1.21 * (1 + (R_{115}/R_{117}))$$

$$V_{OUT} = 1.24$$



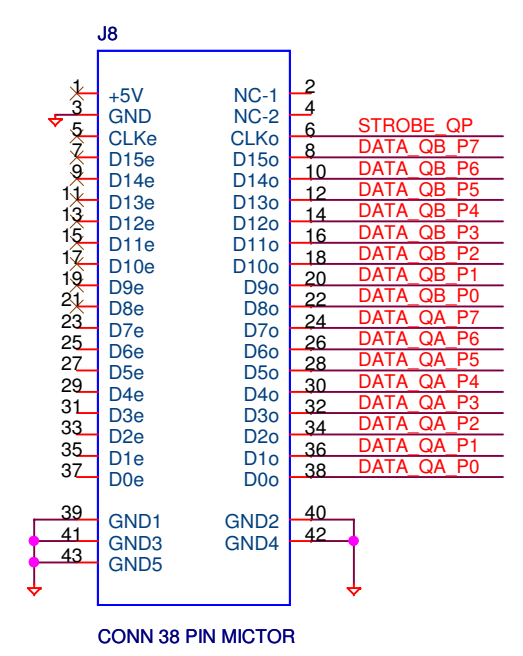
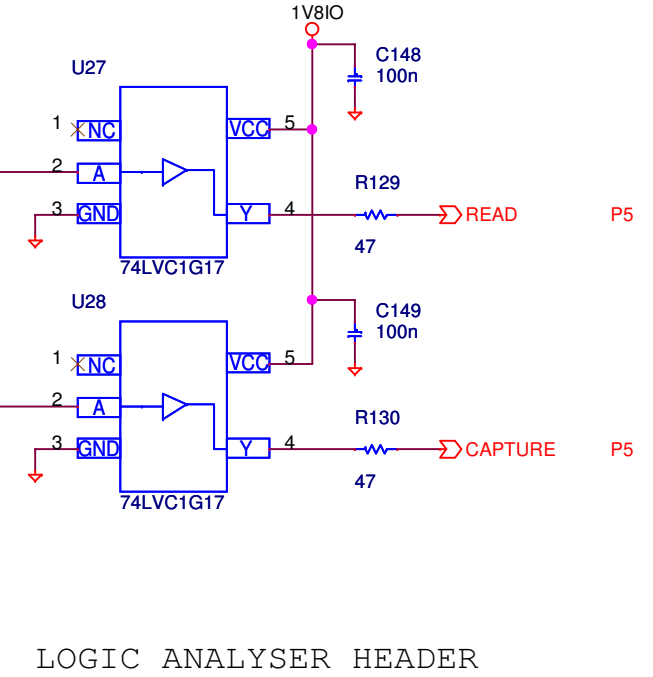
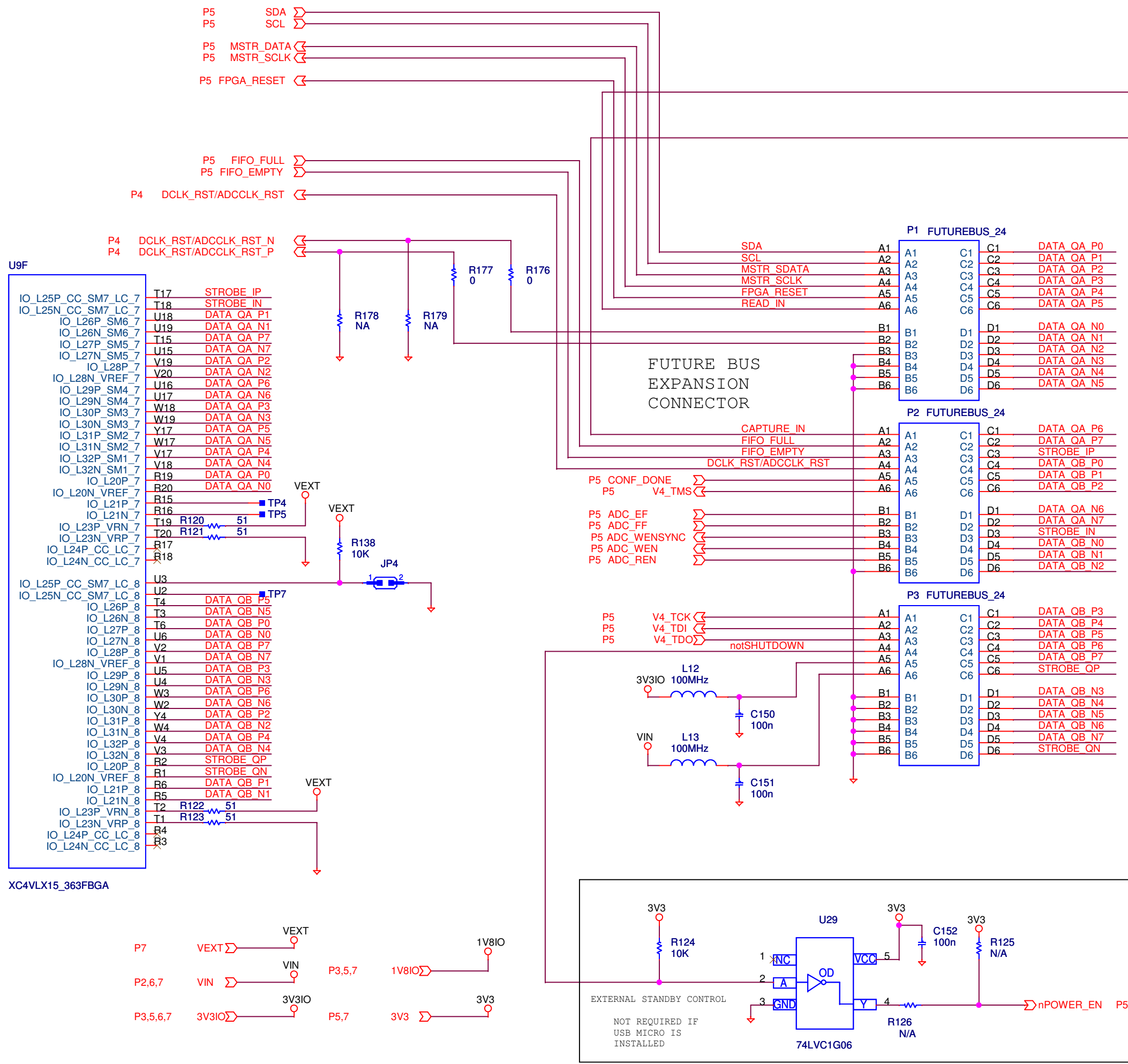
0402 FPGA Decouplers




  
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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE
DESIGNED: Craig Klem		Power Supplies 2
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PROJECT NAME: <b>Big3Gig Evaluation Board</b>		PAGE TITLE: Expansion Port
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