LMK05318 Registers

1 LMK05318 Register Map Generation Using TICS Pro

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user's clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register settings can be exported (in hex format) to enable host programming of the LMK05318 on start-up. The TICS Pro setup file can also be provided to TI for device configuration review, optimization, and to enable factory pre-programmed sample devices.

See the *LMK05318 Ultra-Low Jitter Clock Synchronizer and Jitter Cleaner* data sheet for the General Register Programming Sequence and EEPROM Programming Flow.

Table 1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 1 should be considered as reserved locations and the register contents should not be modified.

Table 1. Device Registers

Address	Acronym	Register Name	Section
0x0	R0	VNDRID_BY1	Go
0x1	R1	VNDRID_BY0	Go
0x2	R2	PRODID	Go
0x3	R3	REVID	Go
0x4	R4	PARTID_BY3	Go
0x5	R5	PARTID_BY2	Go
0x6	R6	PARTID_BY1	Go
0x7	R7	PARTID_BY0	Go
0x8	R8	PINMODE_SW	Go
0xA	R10	SLAVEADR	Go
0xB	R11	EEREV	Go
0xC	R12	DEV_CTL	Go
0xD	R13	INT_LIVE0	Go
0xE	R14	INT_LIVE1	Go
0xF	R15	INT_MASK0	Go
0x10	R16	INT_MASK1	Go
0x11	R17	INT_FLAG_POL0	Go
0x12	R18	INT_FLAG_POL1	Go
0x13	R19	INT_FLAG0	Go
0x14	R20	INT_FLAG1	Go
0x15	R21	INTCTL	Go
0x16	R22	STAT_POL	Go
0x17	R23	MUTELVL1	Go
0x18	R24	MUTELVL2	Go
0x19	R25	OUT_MUTE	Go
0x1D	R29	DPLL_MUTE	Go
0x24	R36	GPIO_OUT	Go
0x27	R39	SPARE_NVMBASE2_BY2	Go

Table 1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x2A	R42	XO_CLKCTL1	Go
0x2B	R43	XO_CLKCTL2	Go
0x2C	R44	XO_CONFIG	Go
0x2D	R45	REF_CLKCTL1	Go
0x2E	R46	REF_CLKCTL2	Go
0x2F	R47	PLL_CLK_CFG	Go
0x30	R48	STAT0_SEL	Go
0x31	R49	STAT1_SEL	Go
0x32	R50	PWDN	Go
0x33	R51	OUTCTL_0	Go
0x34	R52	OUTCTL_1	Go
0x35	R53	OUTDIV_0_1	Go
0x36	R54	OUTCTL_2	Go
0x37	R55	OUTCTL_3	Go
0x38	R56	OUTDIV_2_3	Go
0x39	R57	OUTCTL_4	Go
0x3A	R58	OUTDIV_4	Go
0x3B	R59	OUTCTL_5	Go
0x3C	R60	OUTDIV_5	Go
0x3D	R61	OUTCTL_6	Go
0x3E	R62	OUTDIV_6	Go
0x3F	R63	OUTCTL_7	Go
0x40	R64	OUTDIV_7_STG2_BY2	Go
0x41	R65	OUTDIV_7_STG2_BY1	Go
0x42	R66	OUTDIV_7_STG2_BY0	Go
0x43	R67	OUTDIV_7	Go
0x44	R68	PREDRIVER	Go
0x46	R70	OUTSYNCCTL	Go
0x47	R71	OUTSYNCEN	Go
0x4A	R74	PLL1_CTRL0	Go
0x4F	R79	PLL1_CALCTRL0	Go
0x50	R80	BAW_LOCKDET_PPM_MAX_BY1	Go
0x51	R81	BAW_LOCKDET_PPM_MAX_BY0	Go
0x52	R82	BAW_LOCKDET_CNTSTRT_BY3	Go
0x53	R83	BAW_LOCKDET_CNTSTRT_BY2	Go
0x54	R84	BAW_LOCKDET_CNTSTRT_BY1	Go
0x55	R85	BAW_LOCKDET_CNTSTRT_BY0	Go
0x56	R86	BAW_LOCKDET_VCO_CNTSTRT_BY3	Go
0x57	R87	BAW_LOCKDET_VCO_CNTSTRT_BY2	Go
0x58	R88	BAW_LOCKDET_VCO_CNTSTRT_BY1	Go
0x59	R89	BAW_LOCKDET_VCO_CNTSTRT_BY0	Go
0x5A	R90	BAW_UNLOCKDET_PPM_MAX_BY1	Go
0x5B	R91	BAW_UNLOCKDET_PPM_MAX_BY0	Go
0x5C	R92	BAW_UNLOCKDET_CNTSTRT_BY3	Go
0x5D	R93	BAW_UNLOCKDET_CNTSTRT_BY2	Go
0x5E	R94	BAW_UNLOCKDET_CNTSTRT_BY1	Go
0x5F	R95	BAW_UNLOCKDET_CNTSTRT_BY0	Go

Table 1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x60	R96	BAW_UNLOCKDET_VCO_CNTSTRT_BY3	Go
0x61	R97	BAW_UNLOCKDET_VCO_CNTSTRT_BY2	Go
0x62	R98	BAW_UNLOCKDET_VCO_CNTSTRT_BY1	Go
0x63	R99	BAW_UNLOCKDET_VCO_CNTSTRT_BY0	Go
0x64	R100	PLL2_CTRL0	Go
0x65	R101	PLL2_CTRL1	Go
0x66	R102	PLL2_CTRL2	Go
0x68	R104	PLL2_CTRL4	Go
0x69	R105	PLL2_CALCTRL0	Go
0x6C	R108	PLL1_NDIV_BY1	Go
0x6D	R109	PLL1_NDIV_BY0	Go
0x6E	R110	PLL1_NUM_BY4	Go
0x6F	R111	PLL1_NUM_BY3	Go
0x70	R112	PLL1_NUM_BY2	Go
0x71	R113	PLL1_NUM_BY1	Go
0x72	R114	PLL1_NUM_BY0	Go
0x73	R115	PLL1_MASHCTRL	Go
0x74	R116	PLL1_MODE	Go
0x7B	R123	PLL1_NUM_STAT_BY4	Go
0x7C	R124	PLL1_NUM_STAT_BY3	Go
0x7D	R125	PLL1_NUM_STAT_BY2	Go
0x7E	R126	PLL1_NUM_STAT_BY1	Go
0x7F	R127	PLL1_NUM_STAT_BY0	Go
0x81	R129	PLL1_LF_R2	Go
0x83	R131	PLL1_LF_R3	Go
0x84	R132	PLL1_LF_R4	Go
0x86	R134	PLL2_NDIV_BY1	Go
0x87	R135	PLL2_NDIV_BY0	Go
0x88	R136	PLL2_NUM_BY2	Go
0x89	R137	PLL2_NUM_BY1	Go
0x8A	R138	PLL2_NUM_BY0	Go
0x8B	R139	PLL2_MASHCTRL	Go
0x8C	R140	PLL2_LF_R2	Go
0x8E	R142	PLL2_LF_R3	Go
0x8F	R143	PLL2_LF_R4	Go
0x90	R144	PLL2_LF_C3C4	Go
0x91	R145	XO_OFFSET_SW_TIMER	Go
0x9C	R156	NVMCNT	Go
0x9D	R157	NVMCTL	Go
0x9F	R159	MEMADR_BY1	Go
0xA0	R160	MEMADR_BY0	Go
0xA1	R161	NVMDAT	Go
0xA2	R162	RAMDAT	Go
0xA4	R164	NVMUNLK	Go
0xB4	R180	DPLL_TUNING_FREE_RUN_BY4	Go
0xB5	R181	DPLL_TUNING_FREE_RUN_BY3	Go
0xB6	R182	DPLL_TUNING_FREE_RUN_BY2	Go

Table 1. Device Registers (continued)

Address	Acronym	Register Name	Section
0xB7	R183	DPLL_TUNING_FREE_RUN_BY1	Go
0xB8	R184	DPLL_TUNING_FREE_RUN_BY0	Go
0xB9	R185	DPLL_REF_HISTCTL	Go
0xBA	R186	DPLL_REF_HISTCNT	Go
0xBB	R187	DPLL_REF_HISTDLY_BY3	Go
0xBC	R188	DPLL_REF_HISTDLY_BY2	Go
0xBD	R189	DPLL_REF_HISTDLY_BY1	Go
0xBE	R190	DPLL_REF_HISTDLY_BY0	Go
0xC0	R192	REF01_DETAMP	Go
0xC1	R193	REF0_DETEN	Go
0xC2	R194	REF1_DETEN	Go
0xC3	R195	REF0_MISSCLK_DIV_BY2	Go
0xC4	R196	REF0_MISSCLK_DIV_BY1	Go
0xC5	R197	REF0_MISSCLK_DIV_BY0	Go
0xC6	R198	REF1_MISSCLK_DIV_BY2	Go
0xC7	R199	REF1_MISSCLK_DIV_BY1	Go
0xC8	R200	REF1_MISSCLK_DIV_BY0	Go
0xC9	R201	REF_MISSCLK_CTL	Go
0xCA	R202	REF0_EARLY_CLK_DIV_BY2	Go
0xCB	R203	REF0_EARLY_CLK_DIV_BY1	Go
0xCC	R204	REF0_EARLY_CLK_DIV_BY0	Go
0xCD	R205	REF1_EARLY_CLK_DIV_BY2	Go
0xCE	R206	REF1_EARLY_CLK_DIV_BY1	Go
0xCF	R207	REF1_EARLY_CLK_DIV_BY0	Go
0xD0	R208	REF0_PPM_MIN_BY1	Go
0xD1	R209	REF0_PPM_MIN_BY0	Go
0xD2	R210	REF0_PPM_MAX_BY1	Go
0xD3	R211	REF0_PPM_MAX_BY0	Go
0xD4	R212	REF1_PPM_MIN_BY1	Go
0xD5	R213	REF1_PPM_MIN_BY0	Go
0xD6	R214	REF1_PPM_MAX_BY1	Go
0xD7	R215	REF1_PPM_MAX_BY0	Go
0xD9	R217	REF0_CNTSTRT_BY3	Go
0xDA	R218	REF0_CNTSTRT_BY2	Go
0xDB	R219	REF0_CNTSTRT_BY1	Go
0xDC	R220	REF0_CNTSTRT_BY0	Go
0xDD	R221	REF0_HOLD_CNTSTRT_BY3	Go
0xDE	R222	REF0_HOLD_CNTSTRT_BY2	Go
0xDF	R223	REF0_HOLD_CNTSTRT_BY1	Go
0xE0	R224	REF0_HOLD_CNTSTRT_BY0	Go
0xE1	R225	REF1_CNTSTRT_BY3	Go
0xE2	R226	REF1_CNTSTRT_BY2	Go
0xE3	R227	REF1_CNTSTRT_BY1	Go
0xE4	R228	REF1_CNTSTRT_BY0	Go
0xE5	R229	REF1_HOLD_CNTSTRT_BY3	Go
0xE6	R230	REF1_HOLD_CNTSTRT_BY2	Go
0xE7	R231	REF1_HOLD_CNTSTRT_BY1	Go

Table 1. Device Registers (continued)

Address	Acronym	Register Name	Section
0xE8	R232	REF1_HOLD_CNTSTRT_BY0	Go
0xE9	R233	REF0_VLDTMR	Go
0xEA	R234	REF1_VLDTMR	Go
0xEB	R235	REF0_PH_VALID_CNT_BY3	Go
0xEC	R236	REF0_PH_VALID_CNT_BY2	Go
0xED	R237	REF0_PH_VALID_CNT_BY1	Go
0xEE	R238	REF0_PH_VALID_CNT_BY0	Go
0xEF	R239	REF1_PH_VALID_CNT_BY3	Go
0xF0	R240	REF1_PH_VALID_CNT_BY2	Go
0xF1	R241	REF1_PH_VALID_CNT_BY1	Go
0xF2	R242	REF1_PH_VALID_CNT_BY0	Go
0xF3	R243	REF0_PH_VALID_THR	Go
0xF4	R244	REF1_PH_VALID_THR	Go
0xF9	R249	DPLL_REF01_PRTY	Go
0xFB	R251	DPLL_REF_SWMODE	Go
0xFC	R252	DPLL_GEN_CTL	Go
0xFD	R253	DPLL_SWITCHOVER_TMR_EXP	Go
0xFE	R254	DPLL_SWITCHOVER_TMR_MANT_BY1	Go
0xFF	R255	DPLL_SWITCHOVER_TMR_MANT_BY0	Go
0x100	R256	DPLL_REF0_RDIV_BY1	Go
0x101	R257	DPLL_REF0_RDIV_BY0	Go
0x102	R258	DPLL_REF1_RDIV_BY1	Go
0x103	R259	DPLL_REF1_RDIV_BY0	Go
0x104	R260	DPLL_REF_TDC_CTL	Go
0x105	R261	DPLL_REF_DLY_GEN	Go
0x106	R262	DPLL_REF_CYCSLIP_OFFSET_BY4	Go
0x107	R263	DPLL_REF_CYCSLIP_OFFSET_BY3	Go
0x108	R264	DPLL_REF_CYCSLIP_OFFSET_BY2	Go
0x109	R265	DPLL_REF_CYCSLIP_OFFSET_BY1	Go
0x10A	R266	DPLL_REF_CYCSLIP_OFFSET_BY0	Go
0x10B	R267	DPLL_REF_LOOPCTL	Go
0x10C	R268	DPLL_REF_LOOPCTL_CHG	Go
0x10D	R269	DPLL_REF_DECIMATION	Go
0x10E	R270	DPLL_REF_FILTSCALAR_BY1	Go
0x10F	R271	DPLL_REF_FILTSCALAR_BY0	Go
0x110	R272	DPLL_REF_FILTGAIN	Go
0x111	R273	DPLL_REF_FILTGAIN_FL1	Go
0x112	R274	DPLL_REF_FILTGAIN_FL2	Go
0x113	R275	DPLL_REF_LOOPGAIN	Go
0x114	R276	DPLL_REF_LOOPGAIN_FL1	Go
0x115	R277	DPLL_REF_LOOPGAIN_FL2	Go
0x116	R278	DPLL_REF_LPF0GAIN	Go
0x117	R279	DPLL_REF_LPF0GAIN_FL1	Go
0x118	R280	DPLL_REF_LPF0GAIN_FL2	Go
0x119	R281	DPLL_REF_LPF1GAIN	Go
0x11A	R282	DPLL_REF_LPF1GAIN_FL1	Go
0x11B	R283	DPLL_REF_LPF1GAIN_FL2	Go

Table 1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x11C	R284	DPLL_REF_LPF0GAIN2_FL	Go
0x11D	R285	DPLL_REF_LPF1GAIN2_FL	Go
0x11E	R286	DPLL_REF_TMR_FL1_BY1	Go
0x11F	R287	DPLL_REF_TMR_FL1_BY0	Go
0x120	R288	DPLL_REF_TMR_FL2_BY1	Go
0x121	R289	DPLL_REF_TMR_FL2_BY0	Go
0x122	R290	DPLL_REF_TMR_LCK_BY1	Go
0x123	R291	DPLL_REF_TMR_LCK_BY0	Go
0x124	R292	DPLL_REF_PHC_LPF	Go
0x125	R293	DPLL_REF_PHC_CTRL	Go
0x126	R294	DPLL_REF_PHC_TIMER_BY1	Go
0x127	R295	DPLL_REF_PHC_TIMER_BY0	Go
0x128	R296	DPLL_REF_QUANT	Go
0x129	R297	DPLL_REF_QUANT_FL1	Go
0x12A	R298	DPLL_REF_QUANT_FL2	Go
0x12C	R300	DPLL_PL_LPF_GAIN	Go
0x12D	R301	DPLL_PL_THRESH	Go
0x12E	R302	DPLL_PL_UNLK_THRESH	Go
0x130	R304	DPLL_REF_FB_PREDIV	Go
0x131	R305	DPLL_REF_FB_DIV_BY3	Go
0x132	R306	DPLL_REF_FB_DIV_BY2	Go
0x133	R307	DPLL_REF_FB_DIV_BY1	Go
0x134	R308	DPLL_REF_FB_DIV_BY0	Go
0x135	R309	DPLL_REF_NUM_BY4	Go
0x136	R310	DPLL_REF_NUM_BY3	Go
0x137	R311	DPLL_REF_NUM_BY2	Go
0x138	R312	DPLL_REF_NUM_BY1	Go
0x139	R313	DPLL_REF_NUM_BY0	Go
0x13A	R314	DPLL_REF_DEN_BY4	Go
0x13B	R315	DPLL_REF_DEN_BY3	Go
0x13C	R316	DPLL_REF_DEN_BY2	Go
0x13D	R317	DPLL_REF_DEN_BY1	Go
0x13E	R318	DPLL_REF_DEN_BY0	Go
0x13F	R319	DPLL_REF_MASHCTL	Go
0x140	R320	DPLL_REF_LOCKDET_PPM_MAX_BY1	Go
0x141	R321	DPLL_REF_LOCKDET_PPM_MAX_BY0	Go
0x142	R322	DPLL_REF_LOCKDET_CNTSTRT_BY3	Go
0x143	R323	DPLL_REF_LOCKDET_CNTSTRT_BY2	Go
0x144	R324	DPLL_REF_LOCKDET_CNTSTRT_BY1	Go
0x145	R325	DPLL_REF_LOCKDET_CNTSTRT_BY0	Go
0x146	R326	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY3	Go
0x147	R327	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY2	Go
0x148	R328	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY1	Go
0x149	R329	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY0	Go
0x14A	R330	DPLL_REF_UNLOCKDET_PPM_MAX_BY1	Go
0x14B	R331	DPLL_REF_UNLOCKDET_PPM_MAX_BY0	Go
0x14C	R332	DPLL_REF_UNLOCKDET_CNTSTRT_BY3	Go

Table 1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x14D	R333	DPLL_REF_UNLOCKDET_CNTSTRT_BY2	Go
0x14E	R334	DPLL_REF_UNLOCKDET_CNTSTRT_BY1	Go
0x14F	R335	DPLL_REF_UNLOCKDET_CNTSTRT_BY0	Go
0x150	R336	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY3	Go
0x151	R337	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY2	Go
0x152	R338	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY1	Go
0x153	R339	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY0	Go
0x154	R340	DPLL_REF_SYNC_PH_OFFSET_BY5	Go
0x155	R341	DPLL_REF_SYNC_PH_OFFSET_BY4	Go
0x156	R342	DPLL_REF_SYNC_PH_OFFSET_BY3	Go
0x157	R343	DPLL_REF_SYNC_PH_OFFSET_BY2	Go
0x158	R344	DPLL_REF_SYNC_PH_OFFSET_BY1	Go
0x159	R345	DPLL_REF_SYNC_PH_OFFSET_BY0	Go
0x15A	R346	DPLL_FDEV_CTL	Go
0x15B	R347	DPLL_FDEV_BY4	Go
0x15C	R348	DPLL_FDEV_BY3	Go
0x15D	R349	DPLL_FDEV_BY2	Go
0x15E	R350	DPLL_FDEV_BY1	Go
0x15F	R351	DPLL_FDEV_BY0	Go
0x160	R352	DPLL_FDEV_REG_CTL	Go
0x165	R357	PLL1_CALSTAT1	Go
0x16F	R367	PLL2_CALSTAT1	Go
0x19B	R411	REFVALSTAT	Go

Complex bit access types are encoded to fit into small table cells. Table 2 shows the codes that are used for access types in this section.

Table 2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0C	W 0C	Write 0 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

2 R0 Register (Address = 0x0) [reset = 0x10]

R0 is shown in Table 3.

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Table 3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VNDRID_15:8	R	0x10	Bits 15:8 of VNDRID

3 R1 Register (Address = 0x1) [reset = 0xB]

R1 is shown in Table 4.

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Table 4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VNDRID	R	0xB	Vendor Identification Number Unique 16-bit number assigned to chip vendors.

4 R2 Register (Address = 0x2) [reset = 0x35]

R2 is shown in Table 5.

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Table 5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODID	R	0x35	Product Identification Number Unique 8-bit number used to identify the LMK05318.

5 R3 Register (Address = 0x3) [reset = 0x0]

R3 is shown in Table 6.

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Table 6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REVID	R	0x0	Device Revision Number Used to identify the mask-set revision.

6 R4 Register (Address = 0x4) [reset = 0x0]

R4 is shown in Table 7.

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Table 7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID_31:24	R	0x0	Bits 31:24 of PRTID

7 R5 Register (Address = 0x5) [reset = 0x0]

R5 is shown in Table 8.

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Table 8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID_23:16	R	0x0	Bits 23:16 of PRTID

8 R6 Register (Address = 0x6) [reset = 0x0]

R6 is shown in Table 9.

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Table 9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID_15:8	R	0x0	Bits 15:8 of PRTID

9 R7 Register (Address = 0x7) [reset = 0x0]

R7 is shown in Table 10.

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Table 10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID	R	0x0	Part Identification Number 32-bit number used to serialize individual LMK05318 devices. Factory programmed. Cannot be modified by the user.

10 R8 Register (Address = 0x8) [reset = 0x0]

R8 is shown in Table 11.

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Table 11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	HW_SW_CTRL_MODE	R	0x0	HW_SW_CTRL Pin Configuration Reflects the values sampled on the HW_SW_CTRL pin during device power-on reset (POR). 0x0 = EEPROM/Soft Pin Mode 0x1 = ROM/Hard Pin Mode
5-3	RESERVED	R	0x0	Reserved
2-0	OP_MODE	R	0x0	Operating Mode The OP_MODE fields reflects the device operating mode as determined by the input levels on the HW_SW_CTRL, STATUS0, and STATUS1 pins respectively during POR. 0x0 = Reserved 0x1 = Reserved 0x2 = EEPROM + I2C, Soft pin mode 0x3 = ROM + I2C, Hard pin mode 0x4 = EEPROM + SPI, Soft pin mode 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

11 R10 Register (Address = 0xA) [reset = 0xC8]

R10 is shown in Table 12.

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Table 12. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVEADR_GPIO1_SW	R	0x64	7-bit I2C Slave Address The five MSBs (base address bits) are programmable in EEPROM, which is 11001b for generic factory devices. The two LSBs are determined by control input pin levels. When the HW_SW_CTRL pin is 1, the two LSBs are fixed to 00b. When the HW_SW_CTRL pin is 0, the 2 LSBs are determined by the GPIO1 input state (3-level) during POR.
0	RESERVED	R	0x0	Reserved

12 R11 Register (Address = 0xB) [reset = 0x0]

R11 is shown in Table 13.

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Table 13. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEREV	R	0x0	EEPROM Image Revision ID EEPROM Image Revision ID is automatically retrieved from EEPROM and reflected in the EEREV register after a reset or after a NVM commit operation. This register is user programmable. EEPROM register 11 can be written through the SRAM.

13 R12 Register (Address = 0xC) [reset = 0x39]

R12 is shown in Table 14.

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Table 14. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET_SW	R/W	0x0	Software Reset ALL functions Writing a 1 will cause the device to return to its power-up state apart from the registers and the configuration controller. The configuration controller is excluded to prevent a re-transfer of EEPROM data to on-chip registers.
6	SYNC_SW	R/W	0x0	Output Synchronization (SYNC) Assert bit
5	SYNC_AUTO_DPLL	R/W	0x1	Enable Automatic Output SYNC after DPLL lock
4	SYNC_AUTO_APLL	R/W	0x1	Enable Automatic Output SYNC after PLL lock
3	SYNC_MUTE	R/W	0x1	Determines if the output drivers are muted during a SYNC event 0x0 = Do not mute any outputs during SYNC 0x1 = Mute all outputs during SYNC
2	RESERVED	R	0x0	Reserved
1-0	RESERVED	R/W	0x1	Reserved

14 R13 Register (Address = 0xD) [reset = 0x0]

R13 is shown in Table 15.

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Table 15. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO	R	0x0	Loss of source freq detection XO
3	LOL_PLL2	R	0x0	Loss of Lock APLL2
2	LOL_PLL1	R	0x0	Loss of Lock APLL1
1	RESERVED	R	0x0	Reserved
0	LOS_XO	R	0x0	Loss of source XO

15 R14 Register (Address = 0xE) [reset = 0x0]

R14 is shown in Table 16.

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Table 16. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL	R	0x0	Loss of phase lock DPLL
6	LOFL_DPLL	R	0x0	Loss of frequency lock DPLL
5	HIST	R	0x0	Tuning word history update DPLL
4	HLDOVR	R	0x0	Holdover event DPLL
3	REFSWITCH	R	0x0	Reference switchover DPLL
2	LOR_MISSCLK	R	0x0	Loss of active reference missing clock DPLL
1	LOR_FREQ	R	0x0	Loss of active reference frequency DPLL
0	LOR_AMP	R	0x0	Loss of active reference amplitude DPLL

16 R15 Register (Address = 0xF) [reset = 0x0]

R15 is shown in Table 17.

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Table 17. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_MASK	R/W	0x0	Mask Loss of Source Freq Det XO When set to 1, interrupt output is not triggered.
3	LOL_PLL2_MASK	R/W	0x0	Mask Loss of Lock APLL2 When set to 1, interrupt output is not triggered.
2	LOL_PLL1_MASK	R/W	0x0	Mask Loss of Lock APLL1 When set to 1, interrupt output is not triggered.
1	RESERVED	R	0x0	Reserved
0	LOS_XO_MASK	R/W	0x0	Mask Loss of source XO When set to 1, interrupt output is not triggered.

17 R16 Register (Address = 0x10) [reset = 0x0]

R16 is shown in Table 18.

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Table 18. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_MASK	R/W	0x0	Mask Loss of Phase Lock DPLL When set to 1, interrupt output is not triggered.
6	LOFL_DPLL_MASK	R/W	0x0	Mask Loss of Freq Lock DPLL When set to 1, interrupt output is not triggered.
5	HIST_MASK	R/W	0x0	Mask Tuning word history update DPLL When set to 1, interrupt output is not triggered.
4	HLDOVR_MASK	R/W	0x0	Mask Holdover event DPLL When set to 1, interrupt output is not triggered.
3	REFSWITCH_MASK	R/W	0x0	Mask Reference switchover DPLL When set to 1, interrupt output is not triggered.
2	LOR_MISSCLK_MASK	R/W	0x0	Mask Loss of active reference missing clk DPLL When set to 1, interrupt output is not triggered.
1	LOR_FREQ_MASK	R/W	0x0	Mask Loss of active reference freq DPLL When set to 1, interrupt output is not triggered.
0	LOR_AMP_MASK	R/W	0x0	Mask Loss of active reference amplitude DPLL When set to 1, interrupt output is not triggered.

18 R17 Register (Address = 0x11) [reset = 0x0]

R17 is shown in Table 19.

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Table 19. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity
3	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity
2	LOL_PLL1_POL	R/W	0x0	LOL_PLL1 Flag Polarity
1	RESERVED	R	0x0	Reserved
0	LOS_XO_POL	R/W	0x0	LOS_XO Flag Polarity

19 R18 Register (Address = 0x12) [reset = 0x0]

R18 is shown in Table 20.

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Table 20. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_POL	R/W	0x0	LOPL_DPLL Flag Polarity
6	LOFL_DPLL_POL	R/W	0x0	LOFL_DPLL Flag Polarity
5	HIST_POL	R/W	0x0	HIST Flag Polarity

Table 20. R18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR_POL	R/W	0x0	HLDOVR Flag Polarity
3	REFSWITCH_POL	R/W	0x0	REFSWITCH Flag Polarity
2	LOR_MISSCLK_POL	R/W	0x0	LOR_MISSCLK Flag Polarity
1	LOR_FREQ_POL	R/W	0x0	LOR_FREQ Flag Polarity
0	LOR_AMP_POL	R/W	0x0	LOR_AMP Flag Polarity

20 R19 Register (Address = 0x13) [reset = 0x0]

R19 is shown in Table 21.

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Table 21. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_INTR	R/W0C	0x0	LOL_FDET_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_FDET_XO interrupt source. The bit is cleared by writing a 0.
3	LOL_PLL2_INTR	R/W0C	0x0	LOL_PLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL2 interrupt source. The bit is cleared by writing a 0.
2	LOL_PLL1_INTR	R/W0C	0x0	LOL_PLL1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL1 interrupt source.The bit is cleared by writing a 0.
1	RESERVED	R	0x0	Reserved
0	LOS_XO_INTR	R/W0C	0x0	LOS_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOS_XO interrupt source. The bit is cleared by writing a 0.

21 R20 Register (Address = 0x14) [reset = 0x0]

R20 is shown in Table 22.

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Table 22. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_INTR	R/W0C	0x0	LOPL_DPLL Interrupt Bt is set when an edge of the correct polarity is detected on the LOPL_DPLL interrupt source. The bit is cleared by writing a 0.
6	LOFL_DPLL_INTR	R/W0C	0x0	LOFL_DPLL Interrupt Bit is set when an edge of the correct polarity is detected on the LOFL_DPLL interrupt source. The bit is cleared by writing a 0.
5	HIST_INTR	R/W0C	0x0	HIST Interrupt Bit is set when an edge of the correct polarity is detected on the HIST interrupt source. The bit is cleared by writing a 0.
4	HLDOVR_INTR	R/W0C	0x0	HLDOVR Interrupt Bit is set when an edge of the correct polarity is detected on the HLDOVR interrupt source. The bit is cleared by writing a 0.

Table 22. R20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH_INTR	R/W0C	0x0	REFSWITCH Interrupt Bit is set when an edge of the correct polarity is detected on the REFSWITCH interrupt source. The bit is cleared by writing a 0.
2	LOR_MISSCLK_INTR	R/W0C	0x0	LOR_MISSCLK Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_MISSCLK interrupt source. The bit is cleared by writing a 0.
1	LOR_FREQ_INTR	R/W0C	0x0	LOR_FREQ Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_FREQ interrupt source. The bit is cleared by writing a 0.
0	LOR_AMP_INTR	R/W0C	0x0	LOR_AMP Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_AMP interrupt source. The bit is cleared by writing a 0.

22 R21 Register (Address = 0x15) [reset = 0x0]

R21 is shown in Table 23.

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Table 23. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	INT_AND_OR	R/W	0x0	Interrupt Logical AND or OR Combination 0x0 = OR: Any un-masked interrupt flags can generate an interrupt. 0x1 = AND: All un-masked interrupt flags must be active in order to generate an interrupt.
0	INT_EN	R/W	0x0	Interrupt Enable

23 R22 Register (Address = 0x16) [reset = 0x0]

R22 is shown in Table 24.

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Table 24. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	STAT1_POL	R/W	0x0	STATUS1 Output Polarity Defines the polarity of information presented on the STATUS1 output. If STAT1_POL is set to 1 then STATUS1 is active high, if STAT1_POL is 0then STATUS1 is active low.
0	STAT0_POL	R/W	0x0	STATUS0 Output Polarity Defines the polarity of information presented on the STATUS0 output. If STAT0_POL is set to 1 then STATUS0 is active high, if STAT0_POL is 0then STATUS0 is active low.

24 R23 Register (Address = 0x17) [reset = 0x0]

R23 is shown in Table 25.

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Table 25. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH3_MUTE_LVL	R/W	0x0	Output 3 Mute Level See CH0_MUTE_LVL for description and bit settings.
5-4	CH2_MUTE_LVL	R/W	0x0	Output 2 Mute Level See CH0_MUTE_LVL for description and bit settings.
3-2	CH1_MUTE_LVL	R/W	0x0	Output 1 Mute Level See CH0_MUTE_LVL for description and bit settings.
1-0	CH0_MUTE_LVL	R/W	0x0	Output 0 Mute Level Determines the configuration of the Output Driver during mute. 0x0 = Bypass Mute (Normal Operation) 0x1 = For DIFF or HCSL mute to differential Vocm. For LVCMOS, P is Bypass Mute and N is Mute Low. 0x2 = For DIFF or HCSL mute to differntial High. For LVCMOS, P is Mute Low and N is Bypass Mute. 0x3 = For DIFF or HCSL mute to differential Low. For LVCMOS, P is Mute Low and N is Mute Low.

25 R24 Register (Address = 0x18) [reset = 0x0]

R24 is shown in Table 26.

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Table 26. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH7_MUTE_LVL	R/W	0x0	Output 7 Mute Level See CH0_MUTE_LVL for description and bit settings.
5-4	CH6_MUTE_LVL	R/W	0x0	Output 6 Mute Level See CH0_MUTE_LVL for description and bit settings.
3-2	CH5_MUTE_LVL	R/W	0x0	Output 5 Mute Level See CH0_MUTE_LVL for description and bit settings.
1-0	CH4_MUTE_LVL	R/W	0x0	Output 4 Mute Level See CH0_MUTE_LVL for description and bit settings.

26 R25 Register (Address = 0x19) [reset = 0xFF]

R25 is shown in Table 27.

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Table 27. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_MUTE	R/W	0x1	Output 7 Mute Control
6	CH6_MUTE	R/W	0x1	Output 6 Mute Control
5	CH5_MUTE	R/W	0x1	Output 5 Mute Control
4	CH4_MUTE	R/W	0x1	Output 4 Mute Control
3	CH3_MUTE	R/W	0x1	Output 3 Mute Control
2	CH2_MUTE	R/W	0x1	Output 2 Mute Control
1	CH1_MUTE	R/W	0x1	Output 1 Mute Control
0	CH0_MUTE	R/W	0x1	Output 0 Mute Control

27 R29 Register (Address = 0x1D) [reset = 0x13]

R29 is shown in Table 28.

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Table 28. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	MUTE_APLL2_LOCK	R/W	0x1	APLL2 mute enabled during PLL lock
3	RESERVED	R	0x0	Reserved
2	MUTE_DPLL_PHLOCK	R/W	0x0	DPLL mute enabled during phase lock
1	MUTE_DPLL_FLLOCK	R/W	0x1	DPLL mute enabled during DPLL lock
0	MUTE_APLL1_LOCK	R/W	0x1	APLL1 mute enabled during PLL lock

28 R36 Register (Address = 0x24) [reset = 0x0]

R36 is shown in Table 29.

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Table 29. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	GPIO_STAT1_OUT	R/W	0x0	STAT1 Driver Type Output 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver
0	GPIO_STAT0_OUT	R/W	0x0	STAT0 Driver Type Output 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver

29 R39 Register (Address = 0x27) [reset = 0x0]

R39 is shown in Table 30.

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Table 30. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-2	RESERVED	R/W	0x0	Reserved
1	GPIO2_OUT	R/W	0x0	GPIO2 Driver Type GPIO2 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver
0	RESERVED	R/W	0x0	Reserved

30 R42 Register (Address = 0x2A) [reset = 0x1]

R42 is shown in Table 31.

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Table 31. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	OSCIN_DBLR_EN	R/W	0x0	Enable OSCIn doubler
3	XO_FDET_BYP	R/W	0x0	XO Frequency Detector Bypass If bypassed, the XO detector status is ignored and the XO input is considered valid by the PLL control state machines
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

31 R43 Register (Address = 0x2B) [reset = 0x82]

R43 is shown in Table 32.

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Table 32. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x1	Reserved
6-3	XO_TYPE	R/W	0x0	XO Input Type 0x0 = DC-Differential (external termination) 0x1 = AC-Differential (external termination) 0x3 = AC-Differential (internal termination 100-Ω) 0x4 = HCSL (internal termination 50-Ω) 0x8 = CMOS 0xC = Single-ended (internal termination 50-Ω)
2-0	RESERVED	R/W	0x2	Reserved

32 R44 Register (Address = 0x2C) [reset = 0x1]

R44 is shown in Table 33.

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Table 33. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	OSCIN_RDIV	R/W	0x1	Oscillator Input Divider

33 R45 Register (Address = 0x2D) [reset = 0x3]

R45 is shown in Table 34.

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Table 34. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved

Table 34. R45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SECREF_CMOS_SLEW	R/W	0x0	SECREF input buffer slew rate 0x0 = Select Amplitude Detector Mode 0x1 = Select CMOS Amplitude Detector Mode
2	PRIREF_CMOS_SLEW	R/W	0x0	PRIREF input buffer slew rate 0x0 = Select Amplitude Detector Mode 0x1 = Select CMOS Amplitude Detector Mode
1-0	RESERVED	R/W	0x3	Reserved

34 R46 Register (Address = 0x2E) [reset = 0x0]

R46 is shown in Table 35.

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Table 35. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SECREF_TYPE	R/W	0x0	SECREF Input Type See PRIREF_TYPE for input type bit settings.
3-0	PRIREF_TYPE	R/W	0x0	PRIREF Input Type 0x0 = DC-Differential (external termination) 0x1 = AC-Differential (external termination) 0x3 = AC-Differential (internal termination 100-Ω) 0x4 = HCSL (internal termination 50-Ω) 0x8 = CMOS 0xC = Single-ended (internal termination 50-Ω)

35 R47 Register (Address = 0x2F) [reset = 0x0]

R47 is shown in Table 36.

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Table 36. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL2_RCLK_SEL	R/W	0x0	PLL2 Reference clock selection 0x0 = VCO1 - Cascaded Mode 0x1 = XO
6-4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2-0	RESERVED	R/W	0x0	Reserved

36 R48 Register (Address = 0x30) [reset = 0xA]

R48 is shown in Table 37.

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Table 37. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 37. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	STAT0_SEL	R/W	0xA	STATUS0 Indicator Signal Select The output pin state of 1 indicates the status condition is true. 0x00 = XO Input Loss of Signal (LOS) 0x01 = Low 0x02 = Reserved 0x03 = PLL1 Digital Lock Detect (DLD) 0x04 = PLL1 VCO Calibration Active 0x05 = PLL1 N Divider, div-by-2 0x06 = PLL2 Digital Lock Detect (DLD) 0x07 = PLL2 VCO Calibration Active 0x08 = PLL2 N Divider, div-by-2 0x09 = EEPROM Active 0x0A = Interrupt (INTR) 0x0B = Reserved 0x0C = DPLL Phase Lock Detected ($\overline{\text{LOPL}}$) 0x0D = PRIREF Monitor Divider Output, div-by-2 0x0E = SECREF Monitor Divider Output, div-by-2 0x0F = PLL2 R Divider, div-by-2 0x10 = Reserved 0x11 = PRIREF Amplitude Monitor Fault 0x12 = SECREF Amplitude Monitor Fault 0x13 = Reserved 0x14 = Reserved 0x15 = PRIREF Frequency Monitor Fault 0x16 = SECREF Frequency Monitor Fault 0x17 = Reserved 0x18 = Reserved 0x19 = PRIREF Missing or Early Pulse Monitor Fault 0x1A = SECREF Missing or Early Pulse Monitor Fault 0x1B = Reserved 0x1C = Reserved 0x1D = PRIREF Validation Timer Active 0x1E = SECREF Validation Timer Active 0x1F = Reserved 0x20 = Reserved 0x21 = Reserved 0x22 = Reserved 0x23 = Reserved 0x24 = Reserved 0x25 = PRIREF Phase Validation Monitor Fault 0x26 = SECREF Phase Validation Monitor Fault 0x27 = Reserved 0x28 = Reserved 0x29 = PLL1 Lock Detected ($\overline{\text{LOL}}$) 0x2A = PLL2 Lock Detected ($\overline{\text{LOL}}$) 0x2B = Reserved 0x2C = Reserved 0x2D = Reserved 0x2E = Reserved 0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved

Table 37. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = Reserved 0x3C = Reserved 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = DPLL R Divider, div-by-2 0x41 = DPLL FB Divider, div-by-2 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = DPLL PRIREF Selected 0x47 = DPLL SECREF Selected 0x48 = Reserved 0x49 = Reserved 0x4A = DPLL Holdover Active 0x4B = DPLL Reference Switchover Event 0x4C = Reserved 0x4D = DPLL Tuning History Update 0x4E = DPLL Fast Lock Active 0x4F = Reserved 0x50 = DPLL Loss of Lock (LOFL)

37 R49 Register (Address = 0x31) [reset = 0xA]

R49 is shown in Table 38.

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Table 38. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	STAT1_SEL	R/W	0xA	STATUS1 Indicator Signal Select See STAT0_SEL for status signal and bit settings.

38 R50 Register (Address = 0x32) [reset = 0x0]

R50 is shown in Table 39.

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Table 39. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_FDEV_EN	R/W	0x0	Enable DCO Frequency When enabled, a rising edge on these pins will update the DCO frequency accordingly.
6	RESERVED	R	0x0	Reserved

Table 39. R50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CH7_PD	R/W	0x0	Channel 7 Powerdown When CH7_PD is 1 the regulator that supplies the divider and drivers for OUT7 will be disabled.
4	CH6_PD	R/W	0x0	Channel 6 Powerdown When CH6_PD is 1 the regulator that supplies the divider and drivers for OUT6 will be disabled.
3	CH5_PD	R/W	0x0	Channel 5 Powerdown When CH5_PD is 1 the regulator that supplies the divider and drivers for OUT5 will be disabled.
2	CH4_PD	R/W	0x0	Channel 4 Powerdown When CH4_PD is 1 the regulator that supplies the divider and drivers for OUT4 will be disabled.
1	CH2_3_PD	R/W	0x0	Channel 2 and 3 Powerdown When CH2_3_PD is 1 the regulator that supplies the divider and drivers for OUT2 and OUT3 will be disabled.
0	CH0_1_PD	R/W	0x0	Channel 0 and 1 Powerdown When CH0_1_PD is 1 the regulator that supplies the divider and drivers for OUT0 and OUT1 will be disabled.

39 R51 Register (Address = 0x33) [reset = 0x18]

R51 is shown in Table 40.

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Table 40. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH0_1_MUX	R/W	0x0	Channel 0 and 1 Output Mux Selects frequency source for OUT0 and OUT1. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5-0	OUT0_FMT	R/W	0x18	OUT0 Clock Format Values not displayed below are reserved. 0x00 = Disabled 0x10 = AC-LVDS 0x14 = AC-CML 0x18 = AC-LVPECL 0x2C = HCSL (external termination 50-Ω) 0x2D = HCSL (internal termination 50-Ω)

40 R52 Register (Address = 0x34) [reset = 0x18]

R52 is shown in Table 41.

Return to Summary Table.

Table 41. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved

Table 41. R52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	OUT1_FMT	R/W	0x18	OUT1 Clock Format See OUT0_FMT for bit settings.

41 R53 Register (Address = 0x35) [reset = 0x7]

R53 is shown in Table 42.

Return to Summary Table.

Table 42. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT0_1_DIV	R/W	0x7	Channel 0 and Channel 1 Output Divider This is an 8-bit divider. The valid values for OUT0_1_DIV range from 1 to 255. Output Divider (ODOUT01) = OUT0_1_DIV + 1 Note: 0x00 is disabled.

42 R54 Register (Address = 0x36) [reset = 0x18]

R54 is shown in Table 43.

Return to Summary Table.

Table 43. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH2_3_MUX	R/W	0x0	Channel 2 and 3 Output Mux Selects frequency source for OUT2 and OUT3. See CH0_1_MUX for bit settings.
5-0	OUT2_FMT	R/W	0x18	OUT2 Clock Format See OUT0_FMT for bit settings.

43 R55 Register (Address = 0x37) [reset = 0x18]

R55 is shown in Table 44.

Return to Summary Table.

Table 44. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	OUT3_FMT	R/W	0x18	OUT3 Clock Format See OUT0_FMT for bit settings.

44 R56 Register (Address = 0x38) [reset = 0x7]

R56 is shown in Table 45.

Return to Summary Table.

Table 45. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT2_3_DIV	R/W	0x7	Channel 2 and Channel 3 Output Divider See OUT0_1_DIV for description and bit settings.

45 R57 Register (Address = 0x39) [reset = 0x18]

R57 is shown in Table 46.

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Table 46. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH4_MUX	R/W	0x0	Channel 4 Output Mux Selects frequency source for OUT4. See CH0_1_MUX for bit settings.
5-0	OUT4_FMT	R/W	0x18	OUT4 Clock Format Values not desplayed below are reserved. 0x00 = Disabled 0x10 = AC-LVDS 0x14 = AC-CML 0x18 = AC-LVPECL 0x2C = HCSL (external termination 50-Ω) 0x2D = HCSL (internal termination 50-Ω) 0x30 = LVCMOS(HiZ/HiZ) 0x32 = LVCMOS(HiZ/-) 0x33 = LVCMOS(HiZ/+) 0x35 = LVCMOS(low/low) 0x38 = LVCMOS(-/HiZ) 0x3A = LVCMOS(-/-) 0x3B = LVCMOS(-/+) 0x3C = LVCMOS(+/HiZ) 0x3E = LVCMOS(+/-) 0x3F = LVCMOS(+/+)

46 R58 Register (Address = 0x3A) [reset = 0x7]

R58 is shown in Table 47.

Return to Summary Table.

Table 47. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT4_DIV	R/W	0x7	Channel 4 Output Divider See OUT0_1_DIV for description and bit settings.

47 R59 Register (Address = 0x3B) [reset = 0x18]

R59 is shown in Table 48.

Return to Summary Table.

Table 48. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH5_MUX	R/W	0x0	Channel 5 Output Mux Selects frequency source for OUT5. See CH0_1_MUX for bit settings.
5-0	OUT5_FMT	R/W	0x18	OUT5 Clock Format See OUT4_FMT for bit settings.

48 R60 Register (Address = 0x3C) [reset = 0x7]

R60 is shown in Table 49.

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Table 49. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT5_DIV	R/W	0x7	Channel 5 Output Divider See OUT0_1_DIV for description and bit settings.

49 R61 Register (Address = 0x3D) [reset = 0x18]

R61 is shown in Table 50.

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Table 50. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH6_MUX	R/W	0x0	Channel 6 Output Mux Selects frequency source for OUT6. See CH0_1_MUX for bit settings.
5-0	OUT6_FMT	R/W	0x18	OUT6 Clock Format See OUT4_FMT for bit settings.

50 R62 Register (Address = 0x3E) [reset = 0x7]

R62 is shown in Table 51.

Return to Summary Table.

Table 51. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT6_DIV	R/W	0x7	Channel 6 Output Divider See OUT0_1_DIV for description and bit settings.

51 R63 Register (Address = 0x3F) [reset = 0x18]

R63 is shown in Table 52.

Return to Summary Table.

Table 52. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH7_MUX	R/W	0x0	Channel 7 Output Mux Selects frequency source for OUT7. See CH0_1_MUX for bit settings.
5-0	OUT7_FMT	R/W	0x18	OUT7 Clock Format See OUT4_FMT for bit settings.

52 R64 Register (Address = 0x40) [reset = 0x0]

R64 is shown in Table 53.

Return to Summary Table.

Table 53. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_STG2_DIV_23:16	R/W	0x0	Bits 23:16 of OUT7_STG2_DIV

53 R65 Register (Address = 0x41) [reset = 0x0]

R65 is shown in Table 54.

Return to Summary Table.

Table 54. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_STG2_DIV_15:8	R/W	0x0	Bits 15:8 of OUT7_STG2_DIV

54 R66 Register (Address = 0x42) [reset = 0x0]

R66 is shown in Table 55.

Return to Summary Table.

Table 55. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_STG2_DIV	R/W	0x0	Channel 7 Stage Two Output Divider OD2 = OUT7_STG2_DIV + 1 If OD2 > 1, then ODout7 must be ≥ 6. Total output 7 divide value = OD2 * ODout7.

55 R67 Register (Address = 0x43) [reset = 0x7]

R67 is shown in Table 56.

Return to Summary Table.

Table 56. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_DIV	R/W	0x7	Channel 7 Output Divider This is an 8-bit divider. The valid values for OUT7_DIV range from 1 to 255. ODOUT7 = OUT7_DIV + 1. If OD2 > 1, then total output 7 divide value = OD2 * ODout7 where OD2 is OUT7 secondary output divider value. Note: 0x00 is disabled.

56 R68 Register (Address = 0x44) [reset = 0xFF]

R68 is shown in Table 57.

Return to Summary Table.

Table 57. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0xF	Reserved
3-0	PLL1_CP_BAW	R/W	0xF	APLL1 Charge Pump Current Gain PLL1_CP_BAW ranges from 0 to 15. Gain = PLL1_CP_BAW x 100 µA.

57 R70 Register (Address = 0x46) [reset = 0x0]

R70 is shown in Table 58.

Return to Summary Table.

Table 58. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2	PLL2_P2_SYNC_EN	R/W	0x0	Enable PLL2 P2 divider channel synchronizatrion
1	PLL2_P1_SYNC_EN	R/W	0x0	Enable PLL2 P1 divider channel synchronizatrion
0	PLL1_P1_SYNC_EN	R/W	0x0	Enable PLL1 P1 divider channel synchronizatrion

58 R71 Register (Address = 0x47) [reset = 0x0]

R71 is shown in Table 59.

Return to Summary Table.

Table 59. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	CH7_SYNC_EN	R/W	0x0	Enable Channel 7 output synchronization
4	CH6_SYNC_EN	R/W	0x0	Enable Channel 6 output synchronization
3	CH5_SYNC_EN	R/W	0x0	Enable Channel 5 output synchronization
2	CH4_SYNC_EN	R/W	0x0	Enable Channel 4 output synchronization
1	CH2_3_SYNC_EN	R/W	0x0	Enable Channels 2 and 3 output synchronization
0	CH0_1_SYNC_EN	R/W	0x0	Enable Channels 0 and 1 output synchronization

59 R74 Register (Address = 0x4A) [reset = 0x0]

R74 is shown in Table 60.

Return to Summary Table.

Table 60. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved

Table 60. R74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL1_PDN	R/W	0x0	PLL1 Power down The PLL1_PDN bit determines whether PLL1 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL1 Enabled 0x1 = PLL1 Disabled

60 R79 Register (Address = 0x4F) [reset = 0x11]

R79 is shown in Table 61.

Return to Summary Table.

Table 61. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	BAW_LOCKDET_EN	R/W	0x1	BAW Lock Detect Enable
3-0	RESERVED	R/W	0x1	Reserved

61 R80 Register (Address = 0x50) [reset = 0x0]

R80 is shown in Table 62.

Return to Summary Table.

Table 62. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BAW_LOCK	R/W	0x0	BAW Lock Detect Status 0x0 = Unlocked 0x1 = Locked
6-0	BAW_LOCK_DET_1	R/W	0x0	BAW VCO Lock Detection

62 R81 Register (Address = 0x51) [reset = 0x0]

R81 is shown in Table 63.

Return to Summary Table.

Table 63. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_2	R/W	0x0	BAW VCO Lock Detection

63 R82 Register (Address = 0x52) [reset = 0x0]

R82 is shown in Table 64.

Return to Summary Table.

Table 64. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved

Table 64. R82 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	BAW_LOCK_DET_3	R/W	0x0	BAW VCO Lock Detection

64 R83 Register (Address = 0x53) [reset = 0x0]

R83 is shown in Table 65.

Return to Summary Table.

Table 65. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_4	R/W	0x0	BAW VCO Lock Detection

65 R84 Register (Address = 0x54) [reset = 0x0]

R84 is shown in Table 66.

Return to Summary Table.

Table 66. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_5	R/W	0x0	BAW VCO Lock Detection

66 R85 Register (Address = 0x55) [reset = 0x0]

R85 is shown in Table 67.

Return to Summary Table.

Table 67. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_6	R/W	0x0	BAW VCO Lock Detection

67 R86 Register (Address = 0x56) [reset = 0x0]

R86 is shown in Table 68.

Return to Summary Table.

Table 68. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	BAW_LOCK_DET_7	R/W	0x0	BAW VCO Lock Detection

68 R87 Register (Address = 0x57) [reset = 0x0]

R87 is shown in Table 69.

Return to Summary Table.

Table 69. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_8	R/W	0x0	BAW VCO Lock Detection

69 R88 Register (Address = 0x58) [reset = 0x0]

R88 is shown in Table 70.

Return to Summary Table.

Table 70. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_9	R/W	0x0	BAW VCO Lock Detection

70 R89 Register (Address = 0x59) [reset = 0x0]

R89 is shown in Table 71.

Return to Summary Table.

Table 71. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_DET_10	R/W	0x0	BAW VCO Lock Detection

71 R90 Register (Address = 0x5A) [reset = 0x0]

R90 is shown in Table 72.

Return to Summary Table.

Table 72. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	BAW_UNLK_DET_1	R/W	0x0	BAW VCO Unlock Detection

72 R91 Register (Address = 0x5B) [reset = 0x0]

R91 is shown in Table 73.

Return to Summary Table.

Table 73. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_2	R/W	0x0	BAW VCO Unlock Detection

73 R92 Register (Address = 0x5C) [reset = 0x0]

R92 is shown in Table 74.

Return to Summary Table.

Table 74. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	BAW_UNLK_DET_3	R/W	0x0	BAW VCO Unlock Detection

74 R93 Register (Address = 0x5D) [reset = 0x0]

R93 is shown in Table 75.

Return to Summary Table.

Table 75. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_4	R/W	0x0	BAW VCO Unlock Detection

75 R94 Register (Address = 0x5E) [reset = 0x0]

R94 is shown in Table 76.

Return to Summary Table.

Table 76. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_5	R/W	0x0	BAW VCO Unlock Detection

76 R95 Register (Address = 0x5F) [reset = 0x0]

R95 is shown in Table 77.

Return to Summary Table.

Table 77. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_6	R/W	0x0	BAW VCO Unlock Detection

77 R96 Register (Address = 0x60) [reset = 0x0]

R96 is shown in Table 78.

Return to Summary Table.

Table 78. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	BAW_UNLK_DET_7	R/W	0x0	BAW VCO Unlock Detection

78 R97 Register (Address = 0x61) [reset = 0x0]

R97 is shown in Table 79.

Return to Summary Table.

Table 79. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_8	R/W	0x0	BAW VCO Unlock Detection

79 R98 Register (Address = 0x62) [reset = 0x0]

R98 is shown in Table 80.

Return to Summary Table.

Table 80. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_9	R/W	0x0	BAW VCO Unlock Detection

80 R99 Register (Address = 0x63) [reset = 0x0]

R99 is shown in Table 81.

Return to Summary Table.

Table 81. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_DET_10	R/W	0x0	BAW VCO Unlock Detection

81 R100 Register (Address = 0x64) [reset = 0x1]

R100 is shown in Table 82.

Return to Summary Table.

Table 82. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	PLL2_RDIV_SEC	R/W	0x0	APLL2 secondary reference divider in cascaded APLL2 mode Divider value ranges from 1-32. Divider value = PLL2_RDIV_SEC + 1.
2-1	PLL2_RDIV_PRE	R/W	0x0	APLL2 primary reference divider in cascaded APLL2 mode
0	PLL2_PDN	R/W	0x1	PLL2 Power down The PLL2_PDN bit determines whether PLL2 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL2 Enabled 0x1 = PLL2 Disabled

82 R101 Register (Address = 0x65) [reset = 0x2]

R101 is shown in Table 83.

Return to Summary Table.

Table 83. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1-0	PLL2_CP	R/W	0x2	PLL2 Charge Pump Gain 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

83 R102 Register (Address = 0x66) [reset = 0x22]

R102 is shown in Table 84.

Return to Summary Table.

Table 84. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-4	PLL2_P2	R/W	0x2	PLL2 Post-Divider2 Note: A RESET is required after changing Divider values. See PLL2_P1 for bit settings.
3	RESERVED	R	0x0	Reserved
2-0	PLL2_P1	R/W	0x2	PLL2 Post-Divider1 Note: A RESET is required after changing Divider values. 0x0 = Invalid 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = Invalid

84 R104 Register (Address = 0x68) [reset = 0x0]

R104 is shown in Table 85.

Return to Summary Table.

Table 85. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved

Table 85. R104 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PLL2_RBLEED_CP	R/W	0x0	PLL2 Bleed resistor selection (Ω) 0x0 = Open (high impedance) 0x1 = 23713.2 0x2 = 11875.2 0x3 = 7915.62 0x4 = 5843.79 0x5 = 4753.58 0x6 = 3963.08 0x7 = 3393.52 0x8 = 2970.14 0x9 = 2638.54 0xA = 2375.04 0xB = 2158.91 0xC = 1980.99 0xD = 1827.03 0xE = 1696.76 0xF = 1584.26 0x10 = 1486.55 0x11 = 1397.73 0x12 = 1320.66 0x13 = 1249.6 0x14 = 1187.43 0x15 = 1131.17 0x16 = 1077.88 0x17 = 1033.47 0x18 = 991.03 0x19 = 950.53 0x1A = 913.52 0x1B = 879.47 0x1C = 848.38 0x1D = 818.77 0x1E = 792.13 0x1F = 766.96

85 R105 Register (Address = 0x69) [reset = 0x0]

R105 is shown in Table 86.

Return to Summary Table.

Table 86. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3-2	PLL2_CLSDWAIT	R/W	0x0	Closed Loop Wait Period VCO calibration time per step (up to 7 steps). 0x0 = 0.3 ms 0x1 = 3 ms 0x2 = 30 ms 0x3 = 300 ms
1-0	RESERVED	R/W	0x0	Reserved

86 R108 Register (Address = 0x6C) [reset = 0x0]

R108 is shown in Table 87.

Return to Summary Table.

Table 87. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PLL1_NDIV_11:8	R/W	0x0	Bits 11:8 of PLL1_NDIV

87 R109 Register (Address = 0x6D) [reset = 0x64]

R109 is shown in Table 88.

Return to Summary Table.

Table 88. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NDIV	R/W	0x64	PLL1 N Divider

88 R110 Register (Address = 0x6E) [reset = 0x0]

R110 is shown in Table 89.

Return to Summary Table.

Table 89. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_39:32	R/W	0x0	Bits 39:32 of PLL1_NUM

89 R111 Register (Address = 0x6F) [reset = 0x0]

R111 is shown in Table 90.

Return to Summary Table.

Table 90. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_31:24	R/W	0x0	Bits 31:24 of PLL1_NUM

90 R112 Register (Address = 0x70) [reset = 0x0]

R112 is shown in Table 91.

Return to Summary Table.

Table 91. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_23:16	R/W	0x0	Bits 23:16 of PLL1_NUM

91 R113 Register (Address = 0x71) [reset = 0x0]

R113 is shown in Table 92.

Return to Summary Table.

Table 92. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_15:8	R/W	0x0	Bits 15:8 of PLL1_NUM

92 R114 Register (Address = 0x72) [reset = 0x0]

R114 is shown in Table 93.

Return to Summary Table.

Table 93. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM	R/W	0x0	PLL1 Fractional Divider Numerator

93 R115 Register (Address = 0x73) [reset = 0x0]

R115 is shown in Table 94.

Return to Summary Table.

Table 94. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0x0	Reserved
4-3	PLL1_DTHRMODE	R/W	0x0	APLL1 SDM Dither Mode 0x0 = Weak 0x1 = Medium 0x2 = Strong 0x3 = Disabled
2-0	PLL1_ORDER	R/W	0x0	APLL1 SDM Order 0x0 = Integer Mode 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th

94 R116 Register (Address = 0x74) [reset = 0x1]

R116 is shown in Table 95.

Return to Summary Table.

Table 95. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2-1	RESERVED	R/W	0x0	Reserved
0	PLL1_MODE	R/W	0x1	PLL1 operational mode 0x0 = Free-run mode (APLL only) 0x1 = DPLL mode

95 R123 Register (Address = 0x7B) [reset = 0x0]

R123 is shown in Table 96.

Return to Summary Table.

Table 96. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_39:32	R	0x0	Bits 39:32 of PLL1_NUM_STAT

96 R124 Register (Address = 0x7C) [reset = 0x0]

R124 is shown in Table 97.

Return to Summary Table.

Table 97. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_31:24	R	0x0	Bits 31:24 of PLL1_NUM_STAT

97 R125 Register (Address = 0x7D) [reset = 0x0]

R125 is shown in Table 98.

Return to Summary Table.

Table 98. R125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_23:16	R	0x0	Bits 23:16 of PLL1_NUM_STAT

98 R126 Register (Address = 0x7E) [reset = 0x0]

R126 is shown in Table 99.

Return to Summary Table.

Table 99. R126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_15:8	R	0x0	Bits 15:8 of PLL1_NUM_STAT

99 R127 Register (Address = 0x7F) [reset = 0x0]

R127 is shown in Table 100.

Return to Summary Table.

Table 100. R127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT	R	0x0	APLL1 Numerator Status Byte

100 R129 Register (Address = 0x81) [reset = 0x18]

R129 is shown in Table 101.

Return to Summary Table.

Table 101. R129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved

Table 101. R129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PLL1_LF_R2	R/W	0x18	PLL1 Loop Filter R2 (Ω) 0x00 = 0 0x01 = 414 0x02 = 880 0x03 = 1294 0x04 = 1625 0x05 = 2039 0x06 = 2505 0x07 = 2919 0x08 = 3250 0x09 = 3664 0x0A = 4130 0x0B = 4544 0x0C = 4875 0x0D = 5289 0x0E = 5755 0x0F = 6169 0x10 = 6400 0x11 = 6814 0x12 = 7280 0x13 = 7694 0x14 = 8025 0x15 = 8439 0x16 = 8905 0x17 = 9319 0x18 = 9650 0x19 = 10064 0x1A = 10530 0x1B = 10944 0x1C = 11275 0x1D = 11689 0x1E = 12155 0x1F = 12569 0x20 = 12800 0x21 = 13214 0x22 = 13680 0x23 = 14094 0x24 = 14425 0x25 = 14839 0x26 = 15305 0x27 = 15719 0x28 = 16050 0x29 = 16464 0x2A = 16930 0x2B = 17344 0x2C = 17675 0x2D = 18089 0x2E = 18555 0x2F = 18969 0x30 = 19200 0x31 = 19614 0x32 = 20080 0x33 = 20494 0x34 = 20825 0x35 = 21239 0x36 = 21705

Table 101. R129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x37 = 22119 0x38 = 22450 0x39 = 22864 0x3A = 23330 0x3B = 23744 0x3C = 24075 0x3D = 24489 0x3E = 24955 0x3F = 25369

101 R131 Register (Address = 0x83) [reset = 0x18]

R131 is shown in Table 102.

Return to Summary Table.

Table 102. R131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved

Table 102. R131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PLL1_LF_R3	R/W	0x18	PLL1 Loop Filter R3 (Ω) 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6 0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2 0x2F = 4122.7 0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2

Table 102. R131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

102 R132 Register (Address = 0x84) [reset = 0x18]

R132 is shown in Table 103.

Return to Summary Table.

Table 103. R132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PLL1_LF_R4	R/W	0x18	PLL1 Loop Filter R4 See PLL1_LF_R3 for bit settings.

103 R134 Register (Address = 0x86) [reset = 0x0]

R134 is shown in Table 104.

Return to Summary Table.

Table 104. R134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	Bit 8 of PLL2_NDIV

104 R135 Register (Address = 0x87) [reset = 0x64]

R135 is shown in Table 105.

Return to Summary Table.

Table 105. R135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NDIV	R/W	0x64	Bits 7:0 of PLL2 N Divider

105 R136 Register (Address = 0x88) [reset = 0x0]

R136 is shown in Table 106.

Return to Summary Table.

Table 106. R136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_23:16	R/W	0x0	Bits 23:16 of PLL2_NUM

106 R137 Register (Address = 0x89) [reset = 0x0]

R137 is shown in Table 107.

Return to Summary Table.

Table 107. R137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_15:8	R/W	0x0	Bits 15:8 of PLL2_NUM

107 R138 Register (Address = 0x8A) [reset = 0x0]

R138 is shown in Table 108.

Return to Summary Table.

Table 108. R138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM	R/W	0x0	PLL2 Fractional Divider Numerator

108 R139 Register (Address = 0x8B) [reset = 0x0]

R139 is shown in Table 109.

Return to Summary Table.

Table 109. R139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0x0	Reserved
4-3	PLL2_DTHRMODE	R/W	0x0	SDM Dither Mode 0x0 = Weak 0x1 = Medium 0x2 = Strong 0x3 = Disabled
2-0	PLL2_ORDER	R/W	0x0	APLL2 SDM Order 0x0 = Integer Mode 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th

109 R140 Register (Address = 0x8C) [reset = 0x18]

R140 is shown in Table 110.

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Table 110. R140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PLL2_LF_R2	R/W	0x18	PLL2 Loop Filter R2 See PLL1_LF_R2 for bit settings.

110 R142 Register (Address = 0x8E) [reset = 0x18]

R142 is shown in Table 111.

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Table 111. R142 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PLL2_LF_R3	R/W	0x18	PLL2 Loop Filter R3 See PLL1_LF_R3 for bit settings.

111 R143 Register (Address = 0x8F) [reset = 0x18]

R143 is shown in Table 112.

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Table 112. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PLL2_LF_R4	R/W	0x18	PLL2 Loop Filter R4 See PLL1_LF_R3 for bit settings.

112 R144 Register (Address = 0x90) [reset = 0x0]

R144 is shown in Table 113.

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Table 113. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-4	PLL2_LF_C4	R/W	0x0	PLL2 Loop Filter C4 See PLL2_LF_C3 for bit settings.
3	RESERVED	R	0x0	Reserved
2-0	PLL2_LF_C3	R/W	0x0	PLL2 Loop Filter C3 0x0 = 0 pF 0x1 = 40 pF 0x2 = 20 pF 0x3 = 60 pF 0x4 = 10 pF 0x5 = 50 pF 0x6 = 30 pF 0x7 = 70 pF

113 R145 Register (Address = 0x91) [reset = 0x5]

R145 is shown in Table 114.

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Table 114. R145 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-3	RESERVED	R/W	0x0	Reserved
2-0	XO_TIMER	R/W	0x5	XO Input Wait Timer Sets the startup time for the oscillator input. 0x0 = 1.6 ms 0x1 = 3.3 ms 0x2 = 6.6 ms 0x3 = 13.1 ms 0x4 = 26.2 ms 0x5 = 52.4 ms 0x6 = 104.9 ms 0x7 = Reserved

114 R156 Register (Address = 0x9C) [reset = 0x0]

R156 is shown in Table 115.

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Table 115. R156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMCNT	R	0x0	NVM Program Count The NVMCNT increments automatically after every EEPROM Erase/Program Cycle (after a subsequent power-cycle or hard reset). The NVMCNT value is retrieved automatically after reset or after a NVM Commit operation.

115 R157 Register (Address = 0x9D) [reset = 0x0]

R157 is shown in Table 116.

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Table 116. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	RH/W1S	0x0	REG Commit to NVM SRAM Array The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the NVM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
5	NVMCRCERR	R	0x0	NVM CRC Error Indication This bit will read 1 when a CRC Error has been detected reading back from on-chip EEPROM during device initialization, where the NVMLCRC value does not match NVMSCRC. This bit can only be cleared by successful EEPROM programming and power-on/reset cycle, such that the NVMLCRC value matches NVMSCRC.
4	RESERVED	R/W	0x0	Reserved
3	NVMCOMMIT	RH/W1S	0x0	NVM Commit to Registers The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The registers cannot be read while a NVM Commit operation is taking place.

Table 116. R157 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NVMBUSY	R	0x0	NVM Program Busy Indication This bit will read 1 when an EEPROM Erase/Program cycle is active, during which the EEPROM cannot be accessed.
1-0	NVM_ERASE_PROG	RH/W1S	0x0	NVM Erase/Program Start This bit field is used to initiate an internal EEPROM Erase/Programsequence. The sequence is only executed if the immediately preceding register transaction was a write to the NVMUNLK register with the appropriate unlock code. The NVM Erase/Program sequence takes about 230 ms total (115 ms for Erase or Program). 0x0 = NVM Idle 0x3 = Start NVM Erase/Program

116 R159 Register (Address = 0x9F) [reset = 0x0]

R159 is shown in Table 117.

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Table 117. R159 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	MEMADR_12:8	R/W	0x0	Bits 12:8 of MEMADR

117 R160 Register (Address = 0xA0) [reset = 0x0]

R160 is shown in Table 118.

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Table 118. R160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEMADR	R/W	0x0	Memory Address The MEMADR value determines the starting address for access to the on-chip memories. NVMDAT register = NVM EEPROM Data Array (Read only) RAMDAT register = NVM SRAM Data Array (Read/Write) ROMDAT register = ROM Data Array (Read only)

118 R161 Register (Address = 0xA1) [reset = 0x0]

R161 is shown in Table 119.

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Table 119. R161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMDAT	R	0x0	EEPROM Read Data

119 R162 Register (Address = 0xA2) [reset = 0x0]

R162 is shown in Table 120.

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Table 120. R162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAMDAT	R/W	0x0	RAM Read/Write Data

120 R164 Register (Address = 0xA4) [reset = 0x0]

R164 is shown in Table 121.

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Table 121. R164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMUNLK	R/W	0x0	NVM Program Unlock To perform an EEPROM erase and program operation, this register must be written with a value of 0xEA (unlock code) immediately before setting the NVM_ERASE_PROG bits to 0x3 on the next register write.

121 R180 Register (Address = 0xB4) [reset = 0x0]

R180 is shown in Table 122.

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Table 122. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_TUNING_FREE_RUN_37:32	R/W	0x0	Bits 37:32 of DPLL_TUNING_FREE_RUN

122 R181 Register (Address = 0xB5) [reset = 0x0]

R181 is shown in Table 123.

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Table 123. R181 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN_31:24	R/W	0x0	Bits 31:24 of DPLL_TUNING_FREE_RUN

123 R182 Register (Address = 0xB6) [reset = 0x0]

R182 is shown in Table 124.

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Table 124. R182 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN_23:16	R/W	0x0	Bits 23:16 of DPLL_TUNING_FREE_RUN

124 R183 Register (Address = 0xB7) [reset = 0x0]

R183 is shown in Table 125.

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Table 125. R183 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN_15:8	R/W	0x0	Bits 15:8 of DPLL_TUNING_FREE_RUN

125 R184 Register (Address = 0xB8) [reset = 0x0]

R184 is shown in Table 126.

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Table 126. R184 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN	R/W	0x0	DPLL Free-run tuning word

126 R185 Register (Address = 0xB9) [reset = 0x0]

R185 is shown in Table 127.

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Table 127. R185 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DPLL_REF_HIST_INTMD	R/W	0x0	Controls intermediate updates to DPLL REF tuning history Updates only occur during first averaging period Tavg after reset. Programming restriction: DPLL_REF_HIST_INTMD ≤ DPLL_REF_HISTCNT. 0x0 = No intermediate update 0x1 = 1 intermediate update at Tavg/2 0x2 = 2 intermediate update at Tavg/4 and Tavg/2 0x3 = 3 intermediate updates at Tavg/8, Tavg/4 and Tavg/2 0xF = 15 intermediate updates at Tavg/32768, Tavg/16384, ... Tavg/4 and Tavg/2.
3	RESERVED	R	0x0	Reserved
2-1	RESERVED	R/W	0x0	Reserved
0	DPLL_REF_HIST_EN	R/W	0x0	Enables DPLL REF tuning history monitor

127 R186 Register (Address = 0xBA) [reset = 0x0]

R186 is shown in Table 128.

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Table 128. R186 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_HISTCNT	R/W	0x0	DPLL REF Tuning History Timer Valid range is 0 to 30.

128 R187 Register (Address = 0xBB) [reset = 0x0]

R187 is shown in Table 129.

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Table 129. R187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	DPLL_REF_HISTDLY_30:24	R/W	0x0	Bits 30:24 of DPLL_REF_HISTDLY

129 R188 Register (Address = 0xBC) [reset = 0x0]

R188 is shown in Table 130.

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Table 130. R188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_HISTDLY_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_HISTDLY

130 R189 Register (Address = 0xBD) [reset = 0x0]

R189 is shown in Table 131.

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Table 131. R189 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_HISTDLY_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_HISTDLY

131 R190 Register (Address = 0xBE) [reset = 0x0]

R190 is shown in Table 132.

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Table 132. R190 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_HISTDLY	R/W	0x0	DPLL REF Tuning History delay

132 R192 Register (Address = 0xC0) [reset = 0x55]

R192 is shown in Table 133.

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Table 133. R192 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DETECT_MODE_SECREF	R/W	0x1	SECREF Input Energy Detector Mode Control Determines the method for Energy Detection on the SECREF Input. See DETECT_MODE_PRIREF for bit settings.
5-4	DETECT_MODE_PRIREF	R/W	0x1	PRIREF Input Energy Detector Mode Control Determines the method for Energy Detection on the PRIREF Input. 0x0 = Rising Slew Rate Detector 0x1 = Rising and Falling Slew Rate Detector 0x2 = Falling Slew Rate Detector 0x3 = VIH/VIL Level Detector

Table 133. R192 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	SECREF_LVL_SEL	R/W	0x1	SECREF Input Amplitude Detector See PRIREF_LVL_SEL for description and bit settings.
1-0	PRIREF_LVL_SEL	R/W	0x1	PRIREF Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0x0 = Vid is 200 mV Differential or 400 mVpp Single-Ended 0x1 = Vid is 250 mV Differential or 500 mVpp Single-Ended 0x2 = Vid is 300 mV Differential or 600 mVpp Single-Ended 0x3 = Vid is 300 mV Differential or 600 mVpp Single-Ended

133 R193 Register (Address = 0xC1) [reset = 0x0]

R193 is shown in Table 134.

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Table 134. R193 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	PRIREF_EARLY_DET_EN	R/W	0x0	PRIREF Early Clock Detect Enable
4	PRIREF_PH_VALID_EN	R/W	0x0	PRIREF Phase Valid Detect Enable
3	PRIREF_VALTMR_EN	R/W	0x0	PRIREF Validation Timer Enable
2	PRIREF_PPM_EN	R/W	0x0	PRIREF Frequency ppm Detect Enable
1	PRIREF_MISSCLK_EN	R/W	0x0	PRIREF Missing Clock Detect Enable
0	PRIREF_AMPDET_EN	R/W	0x0	PRIREF Amplitude Detect Enable

134 R194 Register (Address = 0xC2) [reset = 0x0]

R194 is shown in Table 135.

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Table 135. R194 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	SECREF_EARLY_DET_EN	R/W	0x0	SECREF Early Clock Detect Enable
4	SECREF_PH_VALID_EN	R/W	0x0	SECREF Phase Valid Detect Enable
3	SECREF_VALTMR_EN	R/W	0x0	SECREF Validation Timer Enable
2	SECREF_PPM_EN	R/W	0x0	SECREF Frequency ppm Detect Enable
1	SECREF_MISSCLK_EN	R/W	0x0	SECREF Missing Clock Detect Enable
0	SECREF_AMPDET_EN	R/W	0x0	SECREF Amplitude Detect Enable

135 R195 Register (Address = 0xC3) [reset = 0x0]

R195 is shown in Table 136.

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Table 136. R195 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PRIREF_MISSCLK_DET_1	R/W	0x0	PRIREF Missing Clock Detection

136 R196 Register (Address = 0xC4) [reset = 0x0]

R196 is shown in Table 137.

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Table 137. R196 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_MISSCLK_DET_2	R/W	0x0	PRIREF Missing Clock Detection

137 R197 Register (Address = 0xC5) [reset = 0x0]

R197 is shown in Table 138.

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Table 138. R197 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_MISSCLK_DET_3	R/W	0x0	PRIREF Missing Clock Detection

138 R198 Register (Address = 0xC6) [reset = 0x0]

R198 is shown in Table 139.

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Table 139. R198 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	SECREF_MISSCLK_DET_1	R/W	0x0	SECREF Missing Clock Detection

139 R199 Register (Address = 0xC7) [reset = 0x0]

R199 is shown in Table 140.

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Table 140. R199 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_MISSCLK_DET_2	R/W	0x0	SECREF Missing Clock Detection

140 R200 Register (Address = 0xC8) [reset = 0x0]

R200 is shown in Table 141.

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Table 141. R200 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_MISSCLK_DET_3	R/W	0x0	SECREF Missing Clock Detection

141 R201 Register (Address = 0xC9) [reset = 0x0]

R201 is shown in Table 142.

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Table 142. R201 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	SECREF_WINDOW_DET	R/W	0x0	SECREF Window Detection
0	PRIREF_WINDOW_DET	R/W	0x0	PRIREF Window Detection

142 R202 Register (Address = 0xCA) [reset = 0x0]

R202 is shown in Table 143.

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Table 143. R202 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PRIREF_EARLYCLK_DET_1	R/W	0x0	PRIREF Early Clock Detection

143 R203 Register (Address = 0xCB) [reset = 0x0]

R203 is shown in Table 144.

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Table 144. R203 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_EARLYCLK_DET_2	R/W	0x0	PRIREF Early Clock Detection

144 R204 Register (Address = 0xCC) [reset = 0x0]

R204 is shown in Table 145.

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Table 145. R204 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_EARLYCLK_DET_3	R/W	0x0	PRIREF Early Clock Detection

145 R205 Register (Address = 0xCD) [reset = 0x0]

R205 is shown in Table 146.

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Table 146. R205 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	SECREF_EARLYCLK_DET_1	R/W	0x0	SECREF Early Clock Detection

146 R206 Register (Address = 0xCE) [reset = 0x0]

R206 is shown in Table 147.

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Table 147. R206 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_EARLYCLK_DET_2	R/W	0x0	SECREF Early Clock Detection

147 R207 Register (Address = 0xCF) [reset = 0x0]

R207 is shown in Table 148.

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Table 148. R207 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_EARLYCLK_DET_3	R/W	0x0	SECREF Early Clock Detection

148 R208 Register (Address = 0xD0) [reset = 0x0]

R208 is shown in Table 149.

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Table 149. R208 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	PRIREF_FREQ_DET_1	R/W	0x0	PRIREF Frequency Detection

149 R209 Register (Address = 0xD1) [reset = 0x0]

R209 is shown in Table 150.

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Table 150. R209 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_2	R/W	0x0	PRIREF Frequency Detection

150 R210 Register (Address = 0xD2) [reset = 0x0]

R210 is shown in Table 151.

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Table 151. R210 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	PRIREF_FREQ_DET_3	R/W	0x0	PRIREF Frequency Detection

151 R211 Register (Address = 0xD3) [reset = 0x0]

R211 is shown in Table 152.

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Table 152. R211 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_4	R/W	0x0	PRIREF Frequency Detection

152 R212 Register (Address = 0xD4) [reset = 0x0]

R212 is shown in Table 153.

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Table 153. R212 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	SECREF_FREQ_DET_1	R/W	0x0	SECREF Frequency Detection

153 R213 Register (Address = 0xD5) [reset = 0x0]

R213 is shown in Table 154.

Return to Summary Table.

Table 154. R213 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_2	R/W	0x0	SECREF Frequency Detection

154 R214 Register (Address = 0xD6) [reset = 0x0]

R214 is shown in Table 155.

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Table 155. R214 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	SECREF_FREQ_DET_3	R/W	0x0	SECREF Frequency Detection

155 R215 Register (Address = 0xD7) [reset = 0x0]

R215 is shown in Table 156.

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Table 156. R215 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_4	R/W	0x0	SECREF Frequency Detection

156 R217 Register (Address = 0xD9) [reset = 0x0]

R217 is shown in Table 157.

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Table 157. R217 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PRIREF_FREQ_DET_5	R/W	0x0	PRIREF Frequency Detection

157 R218 Register (Address = 0xDA) [reset = 0x0]

R218 is shown in Table 158.

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Table 158. R218 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_6	R/W	0x0	PRIREF Frequency Detection

158 R219 Register (Address = 0xDB) [reset = 0x0]

R219 is shown in Table 159.

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Table 159. R219 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_7	R/W	0x0	PRIREF Frequency Detection

159 R220 Register (Address = 0xDC) [reset = 0x0]

R220 is shown in Table 160.

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Table 160. R220 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_8	R/W	0x0	PRIREF Frequency Detection

160 R221 Register (Address = 0xDD) [reset = 0x0]

R221 is shown in Table 161.

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Table 161. R221 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved

Table 161. R221 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	PRIREF_FREQ_DET_9	R/W	0x0	PRIREF Frequency Detection

161 R222 Register (Address = 0xDE) [reset = 0x0]

R222 is shown in Table 162.

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Table 162. R222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_10	R/W	0x0	PRIREF Frequency Detection

162 R223 Register (Address = 0xDF) [reset = 0x0]

R223 is shown in Table 163.

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Table 163. R223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_11	R/W	0x0	PRIREF Frequency Detection

163 R224 Register (Address = 0xE0) [reset = 0x0]

R224 is shown in Table 164.

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Table 164. R224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_FREQ_DET_12	R/W	0x0	PRIREF Frequency Detection

164 R225 Register (Address = 0xE1) [reset = 0x0]

R225 is shown in Table 165.

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Table 165. R225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	SECREF_FREQ_DET_5	R/W	0x0	SECREF Frequency Detection

165 R226 Register (Address = 0xE2) [reset = 0x0]

R226 is shown in Table 166.

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Table 166. R226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_6	R/W	0x0	SECREF Frequency Detection

166 R227 Register (Address = 0xE3) [reset = 0x0]

R227 is shown in Table 167.

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Table 167. R227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_7	R/W	0x0	SECREF Frequency Detection

167 R228 Register (Address = 0xE4) [reset = 0x0]

R228 is shown in Table 168.

Return to Summary Table.

Table 168. R228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_8	R/W	0x0	SECREF Frequency Detection

168 R229 Register (Address = 0xE5) [reset = 0x0]

R229 is shown in Table 169.

Return to Summary Table.

Table 169. R229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	SECREF_FREQ_DET_9	R/W	0x0	SECREF Frequency Detection

169 R230 Register (Address = 0xE6) [reset = 0x0]

R230 is shown in Table 170.

Return to Summary Table.

Table 170. R230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_10	R/W	0x0	SECREF Frequency Detection

170 R231 Register (Address = 0xE7) [reset = 0x0]

R231 is shown in Table 171.

Return to Summary Table.

Table 171. R231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_11	R/W	0x0	SECREF Frequency Detection

171 R232 Register (Address = 0xE8) [reset = 0x0]

R232 is shown in Table 172.

Return to Summary Table.

Table 172. R232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_FREQ_DET_12	R/W	0x0	SECREF Frequency Detection

172 R233 Register (Address = 0xE9) [reset = 0x0]

R233 is shown in Table 173.

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Table 173. R233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PRIREFVLDTMR	R/W	0x0	PRIREF Validation Timer Timer = 0.1 ms x $2^{PRIREFVLDTMR}$

173 R234 Register (Address = 0xEA) [reset = 0x0]

R234 is shown in Table 174.

Return to Summary Table.

Table 174. R234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	SECREFVLDTMR	R/W	0x0	SECREF Validation Timer Timer = 0.1 ms x $2^{SECREFVLDTMR}$

174 R235 Register (Address = 0xEB) [reset = 0x0]

R235 is shown in Table 175.

Return to Summary Table.

Table 175. R235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	PRIREF_PH_VALID_DET_1	R/W	0x0	PRIREF Phase-valid Detection

175 R236 Register (Address = 0xEC) [reset = 0x0]

R236 is shown in Table 176.

Return to Summary Table.

Table 176. R236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_PH_VALID_DET_2	R/W	0x0	PRIREF Phase-valid Detection

176 R237 Register (Address = 0xED) [reset = 0x0]

R237 is shown in Table 177.

Return to Summary Table.

Table 177. R237 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_PH_VALID_DET_3	R/W	0x0	PRIREF Phase-valid Detection

177 R238 Register (Address = 0xEE) [reset = 0x0]

R238 is shown in Table 178.

Return to Summary Table.

Table 178. R238 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_PH_VALID_DET_4	R/W	0x0	PRIREF Phase-valid Detection

178 R239 Register (Address = 0xEF) [reset = 0x0]

R239 is shown in Table 179.

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Table 179. R239 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	SECREF_PH_VALID_DET_1	R/W	0x0	SECREF Phase-valid Detection

179 R240 Register (Address = 0xF0) [reset = 0x0]

R240 is shown in Table 180.

Return to Summary Table.

Table 180. R240 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_PH_VALID_DET_2	R/W	0x0	SECREF Phase-valid Detection

180 R241 Register (Address = 0xF1) [reset = 0x0]

R241 is shown in Table 181.

Return to Summary Table.

Table 181. R241 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_PH_VALID_DET_3	R/W	0x0	SECREF Phase-valid Detection

181 R242 Register (Address = 0xF2) [reset = 0x0]

R242 is shown in Table 182.

Return to Summary Table.

Table 182. R242 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_PH_VALID_DET_4	R/W	0x0	SECREF Phase-valid Detection

182 R243 Register (Address = 0xF3) [reset = 0x0]

R243 is shown in Table 183.

Return to Summary Table.

Table 183. R243 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	PRIREF_PH_VALID_THR	R/W	0x0	PRIREF Phase Valid Threshold

183 R244 Register (Address = 0xF4) [reset = 0x0]

R244 is shown in Table 184.

Return to Summary Table.

Table 184. R244 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	SECREF_PH_VALID_THR	R/W	0x0	SECREF Phase Valid Threshold

184 R249 Register (Address = 0xF9) [reset = 0x0]

R249 is shown in Table 185.

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Table 185. R249 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	DPLL_SECREF_AUTO_PRTY	R/W	0x0	Set priorty for SECREF See DPLL_PRIREF_AUTO_PRTY for bit settings.
3-2	RESERVED	R/W	0x0	Reserved
1-0	DPLL_PRIREF_AUTO_PRTY	R/W	0x0	Set priorty for PRIREF 0x1 = First priority 0x2 = Second priority

185 R251 Register (Address = 0xFB) [reset = 0x0]

R251 is shown in Table 186.

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Table 186. R251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5	DPLL_REF_MAN_SEL	R/W	0x0	Controls source of manual selection 0x0 = Software register: DPLL_REF_MAN_REG_SEL 0x1 = Hardware pin: REFSEL
4	DPLL_REF_MAN_REG_SEL	R/W	0x0	Controls software manual Ref selection 0x0 = Primary Reference 0x1 = Secondary Reference
3-2	RESERVED	R	0x0	Reserved
1-0	DPLL_SWITCH_MODE	R/W	0x0	Controls switchover mode 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual holdover

186 R252 Register (Address = 0xFC) [reset = 0x0]

R252 is shown in Table 187.

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Table 187. R252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_ZDM_SYNC_EN	R/W	0x0	DPLL Zero Delay Synchronization enable
6	RESERVED	R/W	0x0	Reserved
5	DPLL_SWITCHOVER_1	R/W	0x0	DPLL Switchover Timer
4	DPLL_FASTLOCK_ALWAYS	R/W	0x0	Enable DPLL fast lock
3	RESERVED	R/W	0x0	Reserved
2	DPLL_HLDOVR_MODE	R/W	0x0	DPLL Holdover mode when tuning word history unavailable 0x0 = Enter free-run mode 0x1 = Hold last control value prior to holdover
1	RESERVED	R	0x0	Reserved
0	DPLL_LOOP_EN	R/W	0x0	DPLL Enable

187 R253 Register (Address = 0xFD) [reset = 0x0]

R253 is shown in Table 188.

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Table 188. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_SWITCHOVER_2	R/W	0x0	DPLL Switchover Timer

188 R254 Register (Address = 0xFE) [reset = 0x0]

R254 is shown in Table 189.

Return to Summary Table.

Table 189. R254 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2-0	DPLL_SWITCHOVER_3	R/W	0x0	DPLL Switchover Timer

189 R255 Register (Address = 0xFF) [reset = 0x0]

R255 is shown in Table 190.

Return to Summary Table.

Table 190. R255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_SWITCHOVER_4	R/W	0x0	DPLL Switchover Timer

190 R256 Register (Address = 0x100) [reset = 0x0]

R256 is shown in Table 191.

Return to Summary Table.

Table 191. R256 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_PRIREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_PRIREF_RDIV

191 R257 Register (Address = 0x101) [reset = 0x0]

R257 is shown in Table 192.

Return to Summary Table.

Table 192. R257 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_PRIREF_RDIV	R/W	0x0	DPLL PRIREF divider control

192 R258 Register (Address = 0x102) [reset = 0x0]

R258 is shown in Table 193.

Return to Summary Table.

Table 193. R258 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_SECREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_SECREF_RDIV

193 R259 Register (Address = 0x103) [reset = 0x0]

R259 is shown in Table 194.

Return to Summary Table.

Table 194. R259 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_SECREF_RDIV	R/W	0x0	DPLL SECREF divider control

194 R260 Register (Address = 0x104) [reset = 0x0]

R260 is shown in Table 195.

Return to Summary Table.

Table 195. R260 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-2	RESERVED	R	0x0	Reserved
1	DPLL_REF_AVOID_SLIP	R/W	0x0	Disable Cycle Slip
0	RESERVED	R/W	0x0	Reserved

195 R261 Register (Address = 0x105) [reset = 0x0]

R261 is shown in Table 196.

Return to Summary Table.

Table 196. R261 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_REF_1	R/W	0x0	DPLL Reference Control
6-5	RESERVED	R	0x0	Reserved
4-0	RESERVED	R/W	0x0	Reserved

196 R262 Register (Address = 0x106) [reset = 0x0]

R262 is shown in Table 197.

Return to Summary Table.

Table 197. R262 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	DPLL_REF_2	R/W	0x0	DPLL Reference Control

197 R263 Register (Address = 0x107) [reset = 0x0]

R263 is shown in Table 198.

Return to Summary Table.

Table 198. R263 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_3	R/W	0x0	DPLL Reference Control

198 R264 Register (Address = 0x108) [reset = 0x0]

R264 is shown in Table 199.

Return to Summary Table.

Table 199. R264 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_4	R/W	0x0	DPLL Reference Control

199 R265 Register (Address = 0x109) [reset = 0x0]

R265 is shown in Table 200.

Return to Summary Table.

Table 200. R265 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_5	R/W	0x0	DPLL Reference Control

200 R266 Register (Address = 0x10A) [reset = 0x0]

R266 is shown in Table 201.

Return to Summary Table.

Table 201. R266 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_6	R/W	0x0	DPLL Reference Control

201 R267 Register (Address = 0x10B) [reset = 0x0]

R267 is shown in Table 202.

Return to Summary Table.

Table 202. R267 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3	DPLL_REF_7	R/W	0x0	DPLL Reference Control
2-1	DPLL_REF_LF_1	R/W	0x0	DPLL Loop Filter
0	DPLL_REF_LF_2	R/W	0x0	DPLL Loop Filter

202 R268 Register (Address = 0x10C) [reset = 0xF]

R268 is shown in Table 203.

Return to Summary Table.

Table 203. R268 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	DPLL_REF_8	R/W	0x1	DPLL Reference Control
2	DPLL_REF_9	R/W	0x1	DPLL Reference Control

Table 203. R268 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DPLL_REF_10	R/W	0x1	DPLL Reference Control
0	DPLL_REF_11	R/W	0x1	DPLL Reference Control

203 R269 Register (Address = 0x10D) [reset = 0x0]

R269 is shown in Table 204.

Return to Summary Table.

Table 204. R269 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_12	R/W	0x0	DPLL Reference Control

204 R270 Register (Address = 0x10E) [reset = 0x0]

R270 is shown in Table 205.

Return to Summary Table.

Table 205. R270 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	DPLL_REF_LF_3	R/W	0x0	DPLL Loop Filter

205 R271 Register (Address = 0x10F) [reset = 0x1]

R271 is shown in Table 206.

Return to Summary Table.

Table 206. R271 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_LF_4	R/W	0x1	DPLL Loop Filter

206 R272 Register (Address = 0x110) [reset = 0x0]

R272 is shown in Table 207.

Return to Summary Table.

Table 207. R272 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_LF_5	R/W	0x0	DPLL Loop Filter

207 R273 Register (Address = 0x111) [reset = 0x0]

R273 is shown in Table 208.

Return to Summary Table.

Table 208. R273 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_LF_6	R/W	0x0	DPLL Loop Filter

208 R274 Register (Address = 0x112) [reset = 0x0]

R274 is shown in Table 209.

Return to Summary Table.

Table 209. R274 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_LF_7	R/W	0x0	DPLL Loop Filter

209 R275 Register (Address = 0x113) [reset = 0x0]

R275 is shown in Table 210.

Return to Summary Table.

Table 210. R275 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_8	R/W	0x0	DPLL Loop Filter

210 R276 Register (Address = 0x114) [reset = 0x0]

R276 is shown in Table 211.

Return to Summary Table.

Table 211. R276 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_9	R/W	0x0	DPLL Loop Filter

211 R277 Register (Address = 0x115) [reset = 0x0]

R277 is shown in Table 212.

Return to Summary Table.

Table 212. R277 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_10	R/W	0x0	DPLL Loop Filter

212 R278 Register (Address = 0x116) [reset = 0x0]

R278 is shown in Table 213.

Return to Summary Table.

Table 213. R278 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_11	R/W	0x0	DPLL Loop Filter

213 R279 Register (Address = 0x117) [reset = 0x0]

R279 is shown in Table 214.

Return to Summary Table.

Table 214. R279 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_12	R/W	0x0	DPLL Loop Filter

214 R280 Register (Address = 0x118) [reset = 0x0]

R280 is shown in Table 215.

Return to Summary Table.

Table 215. R280 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_13	R/W	0x0	DPLL Loop Filter

215 R281 Register (Address = 0x119) [reset = 0x0]

R281 is shown in Table 216.

Return to Summary Table.

Table 216. R281 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_14	R/W	0x0	DPLL Loop Filter

216 R282 Register (Address = 0x11A) [reset = 0x0]

R282 is shown in Table 217.

Return to Summary Table.

Table 217. R282 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_15	R/W	0x0	DPLL Loop Filter

217 R283 Register (Address = 0x11B) [reset = 0x0]

R283 is shown in Table 218.

Return to Summary Table.

Table 218. R283 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_16	R/W	0x0	DPLL Loop Filter

218 R284 Register (Address = 0x11C) [reset = 0x0]

R284 is shown in Table 219.

Return to Summary Table.

Table 219. R284 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_17	R/W	0x0	DPLL Loop Filter

219 R285 Register (Address = 0x11D) [reset = 0x0]

R285 is shown in Table 220.

Return to Summary Table.

Table 220. R285 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_LF_18	R/W	0x0	DPLL Loop Filter

220 R286 Register (Address = 0x11E) [reset = 0x0]

R286 is shown in Table 221.

Return to Summary Table.

Table 221. R286 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	DPLL_REF_LF_19	R/W	0x0	DPLL Loop Filter

221 R287 Register (Address = 0x11F) [reset = 0x0]

R287 is shown in Table 222.

Return to Summary Table.

Table 222. R287 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_LF_20	R/W	0x0	DPLL Loop Filter

222 R288 Register (Address = 0x120) [reset = 0x0]

R288 is shown in Table 223.

Return to Summary Table.

Table 223. R288 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	DPLL_REF_LF_21	R/W	0x0	DPLL Loop Filter

223 R289 Register (Address = 0x121) [reset = 0x0]

R289 is shown in Table 224.

Return to Summary Table.

Table 224. R289 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_LF_22	R/W	0x0	DPLL Loop Filter

224 R290 Register (Address = 0x122) [reset = 0x0]

R290 is shown in Table 225.

Return to Summary Table.

Table 225. R290 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	DPLL_PL_DET_1	R/W	0x0	DPLL Phase Lock Detection

225 R291 Register (Address = 0x123) [reset = 0x0]

R291 is shown in Table 226.

Return to Summary Table.

Table 226. R291 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_PL_DET_2	R/W	0x0	DPLL Phase Lock Detection

226 R292 Register (Address = 0x124) [reset = 0x0]

R292 is shown in Table 227.

Return to Summary Table.

Table 227. R292 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	DPLL_HITLESS_SW_1	R/W	0x0	Phase Cancellation for Hitless Switching

227 R293 Register (Address = 0x125) [reset = 0x1]

R293 is shown in Table 228.

Return to Summary Table.

Table 228. R293 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	DPLL_HITLESS_SW_2	R/W	0x1	Phase Cancellation for Hitless Switching

228 R294 Register (Address = 0x126) [reset = 0x0]

R294 is shown in Table 229.

Return to Summary Table.

Table 229. R294 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	DPLL_HITLESS_SW_3	R/W	0x0	Phase Cancellation for Hitless Switching

229 R295 Register (Address = 0x127) [reset = 0x0]

R295 is shown in Table 230.

Return to Summary Table.

Table 230. R295 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_HITLESS_SW_4	R/W	0x0	Phase Cancellation for Hitless Switching

230 R296 Register (Address = 0x128) [reset = 0x0]

R296 is shown in Table 231.

Return to Summary Table.

Table 231. R296 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_LF_23	R/W	0x0	DPLL Loop Filter

231 R297 Register (Address = 0x129) [reset = 0x0]

R297 is shown in Table 232.

Return to Summary Table.

Table 232. R297 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_LF_24	R/W	0x0	DPLL Loop Filter

232 R298 Register (Address = 0x12A) [reset = 0x0]

R298 is shown in Table 233.

Return to Summary Table.

Table 233. R298 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_LF_25	R/W	0x0	DPLL Loop Filter

233 R300 Register (Address = 0x12C) [reset = 0x0]

R300 is shown in Table 234.

Return to Summary Table.

Table 234. R300 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_PL_DET_3	R/W	0x0	DPLL Phase Lock Detection

234 R301 Register (Address = 0x12D) [reset = 0x0]

R301 is shown in Table 235.

Return to Summary Table.

Table 235. R301 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_PL_LOCK_THRESH	R/W	0x0	Phase lock declaration threshold

235 R302 Register (Address = 0x12E) [reset = 0x0]

R302 is shown in Table 236.

Return to Summary Table.

Table 236. R302 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_PL_UNLK_THRESH	R/W	0x0	Phase un-lock declaration threshold

236 R304 Register (Address = 0x130) [reset = 0x0]

R304 is shown in Table 237.

Return to Summary Table.

Table 237. R304 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	DPLL_REF_FB_PRE_DIV	R/W	0x0	DPLL REF Feedback Pre Divider value Divider value ranges from 2 to 17. Divider value = DPLL_REF_FB_PRE_DIV + 2.

237 R305 Register (Address = 0x131) [reset = 0x0]

R305 is shown in Table 238.

Return to Summary Table.

Table 238. R305 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_REF_FB_DIV_29:24	R/W	0x0	Bits 29:24 of DPLL_REF_FB_DIV

238 R306 Register (Address = 0x132) [reset = 0x0]

R306 is shown in Table 239.

Return to Summary Table.

Table 239. R306 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_FB_DIV_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_FB_DIV

239 R307 Register (Address = 0x133) [reset = 0x0]

R307 is shown in Table 240.

Return to Summary Table.

Table 240. R307 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_FB_DIV_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_FB_DIV

240 R308 Register (Address = 0x134) [reset = 0xC8]

R308 is shown in Table 241.

Return to Summary Table.

Table 241. R308 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_FB_DIV	R/W	0xC8	DPLL REF Feedback Divider value

241 R309 Register (Address = 0x135) [reset = 0x0]

R309 is shown in Table 242.

Return to Summary Table.

Table 242. R309 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_NUM_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_NUM

242 R310 Register (Address = 0x136) [reset = 0x0]

R310 is shown in Table 243.

Return to Summary Table.

Table 243. R310 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_NUM_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_NUM

243 R311 Register (Address = 0x137) [reset = 0x0]

R311 is shown in Table 244.

Return to Summary Table.

Table 244. R311 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_NUM_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_NUM

244 R312 Register (Address = 0x138) [reset = 0x0]

R312 is shown in Table 245.

Return to Summary Table.

Table 245. R312 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_NUM_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_NUM

245 R313 Register (Address = 0x139) [reset = 0x0]

R313 is shown in Table 246.

Return to Summary Table.

Table 246. R313 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_NUM	R/W	0x0	DPLL REF FB Divider Numerator

246 R314 Register (Address = 0x13A) [reset = 0x0]

R314 is shown in Table 247.

Return to Summary Table.

Table 247. R314 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_DEN_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_DEN

247 R315 Register (Address = 0x13B) [reset = 0x0]

R315 is shown in Table 248.

Return to Summary Table.

Table 248. R315 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_DEN_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_DEN

248 R316 Register (Address = 0x13C) [reset = 0x0]

R316 is shown in Table 249.

Return to Summary Table.

Table 249. R316 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_DEN_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_DEN

249 R317 Register (Address = 0x13D) [reset = 0x0]

R317 is shown in Table 250.

Return to Summary Table.

Table 250. R317 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_DEN_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_DEN

250 R318 Register (Address = 0x13E) [reset = 0x0]

R318 is shown in Table 251.

Return to Summary Table.

Table 251. R318 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_DEN	R/W	0x0	DPLL REF FB Divider denominator

251 R319 Register (Address = 0x13F) [reset = 0x18]

R319 is shown in Table 252.

Return to Summary Table.

Table 252. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-5	RESERVED	R/W	0x0	Reserved
4-3	DPLL_REF_13	R/W	0x3	DPLL Reference Control
2-0	DPLL_REF_14	R/W	0x0	DPLL Reference Control

252 R320 Register (Address = 0x140) [reset = 0x0]

R320 is shown in Table 253.

Return to Summary Table.

Table 253. R320 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-0	DPLL_LOCK_DET_1	R/W	0x0	DPLL DCO Lock Detection

253 R321 Register (Address = 0x141) [reset = 0x0]

R321 is shown in Table 254.

Return to Summary Table.

Table 254. R321 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_2	R/W	0x0	DPLL DCO Lock Detection

254 R322 Register (Address = 0x142) [reset = 0x0]

R322 is shown in Table 255.

Return to Summary Table.

Table 255. R322 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_LOCK_DET_3	R/W	0x0	DPLL DCO Lock Detection

255 R323 Register (Address = 0x143) [reset = 0x0]

R323 is shown in Table 256.

Return to Summary Table.

Table 256. R323 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_4	R/W	0x0	DPLL DCO Lock Detection

256 R324 Register (Address = 0x144) [reset = 0x0]

R324 is shown in Table 257.

Return to Summary Table.

Table 257. R324 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_5	R/W	0x0	DPLL DCO Lock Detection

257 R325 Register (Address = 0x145) [reset = 0x0]

R325 is shown in Table 258.

Return to Summary Table.

Table 258. R325 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_6	R/W	0x0	DPLL DCO Lock Detection

258 R326 Register (Address = 0x146) [reset = 0x0]

R326 is shown in Table 259.

Return to Summary Table.

Table 259. R326 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_LOCK_DET_7	R/W	0x0	DPLL DCO Lock Detection

259 R327 Register (Address = 0x147) [reset = 0x0]

R327 is shown in Table 260.

Return to Summary Table.

Table 260. R327 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_8	R/W	0x0	DPLL DCO Lock Detection

260 R328 Register (Address = 0x148) [reset = 0x0]

R328 is shown in Table 261.

Return to Summary Table.

Table 261. R328 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_9	R/W	0x0	DPLL DCO Lock Detection

261 R329 Register (Address = 0x149) [reset = 0x0]

R329 is shown in Table 262.

Return to Summary Table.

Table 262. R329 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_LOCK_DET_10	R/W	0x0	DPLL DCO Lock Detection

262 R330 Register (Address = 0x14A) [reset = 0x0]

R330 is shown in Table 263.

Return to Summary Table.

Table 263. R330 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 263. R330 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	DPLL_UNLK_DET_1	R/W	0x0	DPLL DCO Unlock Detection

263 R331 Register (Address = 0x14B) [reset = 0x0]

R331 is shown in Table 264.

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Table 264. R331 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_2	R/W	0x0	DPLL DCO Unlock Detection

264 R332 Register (Address = 0x14C) [reset = 0x0]

R332 is shown in Table 265.

Return to Summary Table.

Table 265. R332 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_UNLK_DET_3	R/W	0x0	DPLL DCO Unlock Detection

265 R333 Register (Address = 0x14D) [reset = 0x0]

R333 is shown in Table 266.

Return to Summary Table.

Table 266. R333 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_4	R/W	0x0	DPLL DCO Unlock Detection

266 R334 Register (Address = 0x14E) [reset = 0x0]

R334 is shown in Table 267.

Return to Summary Table.

Table 267. R334 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_5	R/W	0x0	DPLL DCO Unlock Detection

267 R335 Register (Address = 0x14F) [reset = 0x0]

R335 is shown in Table 268.

Return to Summary Table.

Table 268. R335 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_6	R/W	0x0	DPLL DCO Unlock Detection

268 R336 Register (Address = 0x150) [reset = 0x0]

R336 is shown in Table 269.

Return to Summary Table.

Table 269. R336 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_UNLK_DET_7	R/W	0x0	DPLL DCO Unlock Detection

269 R337 Register (Address = 0x151) [reset = 0x0]

R337 is shown in Table 270.

Return to Summary Table.

Table 270. R337 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_8	R/W	0x0	DPLL DCO Unlock Detection

270 R338 Register (Address = 0x152) [reset = 0x0]

R338 is shown in Table 271.

Return to Summary Table.

Table 271. R338 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_9	R/W	0x0	DPLL DCO Unlock Detection

271 R339 Register (Address = 0x153) [reset = 0x0]

R339 is shown in Table 272.

Return to Summary Table.

Table 272. R339 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_UNLK_DET_10	R/W	0x0	DPLL DCO Unlock Detection

272 R340 Register (Address = 0x154) [reset = 0x0]

R340 is shown in Table 273.

Return to Summary Table.

Table 273. R340 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	DPLL_REF_SYNC_PH_OFFSET_44:40	R/W	0x0	Bits 44:40 of DPLL_REF_SYNC_PH_OFFSET

273 R341 Register (Address = 0x155) [reset = 0x0]

R341 is shown in Table 274.

Return to Summary Table.

Table 274. R341 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_SYNC_PH_OFFSET_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_SYNC_PH_OFFSET

274 R342 Register (Address = 0x156) [reset = 0x0]

R342 is shown in Table 275.

Return to Summary Table.

Table 275. R342 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_SYNC_PH_OFFSET_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_SYNC_PH_OFFSET

275 R343 Register (Address = 0x157) [reset = 0x0]

R343 is shown in Table 276.

Return to Summary Table.

Table 276. R343 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_SYNC_PH_OFFSET_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_SYNC_PH_OFFSET

276 R344 Register (Address = 0x158) [reset = 0x0]

R344 is shown in Table 277.

Return to Summary Table.

Table 277. R344 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_SYNC_PH_OFFSET_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_SYNC_PH_OFFSET

277 R345 Register (Address = 0x159) [reset = 0x0]

R345 is shown in Table 278.

Return to Summary Table.

Table 278. R345 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_SYNC_PH_OFFSET	R/W	0x0	DPLL REF Zero Delay Mode Phase Offset

278 R346 Register (Address = 0x15A) [reset = 0x0]

R346 is shown in Table 279.

Return to Summary Table.

Table 279. R346 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	DPLL_FDEV_EN	R/W	0x0	DPLL Freq Incr/Decr enable via pin or reg control

279 R347 Register (Address = 0x15B) [reset = 0x0]

R347 is shown in Table 280.

Return to Summary Table.

Table 280. R347 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	DPLL_FDEV_37:32	R/W	0x0	Bits 37:32 of DPLL_FDEV

280 R348 Register (Address = 0x15C) [reset = 0x0]

R348 is shown in Table 281.

Return to Summary Table.

Table 281. R348 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_FDEV_31:24	R/W	0x0	Bits 31:24 of DPLL_FDEV

281 R349 Register (Address = 0x15D) [reset = 0x0]

R349 is shown in Table 282.

Return to Summary Table.

Table 282. R349 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_FDEV_23:16	R/W	0x0	Bits 23:16 of DPLL_FDEV

282 R350 Register (Address = 0x15E) [reset = 0x0]

R350 is shown in Table 283.

Return to Summary Table.

Table 283. R350 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_FDEV_15:8	R/W	0x0	Bits 15:8 of DPLL_FDEV

283 R351 Register (Address = 0x15F) [reset = 0x0]

R351 is shown in Table 284.

Return to Summary Table.

Table 284. R351 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_FDEV	R/W	0x0	DPLL Freq Incr/Decr Numerator Step Word This step word is computed based on the desired DCO frequecy step size in ppb (parts-per-billion).

284 R352 Register (Address = 0x160) [reset = 0x0]

R352 is shown in Table 285.

Return to Summary Table.

Table 285. R352 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	DPLL_FDEV_REG_UPDATE	R/W	0x0	DPLL Freq Incr/Decr register control Writing this register applies one FINC/FDEC of the Numerator as defined by the FDEV register.

285 R357 Register (Address = 0x165) [reset = 0x0]

R357 is shown in Table 286.

Return to Summary Table.

Table 286. R357 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	PLL1_VM_INSIDE	R	0x0	PLL1 VCO Status Denotes if the PLL1 charge pump voltage is within operational range.
4-0	RESERVED	R	0x0	Reserved

286 R367 Register (Address = 0x16F) [reset = 0x0]

R367 is shown in Table 287.

Return to Summary Table.

Table 287. R367 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x0	PLL2 VCO Status Denotes if the PLL2 charge pump voltage is within operational range.
4-0	RESERVED	R	0x0	Reserved

287 R411 Register (Address = 0x19B) [reset = 0x0]

R411 is shown in Table 288.

Return to Summary Table.

Table 288. R411 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	SECREF_VALSTAT	R	0x0	SECREF valid state
2	PRIREF_VALSTAT	R	0x0	PRIREF valid state
1	RESERVED	R	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2019) to A Revision	Page
• Updated and added register names	1

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