LMH0026,LMH0036,LMH0046,LMH0056,LMH0346, LMH0356,LMH6321

Literature Number: SNLA197

Reference Clock Daisy-Chaining in the National Semiconductor LMH0XX6 Family of SDI reclockers

National Semiconductor Lab Report

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Abstract

For high density SDI applications it is desirable to use a single reference clock for multiple reclockers. This saves PCB space, component count, and system cost. One scheme for using a single reference clock for multiple reclockers is to connect the XTAL OUT output of one reclocker to the XTAL IN input of the next, propagating the 27 MHz reference signal through a cascade of reclockers. This scheme is referred to as *reference clock daisy-chaining*.

In this report, we discuss the performance of the National Semiconductor reclocker family with the use of a daisy-chained reference clock. The loading on each reclocker's XTAL OUT output and the average DC level at each reclocker's XTAL IN input are critical to proper operation of the daisy-chained reference clock.

We have successfully daisy-chained a single 27 MHz reference clock with 32 National Semiconductor LMH0356 3 Gbps HD/SD reclockers. The cascade of 32 LMH0356 reclockers was tested using the matrix pathological data pattern at 2.97 Gbps. This system ran with no bit errors for over three consecutive days.

We have also investigated the effects of different architectures for coupling the reference clock from one reclocker to another. For reclockers on a single board, optimum reference clock daisy-chain performance is achieved by coupling the XTAL OUT output of each reclocker to the XTAL IN input on the next reclocker using an AC coupling capacitor of 0.1 µF and a bias resistor divider network of two 1KΩ resistors (FIGURE 5). Other coupling schemes may also be used with certain performance tradeoffs.

Where it is necessary to propagate the reference signal from one board to another over a coaxial cable, it is recommended that a unity gain buffer such as the National Semiconductor LMH6321 be used at the output of the board supplying the reference signal. This device can be configured with a 50Ω series output resistor as shown in National Semiconductor Application Note AN-1461 to provide a matched source for a 50Ω coaxial cable. The input to the **first device only** on the second board should be terminated in a termination resistor divider network (which will also set the input common mode voltage) consisting of two 100Ω resistors. This provides a well-matched termination for the cable.

A summary of the experiments performed and the resulting recommendations is shown in Table 1.

Table 1. Summary of Results and Recommendations

Method	Advantage	Limitation	Notes
AC Coupling with 100Ω Termination Resistors	Sets common mode input voltage; low-reflection termination for PCB transmission lines	Small signal swing, large static DC power, low SNR	Use higher value termination resistors
AC Coupling with 1000Ω Termination Resistors	Sets common mode input voltage; good signal swing; low static DC power; higher SNR	Poor match to PCB transmission lines	Recommended for reference daisy chain operation; impedance match is controlled by short PCB transmission lines
DC Coupling with No Termination Resistors	No external coupling components; no static DC power in termination networks	Sensitive to small variations in input common mode voltage	Not reliable for reference daisy chain operation
DC Coupling with 1000Ω Termination Resistors	Sets common mode input voltage; good signal swing; low static DC power; higher SNR; fewer components	Not as robust with respect to variations in input common mode voltage	Possible alternative to AC coupling with 1000Ω termination resistors
Cable Driver/Buffer	Drives reference signal over cable between boards	Extra component	Use for long PCB transmission line or cable

Introduction

The National Semiconductor family of SDI reclockers (LMH0026/LMH0036/LMH0046/LMH0056/ LMH0346/LMH0356) requires a 27 MHz reference clock for operation. The reference clock is used for the digital logic in the reclockers. It is also used as a frequency reference during the phase-lock acquisition sequence, in which the reclocker acquires phase lock to the incoming data signal.

The reclocker family is designed to use either a user-supplied 27 MHz reference signal or a 27 MHz crystal for each reclocker. The reclocker reference oscillator architecture is flexible, however, so that the 27 MHz reference can be daisy-chained from one reclocker to the next. The block diagram of FIGURE 1 illustrates the architecture for daisy-chaining the reference signal.

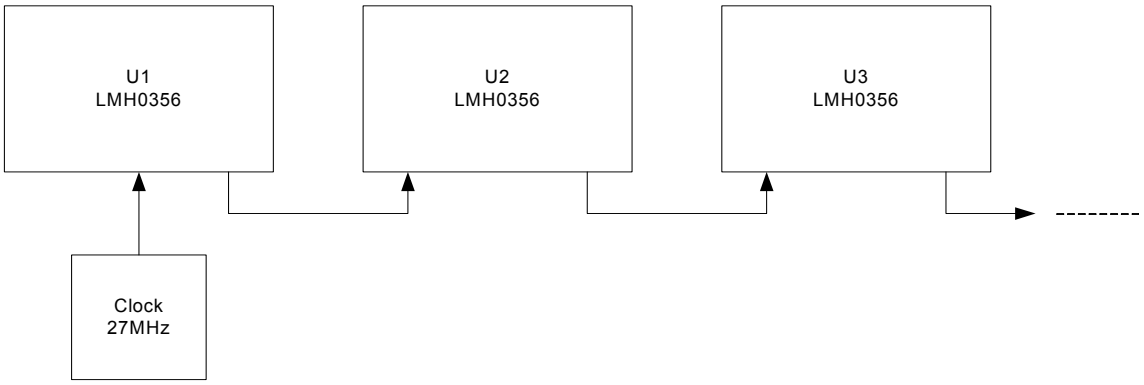

FIGURE 1 - Simplified Block Diagram

The 27 MHz reference signal at the XTAL OUT output of the first reclocker drives the XTAL IN input of the second reclocker. This reference signal can be generated by the first reclocker using its crystal oscillator or supplied from an external source, The XTAL OUT output of the second reclocker drives the XTAL IN input of the third reclocker and so on; this architecture can be replicated for many reclockers in cascade, all sharing the same original 27 MHz reference signal.

The circuit architecture used to couple the 27 MHz reference signal from one reclocker to the next comprises a coupling architecture (DC or AC coupled) and a termination scheme which also sets the input common mode voltage for the following stage. Both of these elements affect the performance of the 27 MHz reference signal coupling. The architecture used to couple the 27 MHz reference signal and the resulting performance of the reclockers is explored in this document.

Reference Clock Requirements

The National Semiconductor family of SDI reclockers is designed to automatically acquire phase lock to SMPTE-compliant video signals with a variety of bit rates. To support this automatic phase-lock acquisition, the reclocker requires an accurate frequency reference. Since 27 MHz frequency reference signals are common in digital video systems, the SDI reclocker family was designed to use a 27 MHz reference frequency.

At the beginning of the phase-lock acquisition sequence, the reclocker sets its internal clock VCO to a frequency close to the clock frequency of the data signal. During this part of the phase-lock acquisition sequence a phase/frequency detector compares the divided clock VCO to the 27 MHz reference and drives the VCO into phase lock with the reference. Once the VCO frequency is set, a separate phase-locked loop drives the VCO into phase lock with the incoming data signal.

After the VCO frequency is initially set the 27 MHz reference signal does not affect the output jitter of the reclocker. The 27 MHz reference signal must be sufficiently accurate and clean enough to lock the VCO to a frequency close to the data frequency. Beyond that, the quality of the reference signal is not critical.

Reference Clock Signal Generation

The design for the reclockers includes a crystal oscillator circuit. This circuit is shown schematically in FIGURE 2. This architecture is adaptable to daisy-chaining the reference signal. When the reference signal is daisy-chained the oscillator circuit acts as an inverting buffer.

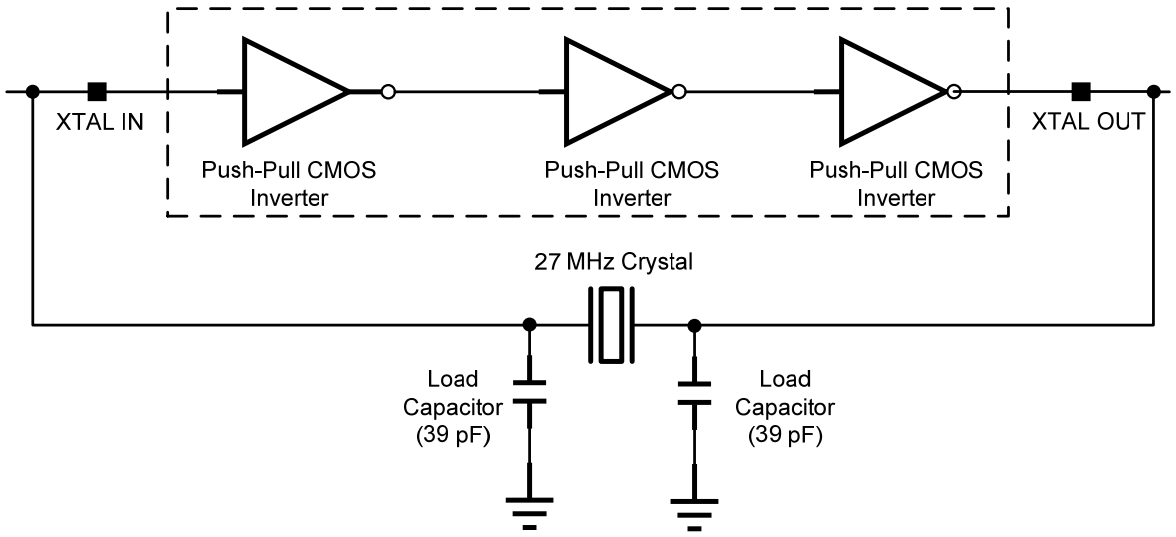

FIGURE 2 – Schematic Illustration of the LMH0XX6 Crystal Oscillator Circuit

Reference Daisy-Chain Circuit Experiments

Several reference daisy-chain architectures were evaluated using a set of 8-channel output cards with various assembly options. The output cards were designed to mate with corresponding 8-channel input cards. The output cards were designed so that the 27 MHz reference signal could be daisy-chained from one reclocker to all the others on an output card with short PC board traces. The output cards were also designed so that the 27 MHz reference signal could be daisy-chained from one output card to another by means of a 50Ω coaxial cable. A schematic for the 8-channel output card is shown in FIGURE 3.

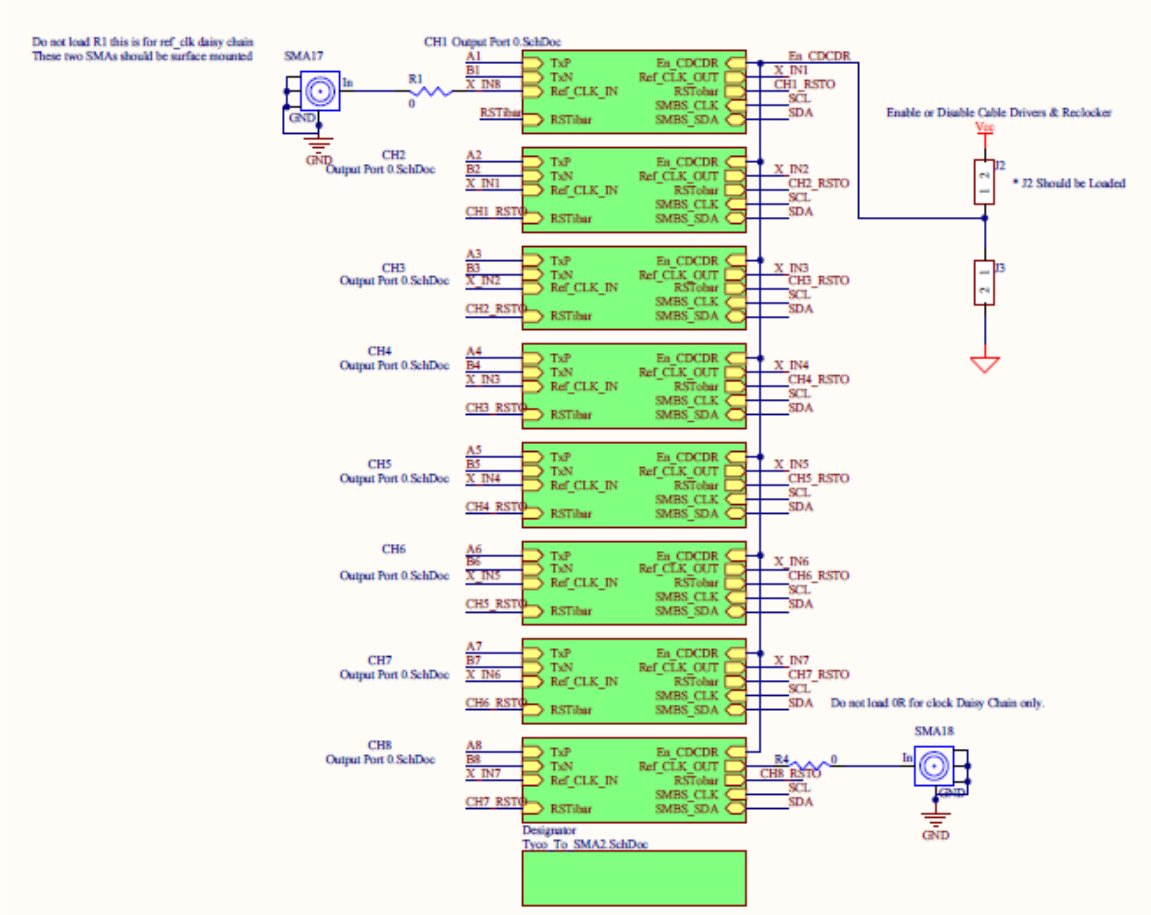

FIGURE 3 - Partial Schematic of the 8-Channel Output Card

A section of the PC board layout of the output card is shown in FIGURE 4. This figure shows channel 1 of the output card. The callouts indicate the PC board trace used to transport the 27 MHz reference signal from the reclocker on channel 1 to the reclocker on channel 2 for daisy-chaining. The layouts are identical for all the channels on this card.

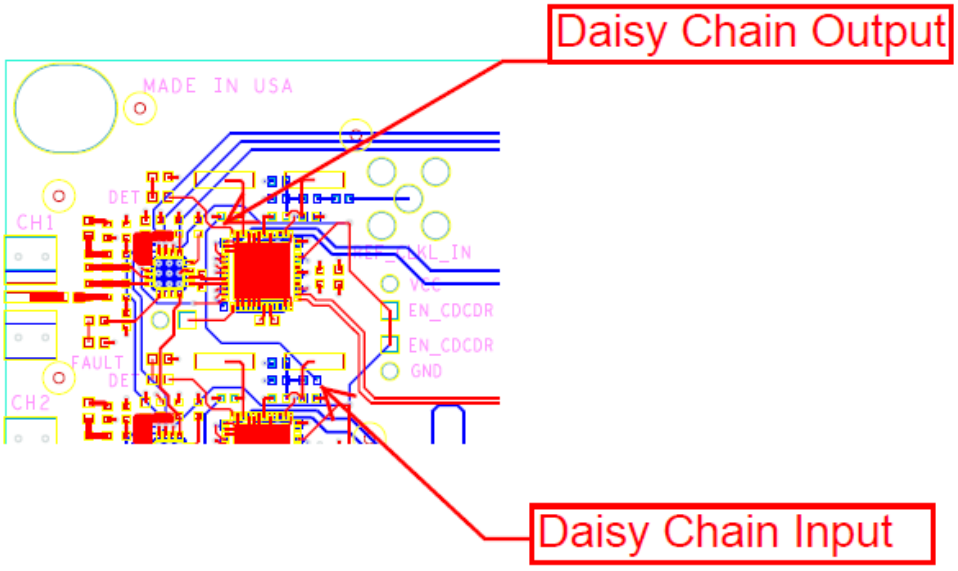

FIGURE 4 - Layout of the 8-Channel Output Card, Channel 1, Showing the Daisy-Chain Connection

AC Coupling with 1KΩ Terminations

The circuit shown in FIGURE 5, AC coupled with 1KΩ terminations, is the recommended circuit configuration for daisy-chaining the reference clock. The placement of the coupling capacitor and the voltage divider resistors on the board is not critical as long as the transmission line between the reclockers is kept electrically short. A good rule of thumb for the length of this transmission line is the same as the rule of thumb for the length of an unterminated stub on a PC board. The length of the transmission line in inches (L) should be less than or equal to the rise time of the signal in ns (T_R). For the 27 MHz reference, $T_R \approx 4$ns, so we should design for $L \leq 4$".

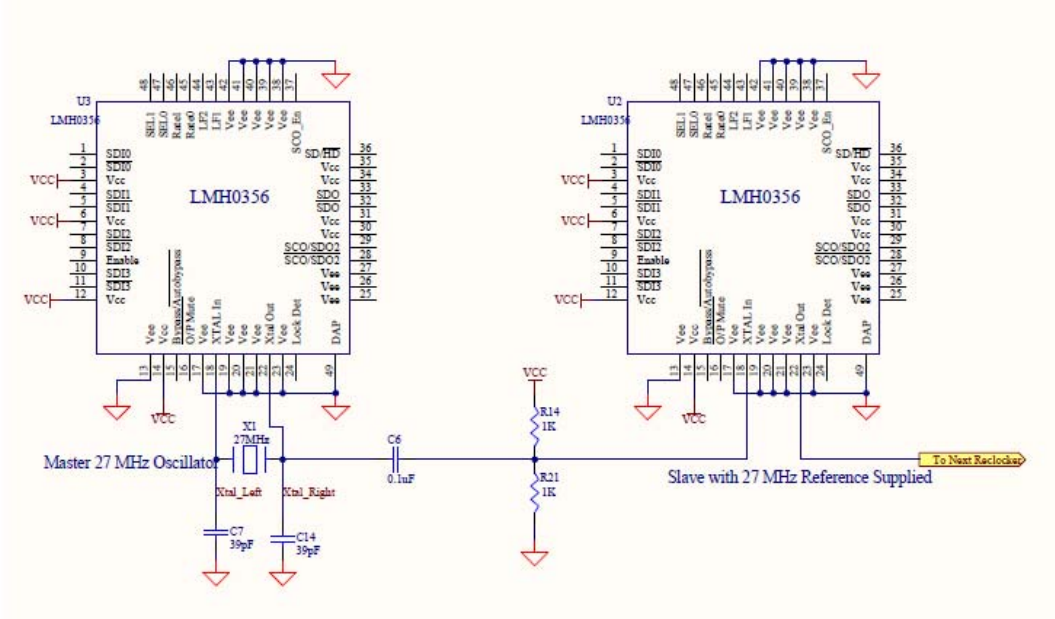

FIGURE 5 - Recommended Reference Clock Daisy-Chain Design with AC Coupling Between the Reclocker Reference Stages

FIGURE 6 shows the XTAL OUT output of the reclockers for channel 1. FIGURE 7 shows the XTAL OUT output of the reclockers for channel 3. As expected, the output of channel 1 is essentially a single-frequency sinusoid, and the outputs of subsequent channels show some rounding in the waveforms. The amplitude of the output of all the channels is approximately 1V.

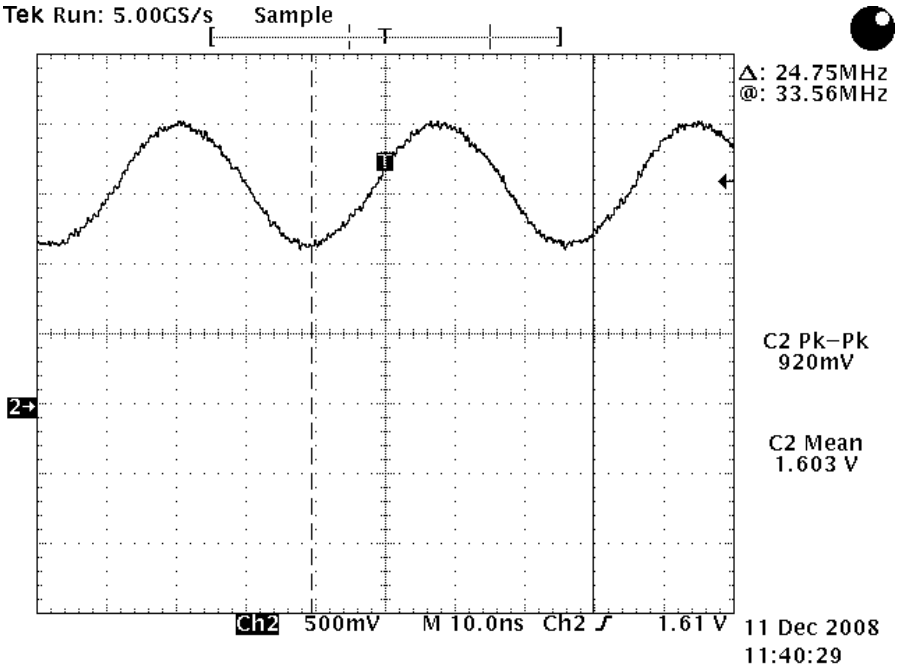

FIGURE 6 - XTAL OUT Output of Channel 1, AC Coupled, 1KΩ Terminations

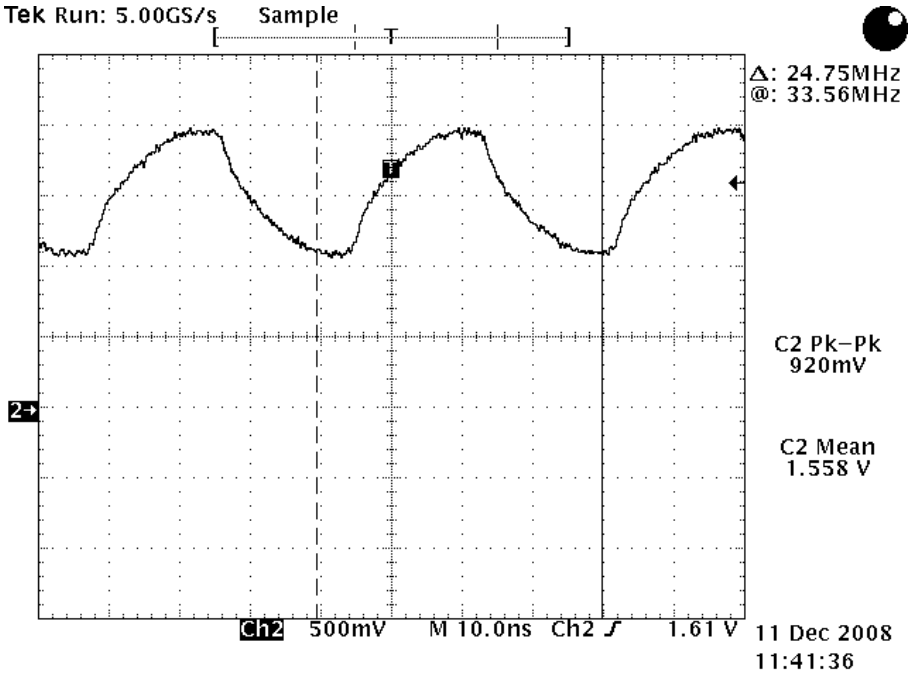

FIGURE 7 - XTAL OUT Output of Channel 3, AC Coupled, 1KΩ Terminations

For this circuit configuration the mean voltage at the XTAL IN input to each reclocker is approximately the nominal value of $V_{CC}/2$. The 1KΩ terminations in combination with AC coupling are sufficient to constrain the common mode voltage at the input to each reclocker stage so that stable operation is maintained throughout the 27 MHz reference daisy-chain. Smaller termination resistors would also work but would draw more static DC current from the power supply.

The spectrum of the XTAL OUT output for channel 1 is shown in FIGURE 8. FIGURE 9 shows the spectrum of the output for channel 8, which is unterminated in this experiment. This channel shows no significant difference from the channels earlier in the chain.

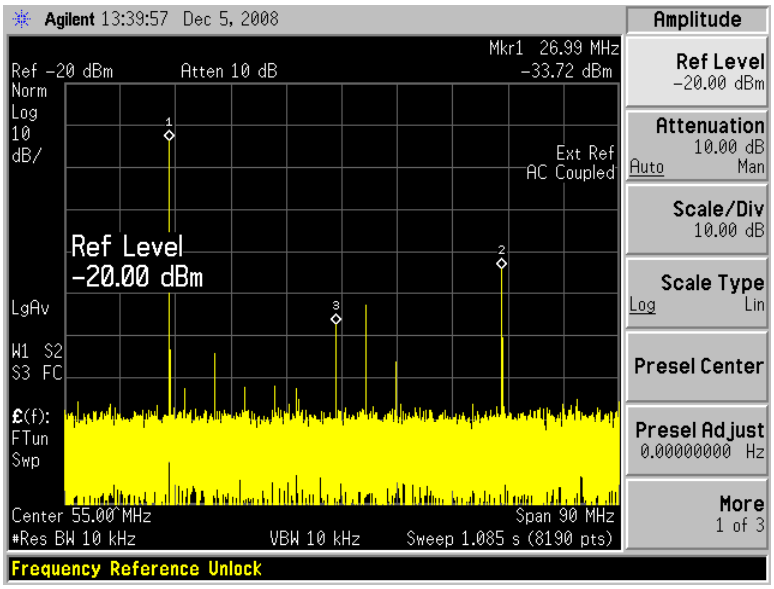

FIGURE 8 - Spectrum Analyzer Measurement of XTAL OUT Output of Channel 1, AC Coupled, 1KΩ Terminations

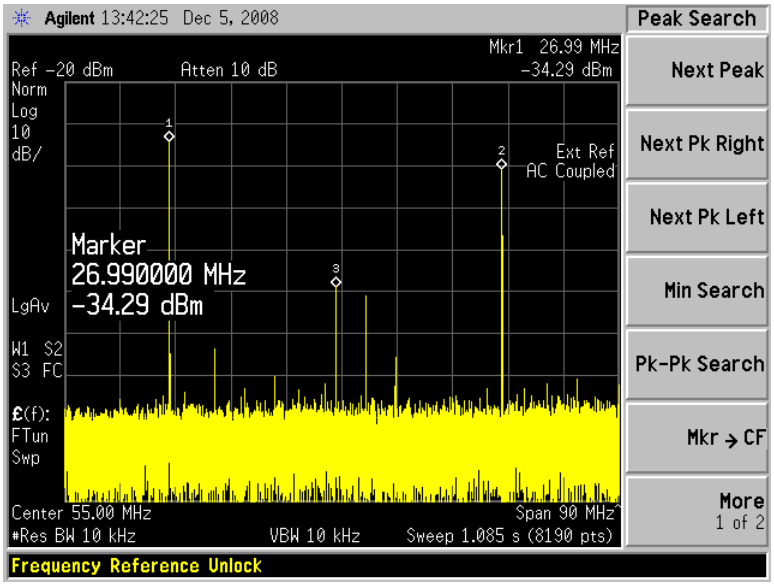

FIGURE 9 - Spectrum Analyzer Measurement of XTAL OUT Output of Channel 8, AC Coupled, 1KΩ Terminations

Alternative Circuit Architectures

DC Coupling with No External Terminations

For the circuit shown in FIGURE 10, DC coupled with no external terminations, one might expect that the signal amplitude would be large (rail-to-rail) at the XTAL OUT output of each reclocker and that the signal would be essentially the same as it propagates from one reclocker to the next. Accordingly, one might expect this circuit architecture to perform well in a reference daisy-chain application. Unfortunately, this does not turn out to be the case.

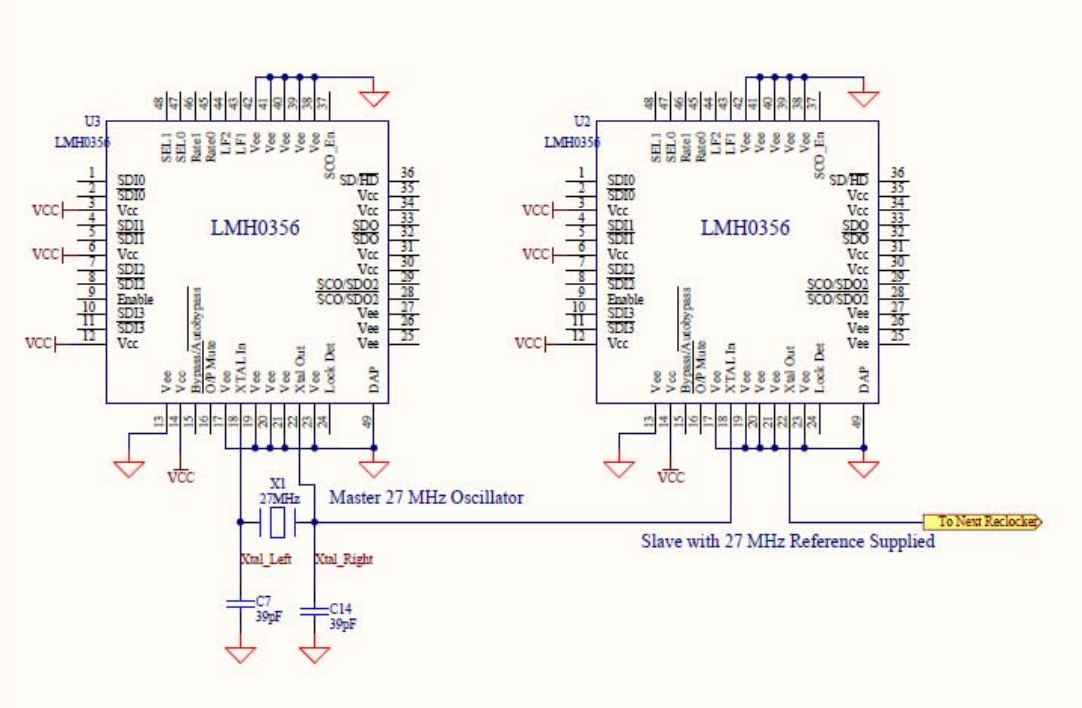

FIGURE 10 - Reference Clock Daisy-Chain Design with DC Coupling and No External Terminations

For this circuit architecture, the mean (common mode) value of the XTAL OUT output voltage begins to deviate from its nominal value of $V_{CC}/2$ as the signal propagates down the chain. Since the buffer in each reclocker performs an inversion, the sign of the deviation reverses at each stage and its absolute value increases. This manifests itself by an increasing duty-cycle distortion which lengthens the negative and positive pulses alternately. By the time the signal reaches the input of channel 8 there is not enough signal amplitude to cause the crystal oscillator circuit to toggle. FIGURE 11 shows a plot of the mean XTAL OUT output voltage for each channel.

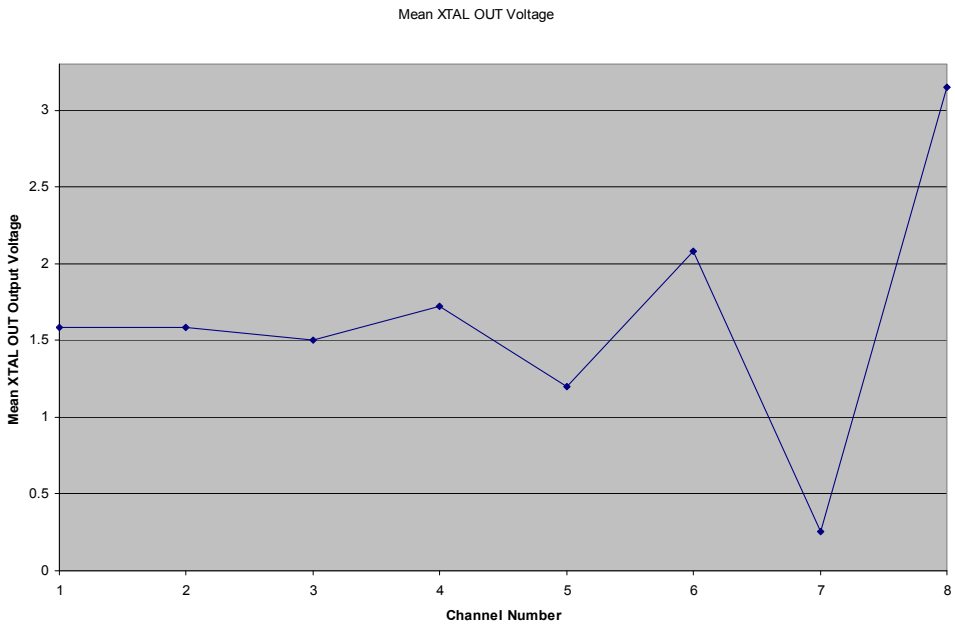

FIGURE 11 - Mean XTAL OUT Output Voltage Versus Channel Number

As the 27 MHz reference signal propagates down the chain of reclockers it also becomes significantly noisier as viewed on the oscilloscope. It is not possible to capture this behavior on the static oscilloscope shots shown but spectrum analyzer measurements illustrate the effect.

The spectrum of the XTAL OUT output reference signal from channel 1 is shown in FIGURE 12. There is a strong spectral line at 27 MHz and much less power (-40 dB) at the second harmonic. By the time the reference signal has propagated to channel 7, shown in FIGURE 13, there is much more power near the second harmonic and noise skirts appear in the spectrum around each of the measured harmonics.

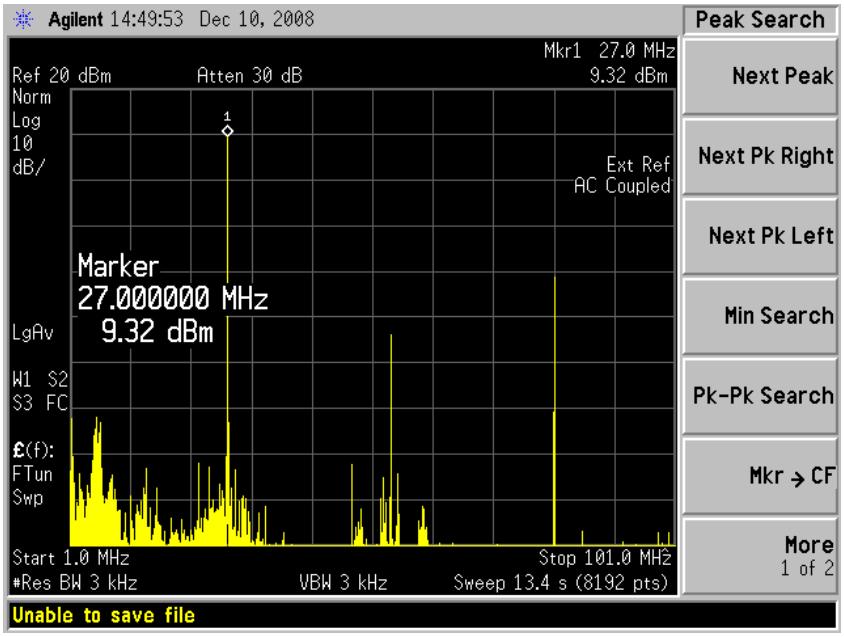

FIGURE 12 - Spectrum Analyzer Measurement of XTAL OUT Output of Channel 1, DC Coupled, No Terminations

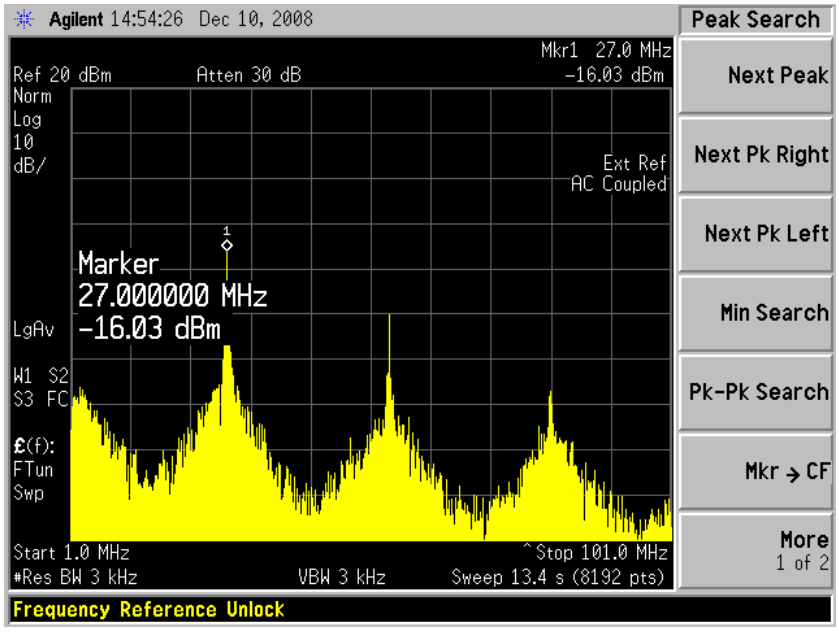

FIGURE 13 - Spectrum Analyzer Measurement of XTAL OUT Output of Channel 7, DC Coupled, No Terminations

Because of the buildup of noise on the spectrum and the deviation of the common mode voltage from the nominal value of $V_{CC}/2$, this configuration is not recommended for reference clock daisy-chain applications.

DC Coupling with 1KΩ Terminations

FIGURE 14 shows the mean value of the XTAL OUT output voltage versus channel number for DC coupling with 1KΩ terminations. There was no build up of deviations of the mean voltage from the nominal value of VCC/2. The 1KΩ terminations were sufficient to constrain the common mode voltage at the input to each reclocker stage so that stable operation was maintained throughout the 27 MHz reference daisy-chain. DC coupling with 1KΩ terminations can provide an alternative architecture for reliable reference daisy-chain performance.

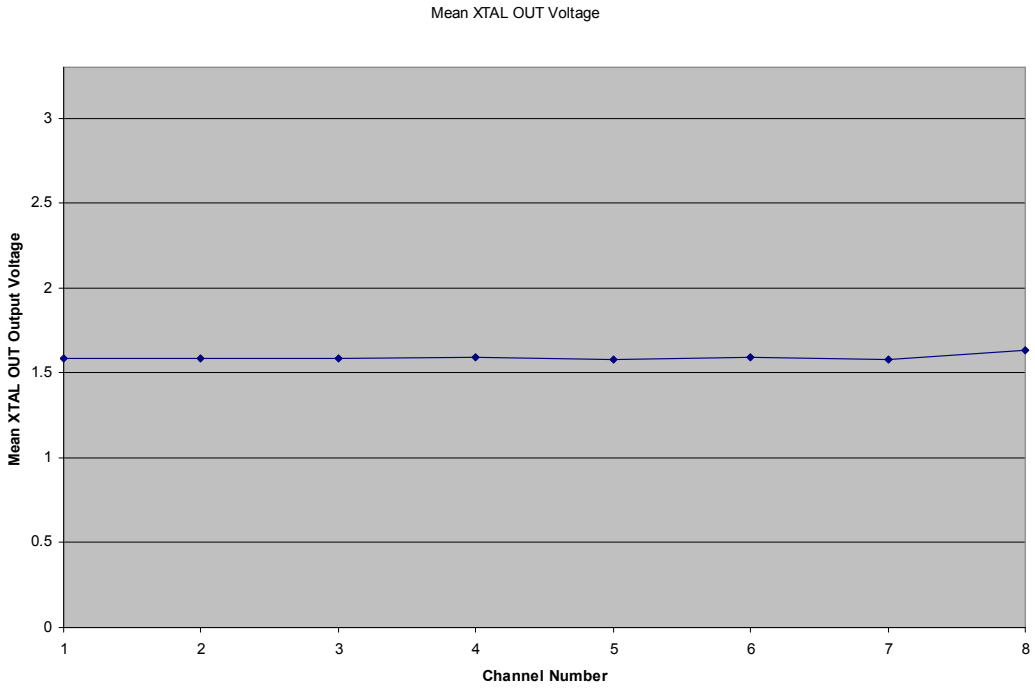

FIGURE 14 - Mean XTAL OUT Output Voltage Versus Channel Number for 1KΩ Terminations

AC Coupling with No External Terminations

With AC coupling and no termination resistors the 27 MHz signal exhibits the same noisy characteristic as for DC coupling. The spectrum analyzer output for channel 1 is shown in FIGURE 15. The spectrum for this output is as expected with a strong spectral line at 27 MHz and much lower spectral content at the second harmonic. However, by the time the signal has propagated to the output of channel 7, the noise is clearly visible on the spectrum just as it was for DC coupling. This is shown in FIGURE 16.

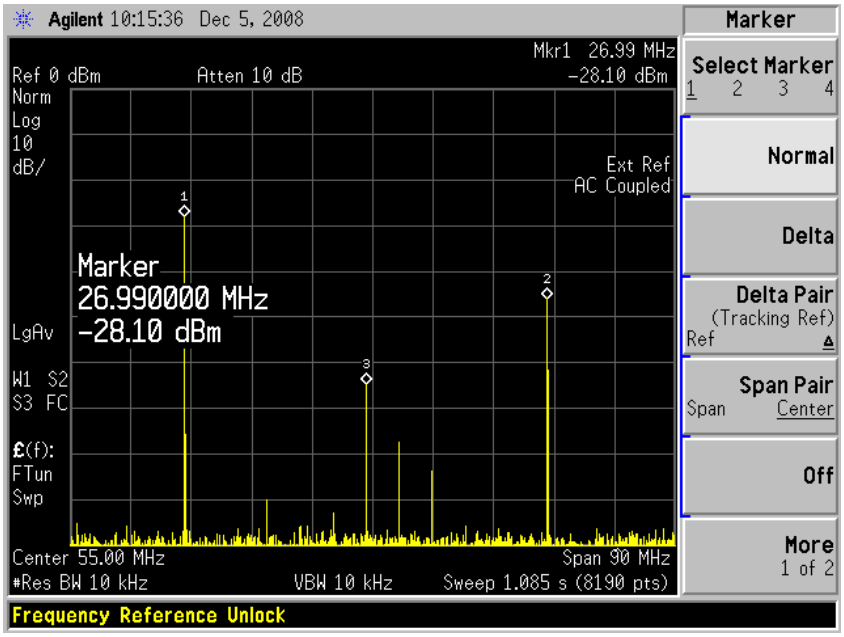

FIGURE 15 - Spectrum Analyzer Measurement of XTAL OUT Output of Channel 1, AC Coupled, No Terminations

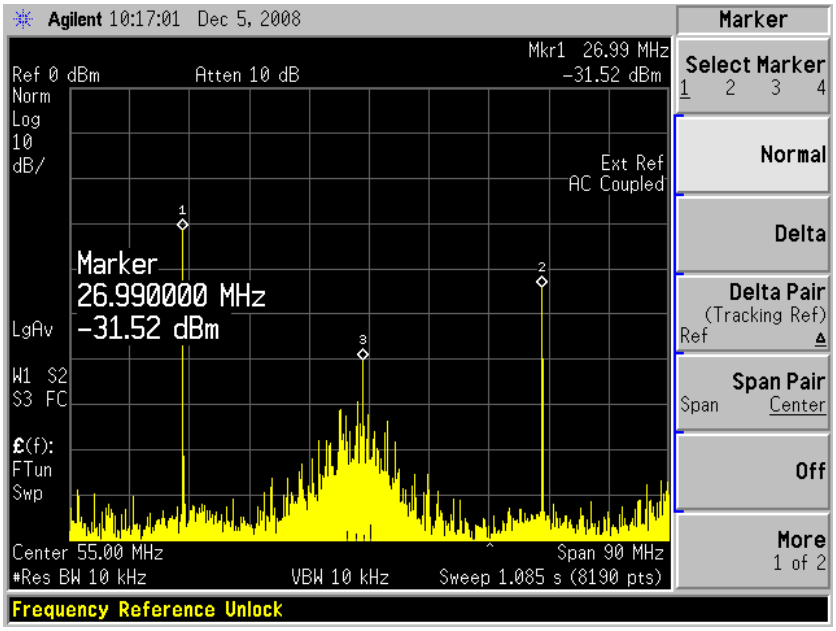

FIGURE 16 - Spectrum Analyzer Measurement of XTAL OUT Output of Channel 7, AC Coupled, No Terminations

AC Coupling with 100Ω Terminations

When the reference signal is AC coupled with 100Ω terminations, the signal amplitude is significantly decreased at the XTAL OUT output of each reclocker. The signal is essentially the same as it propagated from one reclocker to the next.

The output of channel 8 is shown in FIGURE 17. The amplitude of the signal is 260 mV and its mean value is essentially $V_{CC}/2$. The mean value is set by the bias point of the final inverter in the oscillator circuit.

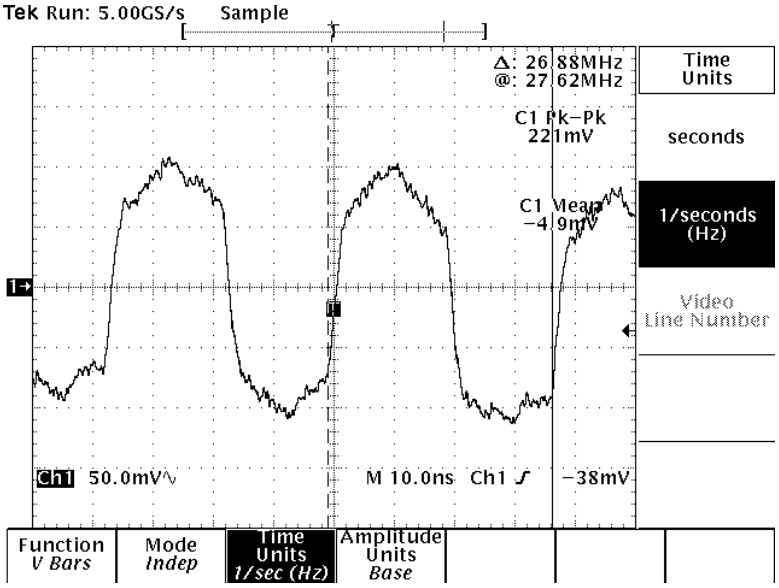

FIGURE 17 - XTAL OUT Output of Channel 8, AC Coupled, 100Ω Terminations. Expanded Scale, Oscilloscope Input AC Coupled

Even though the amplitude of the 27 MHz reference signal at the XTAL OUT output is small, it is sufficient to drive the XTAL IN of the next reclocker in the chain. The disadvantages of using AC coupling with 100Ω terminations are (1) the small output amplitude means that the reference signal is more susceptible to noise and to variations in the switching point of the XTAL IN input; and (2) each reclocker stage uses 16.5 mA of power supply current to set the input common mode voltage. On the other hand, this termination scheme has been verified for 32 reclockers in cascade.

Summary

In order to daisy-chain the 27 MHz reference it is necessary to provide an external termination in order to set the common mode input voltage at each reclocker stage. The termination networks can be realized with large resistors, on the order of 1KΩ, in order to minimize the static DC current drawn from the power supply by the termination networks. The large termination resistors are not well-matched to the PC board transmission line, but this does not degrade the performance if the lines are kept electrically short.

It is not possible to achieve reliable reference clock daisy-chain operation without the termination networks. When the reclockers are DC-coupled without termination networks, common mode offsets build up as the signal propagates from stage to stage until finally the reference oscillator circuitry in a reclocker is unable to toggle. This is accompanied by a buildup of noise in the signal which may interfere with the operation of the reclockers even before the common mode offset stops the reference circuit from toggling.

With AC coupling and no terminations, the common mode buildup may not occur, or it may take many more stages to cause a problem. The noise on the signal builds up in this case, however, just as it does with DC coupling and no terminations. Whether DC or AC coupling is used, the termination networks are necessary.

With the termination networks, both AC and DC coupling between reclocker stages provide reliable operation. AC coupling provides more robust operation. Therefore, the recommended circuit architecture for daisy-chaining the 27 MHz reference signal through a series of reclockers is the AC-coupled, 1KΩ-terminated circuit configuration shown in FIGURE 5.

Bit Error Rate Testing with Reference Daisy-Chain

Using the Agilent J-BERT, a 32 port reference clock cascade was tested for bit errors. This test ran error free for over three days. A single 27 MHz reference was daisy-chained through 32 reclockers on four different 8-channel output cards. The daisy-chaining configuration was the AC-coupled configuration with 100Ω termination resistors.

The J-BERT setup screen is shown in FIGURE 18. The test was run at 2.97 Gb/s. Sinusoidal jitter of 0.5 UI at a jitter frequency of 5 MHz was imposed on the input signal to the first reclocker.

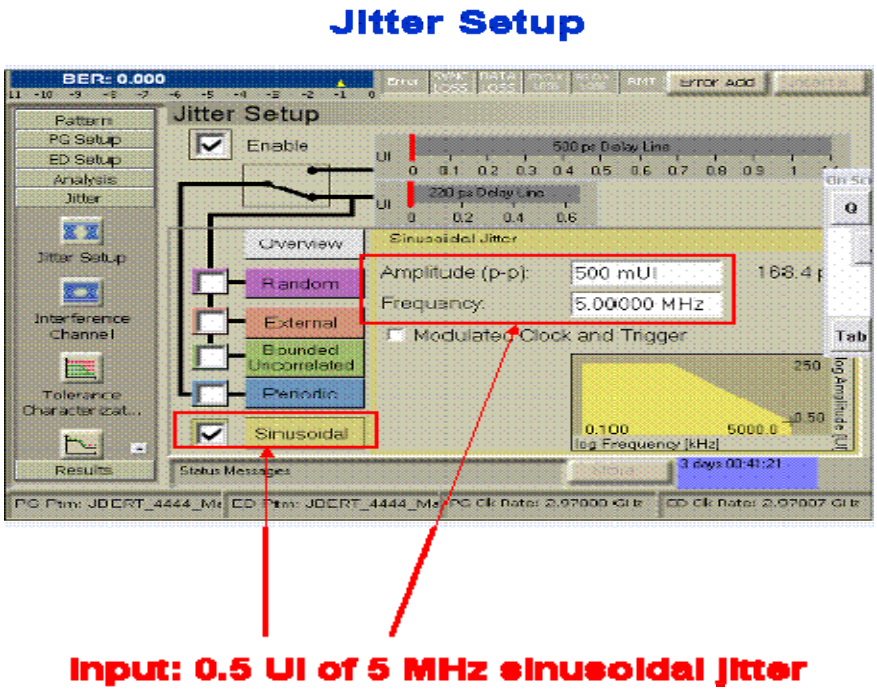

FIGURE 18. J-BERT Jitter Setup for for Cascade of 32 Reclockers' Reference Signals

The J-BERT results screen is shown in FIGURE 19. As the figure indicates, with 32 reclockers sharing a single 27 MHz reference by daisy-chaining the reference signal, the cascade of 32 reclockers provided error-free performance at 2.97 Gb/s during a continuous test for three days.

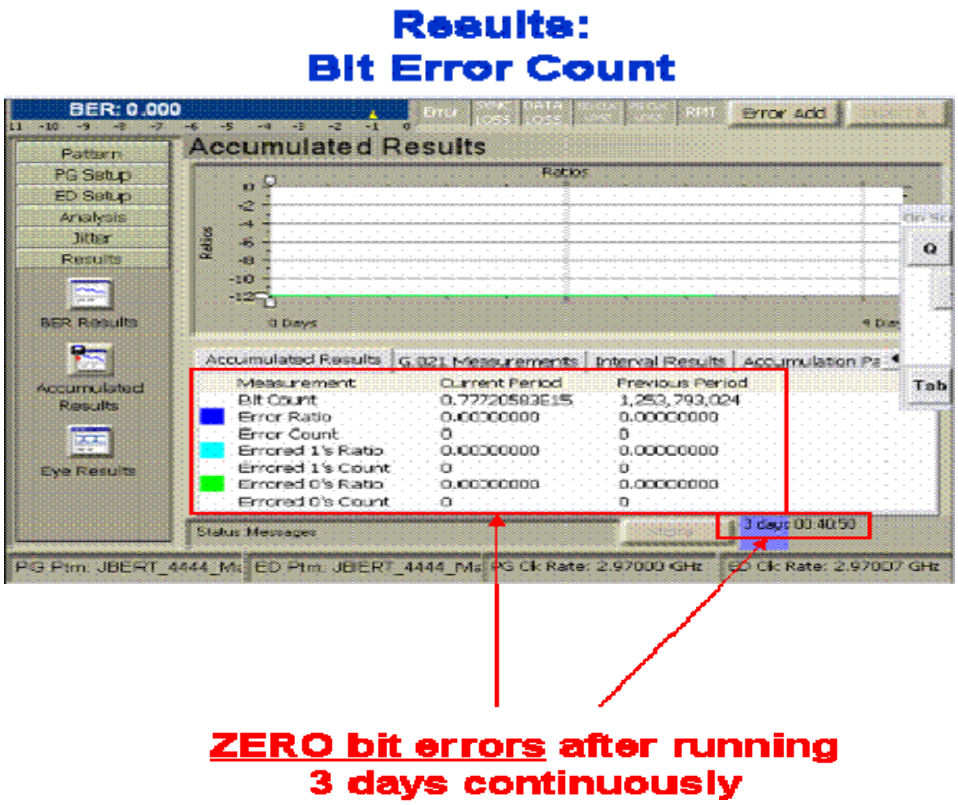

FIGURE 19. J-BERT Results Screen for Cascade of 32 Reclockers' Reference Signals.

Board-to-Board Reference Signal Transmission

The bit error rate test results were achieved with the 27 MHz reference transmitted from one 8-channel output card to the next over a short 50Ω coaxial cable. The cable was driven directly by the XTAL OUT output of the last reclocker on the supplying board and the cable was AC coupled and terminated with two 100Ω resistors at the receiving end. The resistors were in parallel from the point of view of the 27 MHz reference signal, so the effective termination was 50Ω.

Even though this configuration achieved zero bit error operation, the XTAL OUT output of the driving reclocker is heavily loaded by the 50Ω termination. This reduces the amplitude of the 27 MHz reference signal as it comes into the receiving board, which reduces the robustness of the daisy-chain architecture.

Where it is necessary to propagate the reference signal from one board to another over a coaxial cable, it is recommended that a unity gain buffer such as the National Semiconductor LMH6321 be used at the output of the board supplying the reference signal. This device can be configured with a 50Ω series output resistor as shown in National Semiconductor Application Note AN-1461 to provide a matched source for a 50Ω coaxial cable.

When this configuration is used, the XTAL IN input circuit for the **first** reclocker on the board receiving the reference signal should be configured with 100Ω termination resistors. The subsequent reclockers in the chain may be configured with 1KΩ termination resistors as recommended in this document.

Summary

The 27 MHz reference signal required by the National Semiconductor LMH0XX6 family of SDI reclockers can be shared among multiple reclockers by daisy-chaining the reference signal from one reclocker to the next. For reclockers on a single board, the XTAL OUT output of each reclocker may be coupled to the XTAL IN input on the next reclocker using an AC coupling capacitor of 0.1 µF and a termination resistor divider network of two 1KΩ resistors. This configuration is shown in FIGURE 5. This configuration provides stable propagation of the reference clock for a cascade of 8 to 32 reclockers.

For reclockers on different boards, a buffer amplifier should be used to drive a 50Ω coaxial cable to propagate the reference signal from one board to the next. The first reclocker on the board receiving the reference signal should be equipped with a termination network consisting of two 100Ω resistors.

When the 27 MHz reference clock is daisy-chained correctly, it may be shared by many reclockers in cascade. Error-free operation has been demonstrated for a cascade of 32 reclockers using this technique. It is possible that cascades of more than 32 reclockers could be implemented with reference signal daisy-chaining using this technique.

Appendix

The equipment used for the measurements reported in this document is shown in **Error! Reference source not found.**. The oscilloscope measurements of the reference signal were made with the single-ended and differential probes. No significant difference in the signal was noted.

TABLE 2 - Equipment Used in Reference Daisy-Chain Experiments

Equipment Model Number	Description	Measurement Utilization	Comments
Tektronix TDS684B	Real-time Oscilloscope	27 MHz Reference Signal Quality	1 GHz 5 Gsamples/sec
Tektronix P6105A	Passive X10 Oscilloscope Probe	27 MHz Reference Signal Quality	10 MΩ 11.2 pF 100 MHz
Tektronix P6247	Active Differential Oscilloscope Probe	27 MHz Reference Signal Quality	1 GHz 200 KΩ/<1 pF
Agilent E4445A	Spectrum Analyzer	27 MHz Reference Signal Spectrum	3 Hz – 13.2 GHz
Agilent 85024A	High Frequency Spectrum Analyzer Probe	27 MHz Reference Signal Spectrum	300 KHz – 3 GHz
Agilent N4903A	J-BERT Serial Bit Error Rate Test Set	Bit Error Rate Testing	12.5 Gb/s

Revision History

Revision Number	Revision Date	Author	Comments
1.5	October, 2008	Nasser Mohammadi	Initial Release
2.0	December 15, 2008	John Jones	Added experimental data on reference clock coupling
2.1	January 16, 2009	John Jones	Edited for web release

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