



ABSTRACT

This user's guide describes the evaluation module (EVM) for TI's reverse polarity protection controller, LM74501-Q1. This document provides configuration information and test setup details for evaluating LM74501-Q1 devices. An EVM schematic, board layout images, and bill of materials (BOM) are included.

Table of Contents

1 Introduction	2
2 Setup	2
2.1 I/O Connector Description.....	2
2.2 Board Setup.....	3
2.3 Schematic.....	4
3 Operation	5
3.1 LM74501-Q1EVM Performance Capture.....	5
4 EVM Board Assembly Drawings and Layout Guidelines	7
4.1 PCB Drawings.....	7
4.2 Bill of Materials.....	9
5 Revision History	11

List of Figures

Figure 2-1. LM74501-Q1EVM Typical Application Circuit.....	2
Figure 2-2. LM74501-Q1EVM.....	3
Figure 2-3. LM74501-Q1EVM Schematic.....	4
Figure 3-1. LM74501-Q1EVM Startup.....	5
Figure 3-2. Startup Reverse Polarity (–12 V).....	6
Figure 4-1. LM74501-Q1EVM Top Side Placement.....	7
Figure 4-2. LM74501-Q1EVM Bottom Side Placement.....	7
Figure 4-3. LM74501-Q1EVM Top Layer Routing.....	8
Figure 4-4. LM74501-Q1EVM Bottom Layer Routing.....	8

List of Tables

Table 4-1. Bill of Materials.....	9
-----------------------------------	---

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The LM74501-Q1 evaluation module (LM74501-Q1EVM) helps designers evaluate the operation and performance of the LM74501-Q1 reverse polarity protection controller. This evaluation module demonstrates how an N-channel power MOSFET can emulate a very-low forward voltage diode with low I_Q and low-leakage current flowing through the IC. In this design scheme, the LM74501-Q1 is combined with a MOSFET and used in series with a battery as a replacement for a Schottky diode and PFET, in reverse-polarity protection circuitry as shown in Figure 2-1. For more information on the LM74501-Q1 functional and electrical characteristics, see [LM74501-Q1 "TVS Less" Reverse Battery Protection Controller](#) data sheet.

2 Setup

This section describes the jumpers and connectors on the EVM, and how to properly connect, setup, and use the LM74501-Q1EVM. Ensure the power supply is turned off while making connections on the board.

2.1 I/O Connector Description

VIN	J1: Power input connector to the positive rail of the input power supply
GND1	J3: Ground connection for the power supply
VOUT	J2: Power output connector to the positive side of the load
GND2	J4: Ground connection for the load
EN	J5: Jumper to enable LM74501Q1 gate driver 1-2 position connects EN to Source, 2-3 position connects EN to GND
Test Points	VINA, VOUTA, GATE, ENA, BATT_MON, GND1, and GND2 are test points

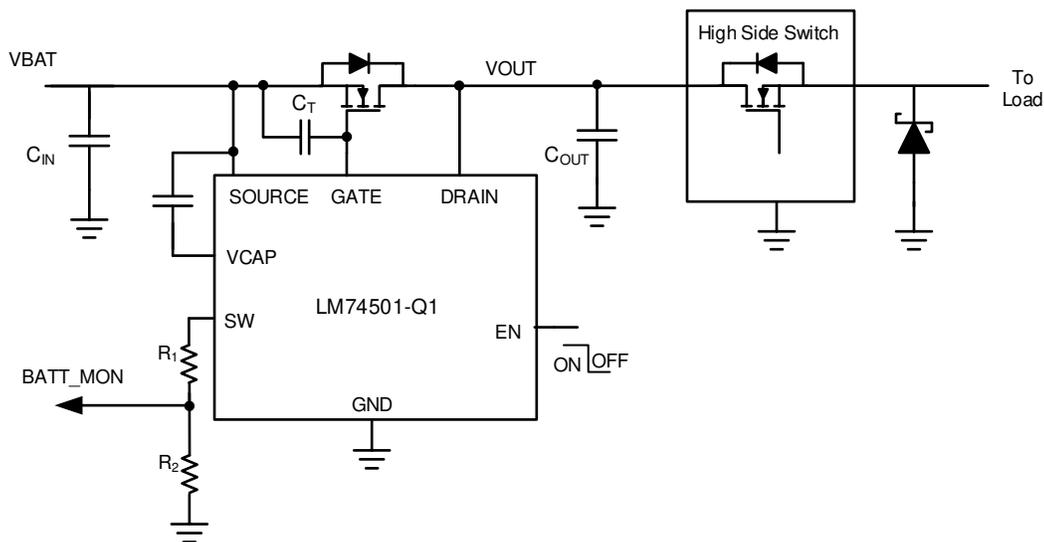


Figure 2-1. LM74501-Q1EVM Typical Application Circuit

2.2 Board Setup

- Before applying power to the LM74501-Q1EVM, verify all external connections.
- Turn off external power supplies and connect them with the proper polarity to the VIN and GND1 connectors.
- An electronic or resistive load must be connected at the output VOUT and GND2 connectors.
- The tests outlined in this document are conducted with 3-A constant current as the load and 12 V at the input.
- Make sure that the external power-supply source for the input voltage is capable of providing enough current to the output load so that the output voltage can be obtained.

When all connections to the LM74501-Q1EVM are verified, apply power to VIN. [Figure 2-2](#) captures EVM board setup.

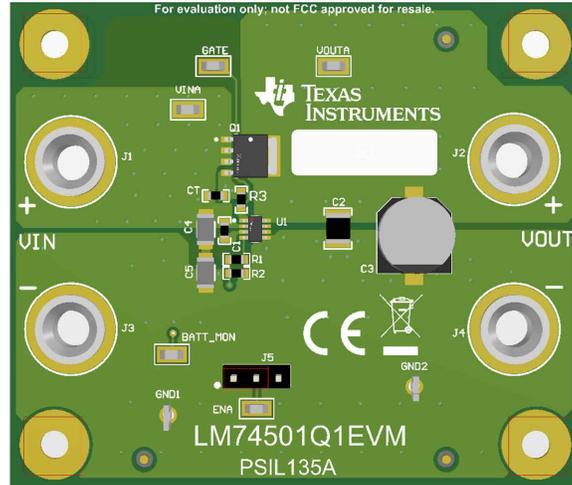


Figure 2-2. LM74501-Q1EVM

3 Operation

3.1 LM74501-Q1EVM Performance Capture

3.1.1 LM74501-Q1EVM Startup

- A startup pulse from 0 V to 12 V is applied at the input of the LM74501-Q1EVM.
- [Figure 3-1](#) shows the input voltage (CH2) rises from 0 V to 12 V and the gate voltage (CH3) comes up after input voltage crosses device PoR threshold.
- The gate of external N-FET is fully enhanced and FET is turned on. Output voltage (CH1) rises smoothly from 0 V to 12 V.

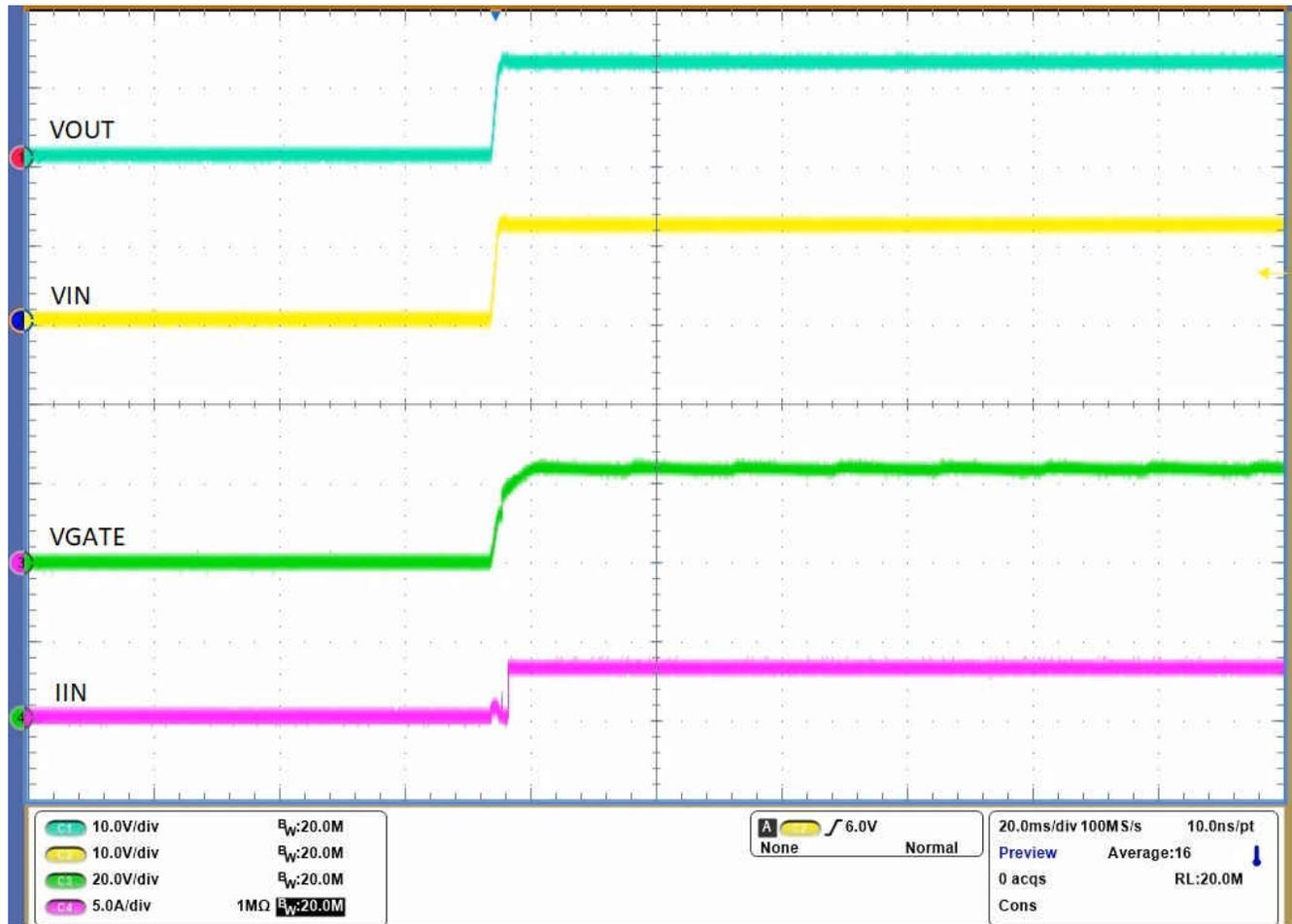


Figure 3-1. LM74501-Q1EVM Startup

3.1.2 Startup Reverse Polarity (-12 V)

- A -12-V source is connected to the VIN input of the LM74501-Q1EVM.
- [Figure 3-2](#) shows that the output voltage remains at a constant 0 V in this situation.
- This test simulates the event of connecting a 12-V battery in the reverse direction; therefore, protecting the load from negative input voltages.

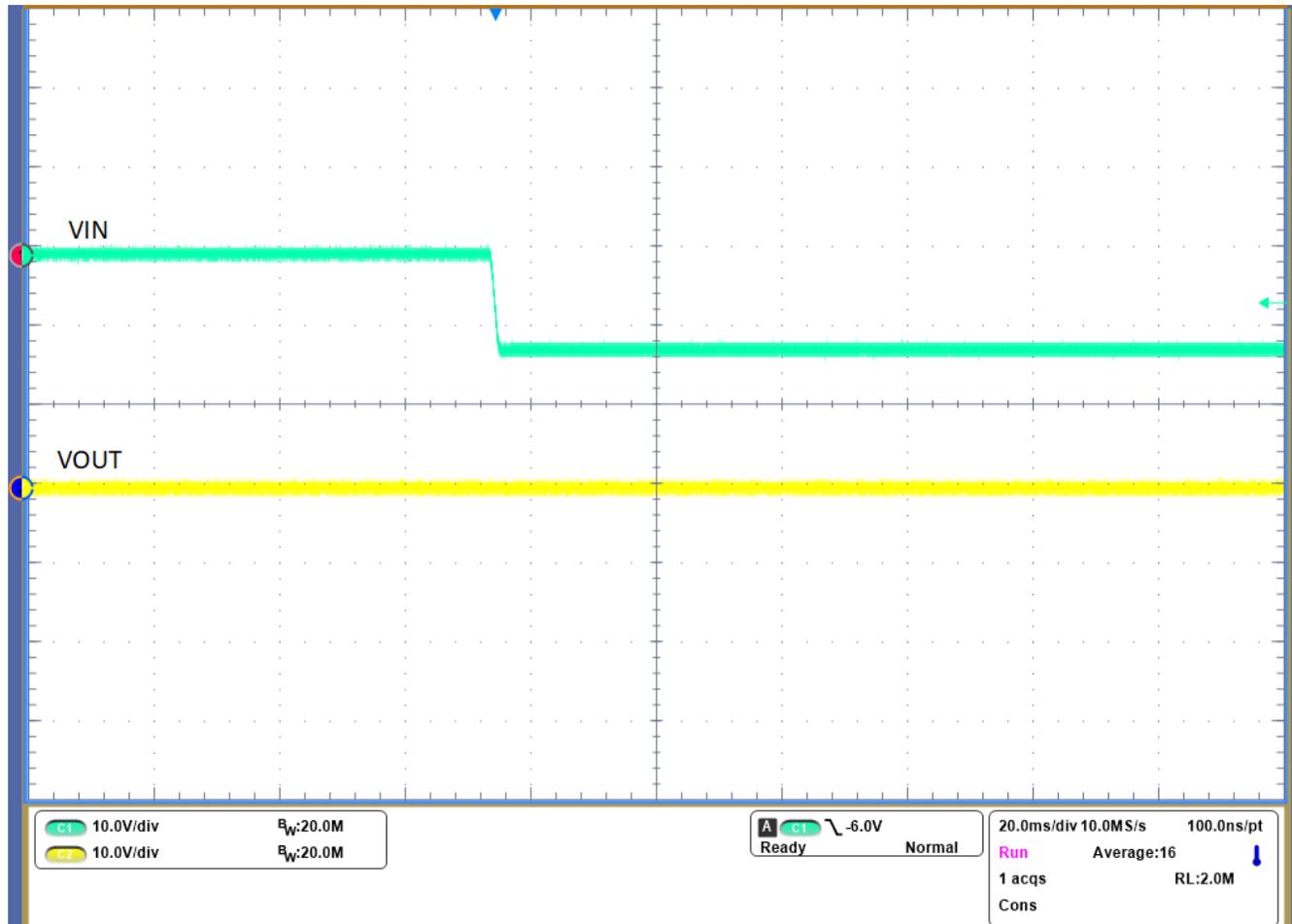


Figure 3-2. Startup Reverse Polarity (-12 V)

4 EVM Board Assembly Drawings and Layout Guidelines

4.1 PCB Drawings

Figure 4-1 through Figure 4-4 show component placement and layout of this EVM.

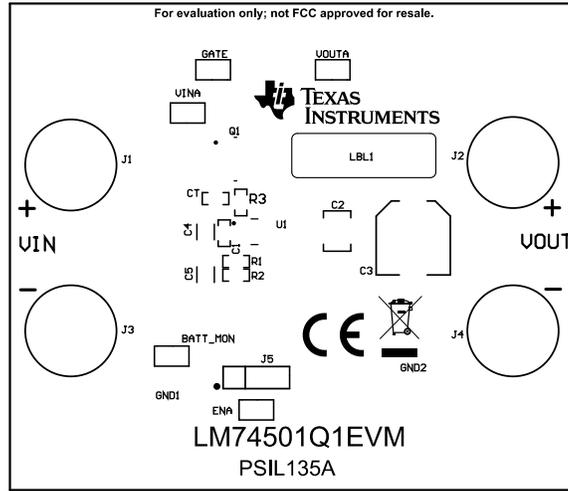


Figure 4-1. LM74501-Q1EVM Top Side Placement

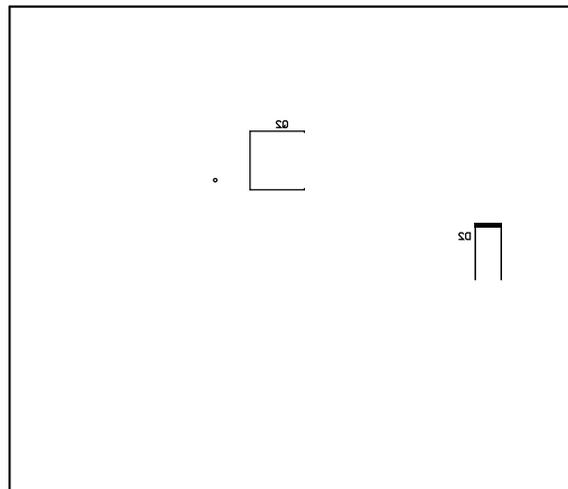


Figure 4-2. LM74501-Q1EVM Bottom Side Placement

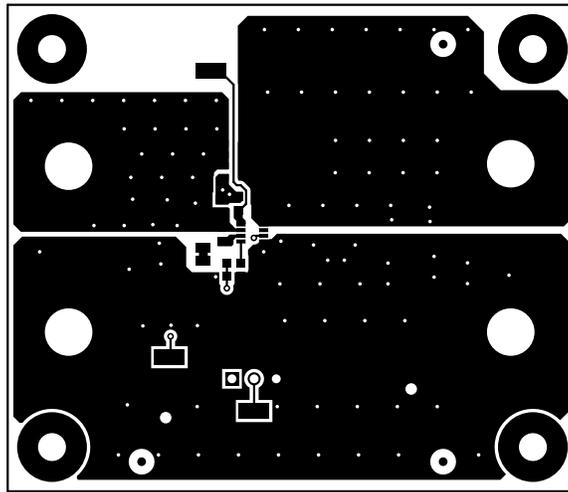


Figure 4-3. LM74501-Q1EVM Top Layer Routing

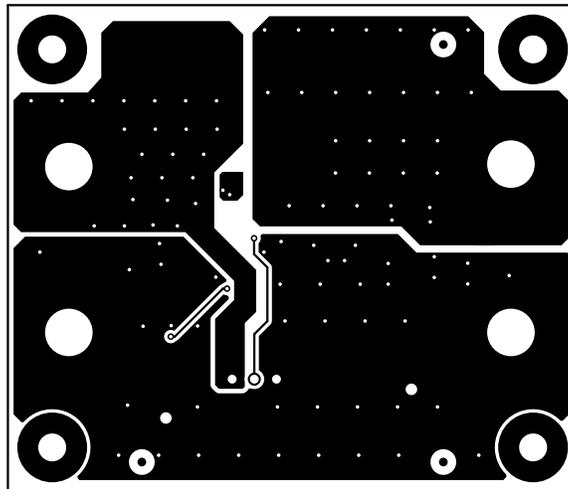


Figure 4-4. LM74501-Q1EVM Bottom Layer Routing

4.2 Bill of Materials

Table 4-1 lists the LM74501-Q1EVM BOM.

Table 4-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		PSIL135	Any
BATT_MON, ENA, GATE, VINA, VOUTA	5		Test Point, Miniature, SMT	Testpoint_Keystone_Miniatu re	5015	Keystone
C1	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R1E104K080A A	TDK
C2	1	2.2uF	CAP, CERM, 2.2 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1,		CGA6N3X7R2A225K230A B	TDK
C3	1	47uF	CAP, AL, 47 uF, 63 V, +/- 20%, AEC-Q200 Grade 2, SMD	D8xL10.2mm	EEE-HA1J470UP	Panasonic
C4, C5	2	0.33uF	CAP, CERM, 0.33 uF, 50 V, +/- 10%, X8R, AEC-Q200 Grade 0, 1206	1206	CGA5L2X8R1H334K160A A	TDK
CT	1	0.022uF	CAP, CERM, 0.022 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R2A223K080A A	TDK
GND1, GND2	2		TEST POINT SLOTTED .118", TH	Test point, TH Slot Test point	1040	Keystone
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2, J3, J4	4		Standard Banana Jack, Uninsulated, 8.9mm	Keystone575-8	575-8	Keystone

Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J5	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1	1		N-Channel 40V 120A (Ta) 172W (Ta) Surface Mount LFPK56, Power-SO8	SOT669	BUK7Y3R0-40HX	Nexperia
R1	1	91k	RES, 91 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060391K0JNEA	Vishay-Dale
R2	1	9.1k	RES, 9.1 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06039K10JNEA	Vishay-Dale
R3	1	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
U1	1		Low IQ Reverse Battery Protection Controller with Integrated VDS Clamp	SOT23-8	LM74501QDDDFQ1	Texas Instruments
D2	0	58V	Diode, TVS, Uni, 58 V, SMA	SMA	SMAJ58A	Diodes Inc.
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
Q2	0		N-Channel 40V 100A (Tc) 136W (Tc) Surface Mount TO-252AA	TO-252	SQD100N04-3M6_GE3	Vishay

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (September 2021)	Page
• Updated Figure 2-2	3
• Updated Figure 2-3	4
• Updated Figure 4-1 through Figure 4-4	7
• Updated Table 4-1	9

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated