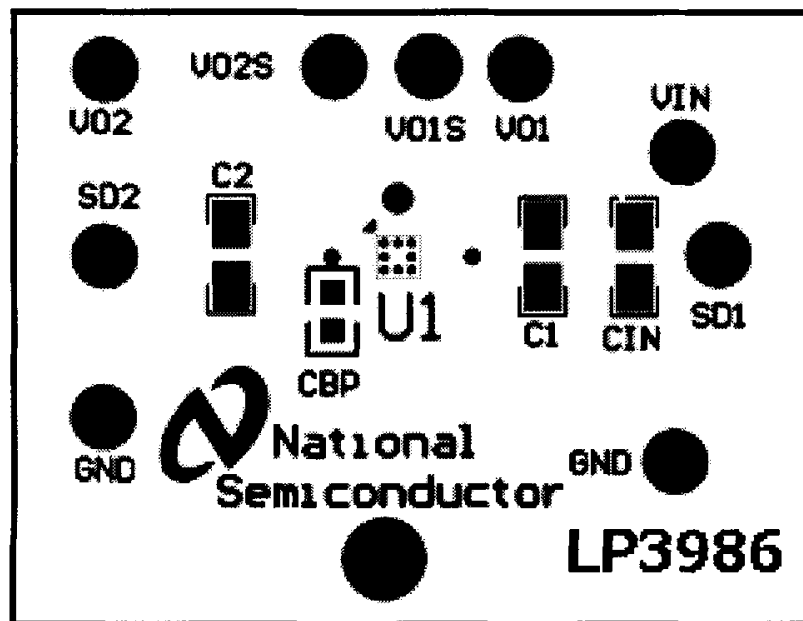
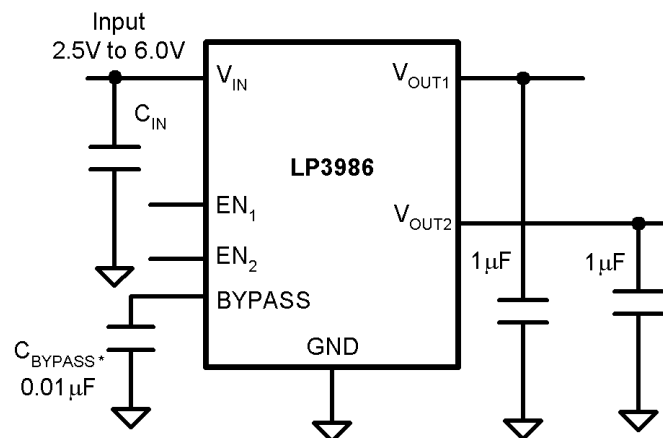


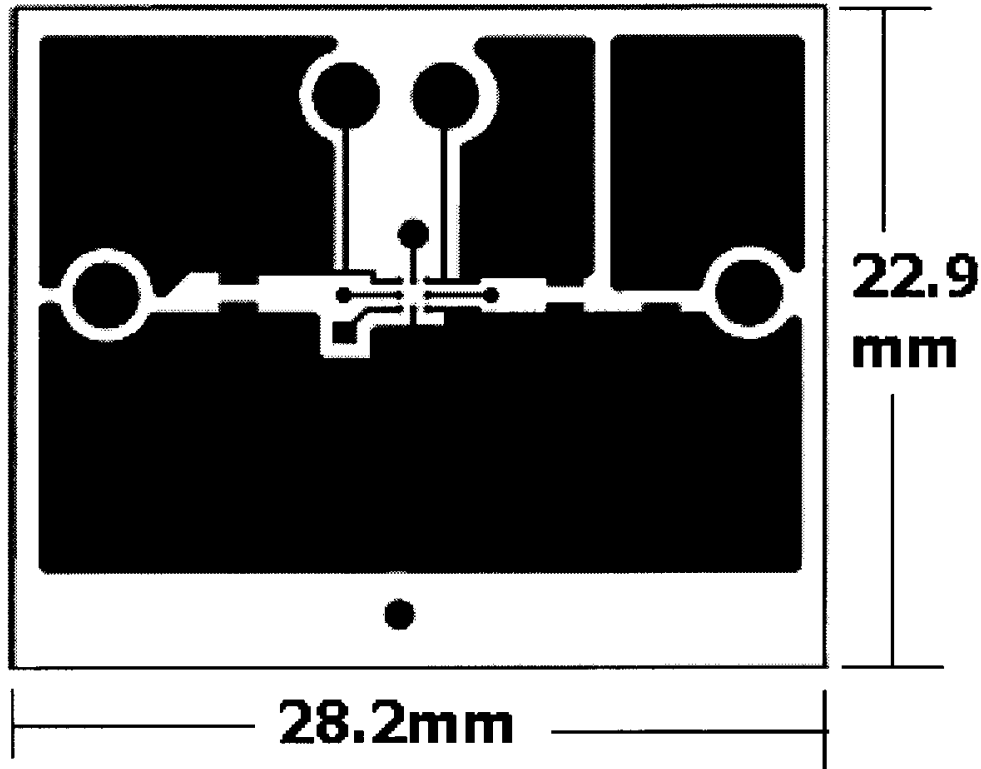
## AN-1228 LP3986 DSBGA Evaluation Board Instruction

### 1 Introduction

This evaluation board is designed to enable independent evaluation of the LP3986 electrical performances. Each board is assembled and tested in the factory. This evaluation board instruction is for the DSBGA-8 large bump package.

The schematic and layout of the evaluation board are shown below:





The LP3986 is a dual micropower CMOS voltage regulator designed for portable and wireless applications with demanding performance and space critical requirements. The LP3986 can deliver up to 150 mA current per output and it can be enabled and disabled independently via the SD1(EN1) and SD2(EN2) pins. The 0.01  $\mu\text{F}$  bypass capacitor is optional; but if used, it will reduce noise on the regulator output.

The input sense and output sense pins are used for more precise voltage measurements. These pins are connected to the LP3986 input and output via high impedance traces.

Table 1 shows the bill of material (BOM) for the LP3986 DSBGA-8 board.

**Table 1. Bill of Materials**

Designator	Value	Amount	Footprint	Note
CB	0.01 $\mu\text{F}$	1	0805	Taiyo Yuden
C <sub>IN</sub>	1 $\mu\text{F}$	1	0805	Taiyo Yuden EMK212F105ZG
C <sub>OUT1</sub> and C <sub>OUT2</sub>	1 $\mu\text{F}$	2	0805	Taiyo Yuden EMK212F105ZG
U1	LP3986-xxyy	1	YZR0008	The "xx" corresponds to the appropriate LDO output V <sub>OUT1</sub> and yy corresponds to V <sub>OUT2</sub> such as 2.52.8, 2.92.9, and so forth.
VO1, VO2, SD1, SD2, VIN, GND and GND <sup>(1)</sup>	Test pins	7		Keystone 1040

<sup>(1)</sup> SD1(EN1) and SD2(EN2) are not connected electrically on the evaluation board. It is left for the you to connect the SD1 and SD2 to V<sub>IN</sub> when needed.

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