

# ***AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs***

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## **ABSTRACT**

Of all the voltage regulator control strategies ever devised, the hysteretic regulator is probably about the simplest. This control methodology simply turns a switch on when the output voltage is below a reference and turns the switch off when the output rises to a slightly higher reference. The output ripple is therefore a direct function of the difference between the upper and lower reference threshold, the hysteresis amplitude. It's hard to imagine something much simpler and, as usual, with simplicity comes performance shortcomings.

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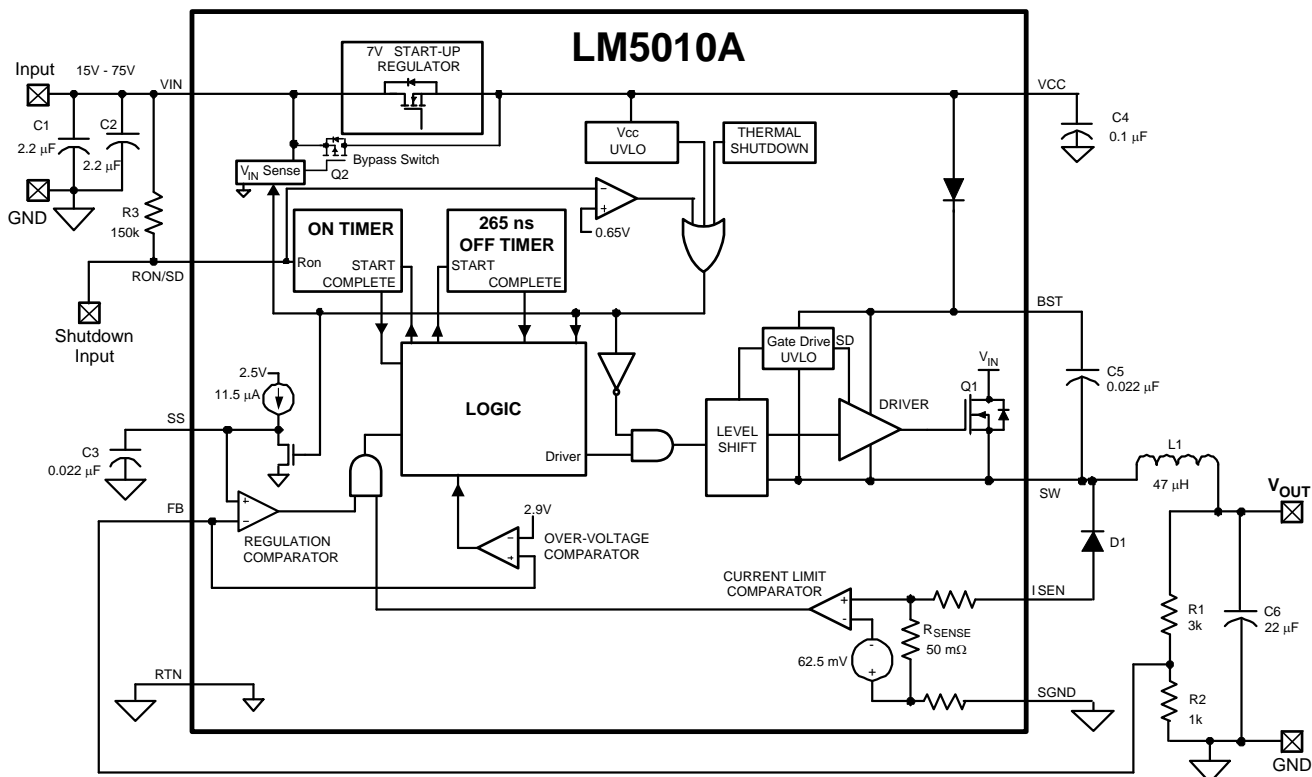
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## 1 Introduction

A major disadvantage of the hysteretic architecture is a very large variation in switching frequency as the input voltage varies. An attempt to improve this situation called constant on-time control (COT) provides dramatically better frequency control while only adding a very modest increase in complexity. A one-shot timer is inserted into the signal path. The period of the one-shot is an inverse function of the input voltage. The on-time programming requires only a single resistor to  $V_{IN}$ . Deep down underneath it all, it's still a hysteretic control circuit however, and it therefore still has a need for some ripple voltage at its feedback pin. The upper threshold is eliminated, being replaced by the programmed on-time. But the lower threshold still requires the output voltage to have enough ripple to be able to distinguish the falling output turn-on point.

Unfortunately, this required ripple component can get larger than desired in some cases and, if using all ceramic output capacitors, will be phase shifted by 90 degrees to the desired timing relationship to the main switch. What follows is a collection of circuits that address these problems and can allow dramatically lower output ripple in addition to complete ESR independence in some cases, with only a very slight increase in circuit complexity.

The LM5010A is shown throughout the examples below, but the same circuit tricks will work with any of TI's COT regulators including the LM5007, LM5008, and LM5009 and should, at least in principle, work with pure hysteretic designs as well. Some of the more recently introduced parts like the LM3100 incorporate the kinds of methodologies outlined here internally, in order to achieve ESR independence. The circuits that follow were configured for a nominal 10 V out at 1.25A with an input range of 15 to 75 V. Most of the testing was done with 30 V in.



**Figure 1. Typical LM5010A Application Circuit**

Figure 1 shows an LM5010A block diagram and typical application circuit. Note the On-Timer block with its programming resistor, R3. This resistor sets the operating frequency by determining the on-time based on the input voltage. The regulation comparator looks at the output voltage through the feedback divider consisting of R1 and R2. This circuit will function correctly as long as the output capacitor, C6 has sufficient ESR to look resistive at the switching frequency. An aluminum electrolytic capacitor with roughly 1.5  $\Omega$  of ESR will work nicely.

The LM5010A regulates the bottom of the output ripple triangle as seen at the feedback divider at 2.5 V nominally. When  $V_{OUT}$  decays below this level a programmed on-time is initiated that forces the output higher and the FB pin voltage a bit above 2.5 V. This process repeats. The switching frequency and output ripple are therefore controlled by the programmed on-time. Programming a longer on-time will reduce the switching frequency and increase the output ripple, all other things being equal. If the output capacitor is made extremely large with proportionally lower ESR there will be very little signal in the form of output ripple and the circuit will become rather noise sensitive due to the feedback signal's low signal to noise ratio. A similar problem arises if a very low ESR ceramic capacitor is used due to the low signal amplitude and the fact that the desired information will get phase shifted by 90°.

Figure 2 was shot with a 22  $\mu\text{F}$  ceramic output capacitor in series with a 1.5  $\Omega$  resistor. This provides for a finite and well controlled ESR. The switcher is quite stable and well behaved but the output ripple is approximately 500 mV pk-pk on a 10 V output.

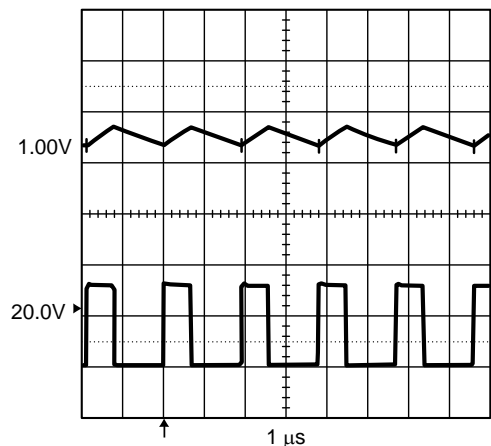


Figure 2. Output Ripple and Switch Node Voltage With 22  $\mu\text{F}$  Output Cap and 1.5  $\Omega$  ESR

In many cases, this can be a perfectly acceptable result and the design can be considered completed. But what happens if the 1.5  $\Omega$  is eliminated in an effort to reduce the ripple? Figure 3 shows the disappointing results of doing this.

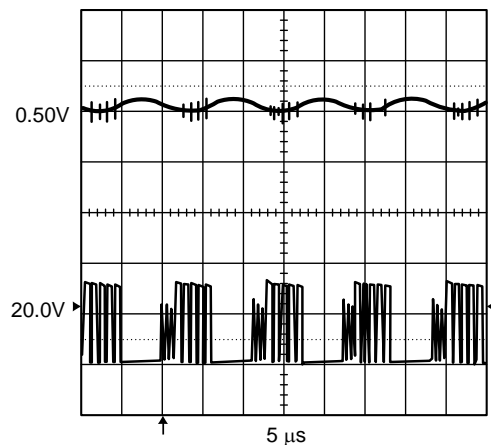


Figure 3. Output Ripple and Switch Node Voltage With 22  $\mu\text{F}$  Output Cap and Zero ESR

Notice that the switching pulses come in bunches and the ripple looks nearly sinusoidal. The ripple amplitude has been cut approximately in half, but at the expense of proper operation. A look at the circuit design provides the first clue as to where to start the improvement process. Note that the R1/R2 divider is used to provide feedback to the regulator and set the desired output voltage. The reference voltage for the regulator depicted here is 2.5 V so there's a 4:1 divider for a 10 V output. This divider attenuates the ripple voltage as well as the DC level and therefore reduces the available AC signal to the control circuit. If the top divider resistor, R1, is bypassed with a capacitor that's a low impedance relative to R1 at the switching frequency, a significant improvement in AC signal is obtained while having no effect on the DC regulation. Setting the break frequency at roughly 1/10 of the switching frequency is a good place to start. With a 500 kHz switching frequency, that implies a 50 kHz cutoff frequency for the RC, so  $C = 1/2\pi RF$ . With R1 at 3 k $\Omega$  the capacitor value calculates to approximately 1000 pF. Since this will give a 4X increase in the AC feedback signal you should in theory be able to reduce the ESR by a factor of 4 and get proper operation again. That translates to an ESR of 375 m $\Omega$ . The revised circuit is shown in [Figure 4](#):

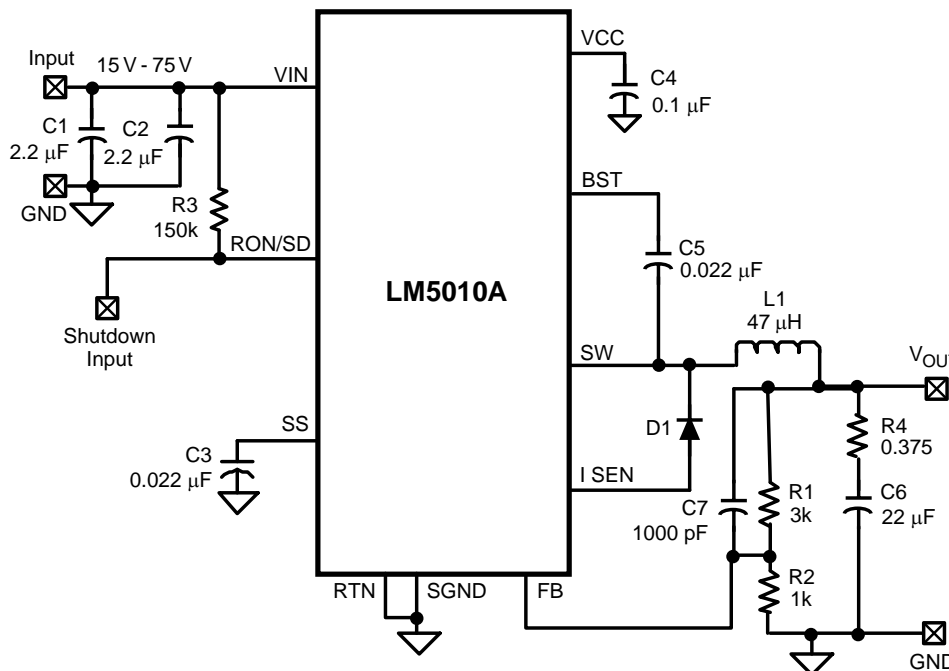


Figure 4. 375 m $\Omega$  ESR Design. Note the Addition of C7.

[Figure 5](#) shows the results are about as predicted. Ripple is down to approximately 150 mV pk-pk and the switching frequency is nearly the same as in the prior example.

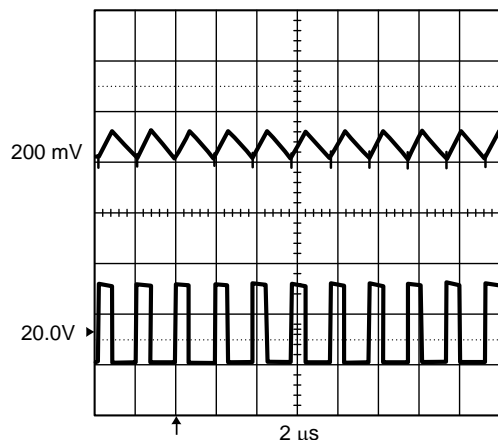


Figure 5. Output Ripple and Switch Node With ESR = 375 m $\Omega$  and C7 Added

Something to pay close attention to on designs that depend on the filter cap's ESR for proper operation is the effect of additional capacitance located at the load. In general, as long as the additional capacitance is a few inches from the regulator's output capacitor, there will be sufficient lead inductance isolating the two parts that operation will not be adversely effected. Here's an example of adding a 10  $\mu\text{F}$ , 35 V, 125 m $\Omega$  ESR tantalum capacitor approximately 1 inch from the main output capacitor. As you can see, the ripple is now down to approximately 35 mV pk-pk.

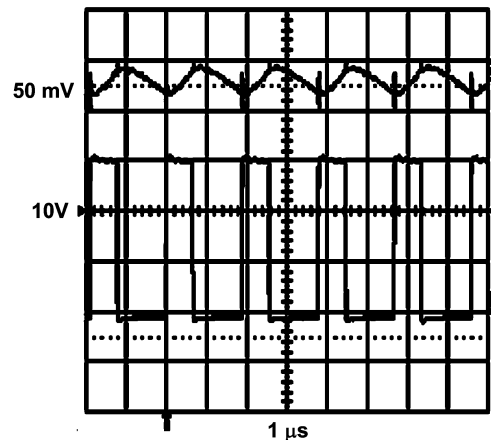


Figure 6. Adding a 10  $\mu\text{F}$  Tantalum Capacitor at the Load

Adding a fairly large ceramic capacitor close to the output capacitor does have the potential to cause problems. Here's what happened to the circuit when a 2.2  $\mu\text{F}$  ceramic was connected close to the output:

The switching pulses are starting to bunch up again. Placing the additional filter capacitor effectively in parallel with the ESR of the main output capacitor is causing the problem. If the corner frequency of the added capacitor and the main output capacitor's ESR is near the switching frequency of the regulator, the effective ESR starts to get reduced and the ripple the control circuit "sees" becomes attenuated. Only if you can guarantee sufficient trace inductance to effectively isolate the additional capacitance from the main output capacitor, will normal operation be ensured. Of course, it's difficult to know for sure that this will be the case. Another possible solution to the problem is to configure the circuit as shown in [Figure 8](#).

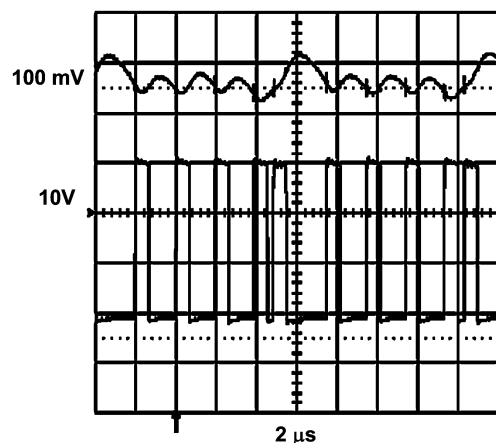


Figure 7. Ripple Voltage and Switch Node With a 2.2  $\mu\text{F}$  Ceramic Capacitor at the Load

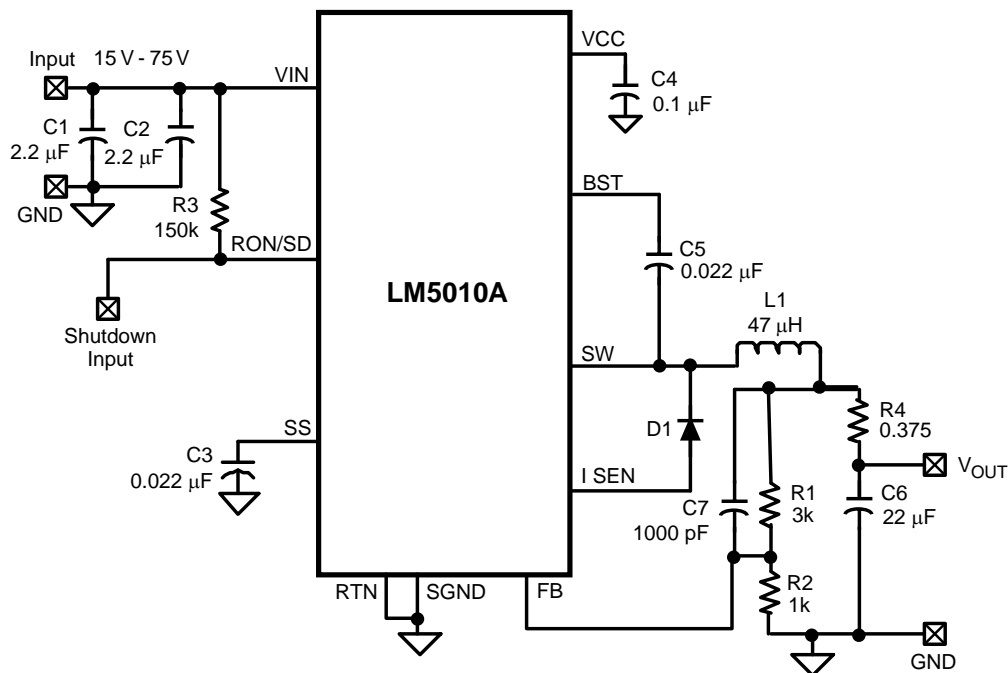


Figure 8. Adding 375 mΩ in Series With the DC Current Path

In this case, the 375 mΩ resistor, R4, is in series with the DC output current path. The ripple on C6 will be very small and in fact can be made arbitrarily small by making C6 larger, if desired. The downside is that the feedback is now taken up stream of R4 so the load regulation is substantially degraded and significant power is dissipated in R4. When used in conjunction with C7, however, the magnitude of these issues can be kept reasonably small for relatively high output voltage designs. In the example shown here for a load change from zero to 1.0A the output voltage droops roughly 400 mV. But the ripple is now down to a little over 10 mV pk-pk. This circuit is completely immune to adding more filter capacitance at the load, regardless of the trace inductance of the interconnect.

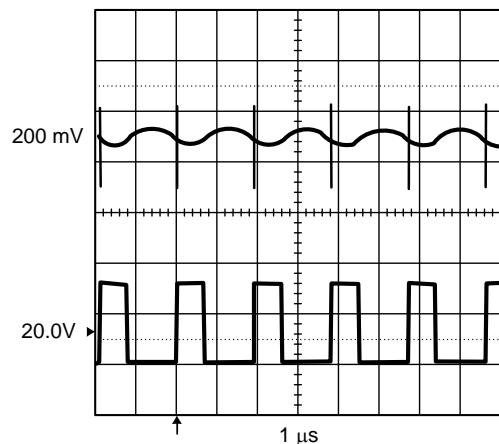


Figure 9. Ripple Voltage and Switch Node With 375 mΩ in Series With the DC Current Path

The resulting ripple waveform is shown in Figure 10.

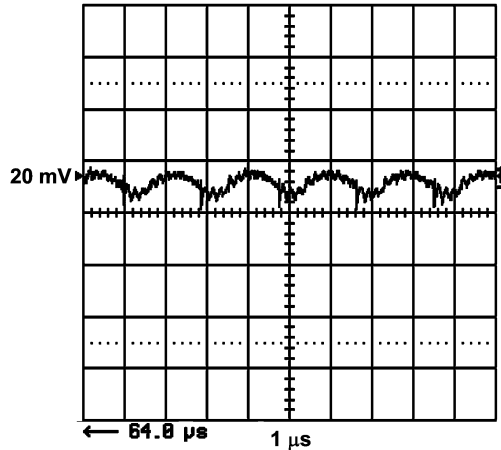


Figure 10. Ripple Voltage With Feedback Ripple Synthetically Generated

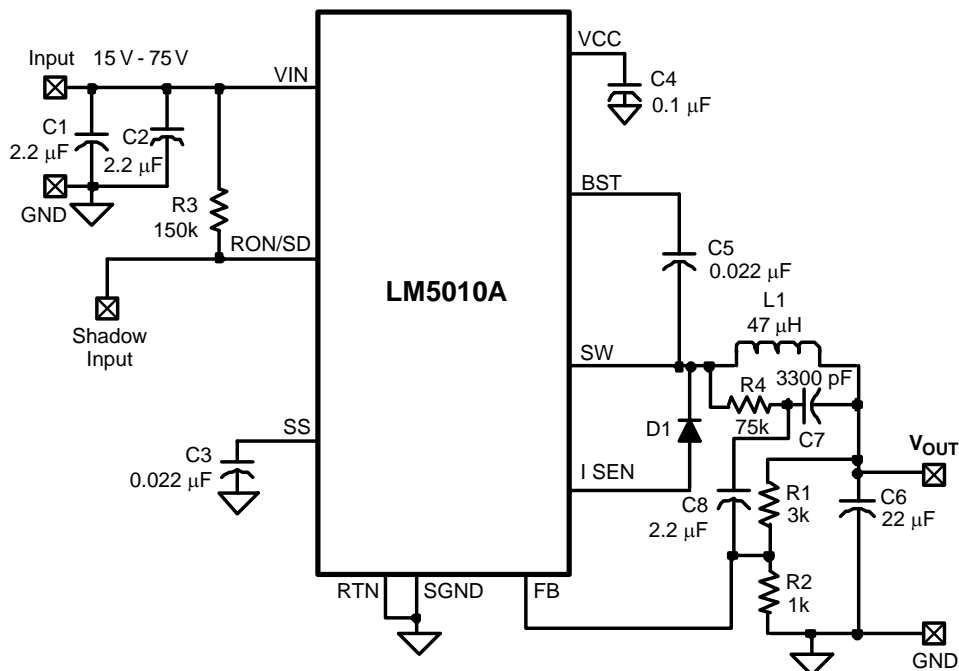


Figure 11. Artificial Ripple Generation

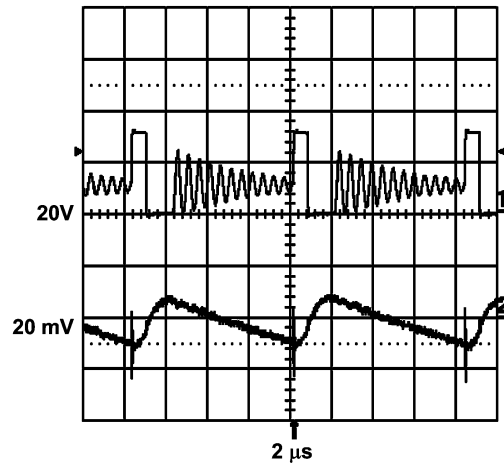
Artificially generating the desired ripple information and feeding it to the controller to fool it into seeing what it expects to see is probably the best solution. This allows the output ripple to be made arbitrarily small and still have the circuit function correctly. There's no degradation of the load regulation and no additional resistance in the power path. The R4, C7, and C8 network in [Figure 11](#) form a triangle wave generator that provides the desired information to the FB pin. It does this by integrating the voltage across the inductor with R4 and C7, and AC coupling the resulting signal to the Feedback pin through C8. One way to think of this is that the inductor integrates the voltage impressed across it to produce a triangular current waveform. The resulting current flows through the ESR of the output capacitor producing a triangular voltage waveform for the feedback. The RC circuit shown here does a very similar thing. The capacitor, C7, integrates the current through R4, which is proportional to the voltage across it. This is the same voltage that appears across the inductor. As far as the feedback circuit is concerned, these are exactly the same thing. The ESR resistor from the previous circuits has been completely eliminated so the only ESR in the circuit is that of the 22  $\mu$ F ceramic capacitor. This would leave a total ESR on the order of 10 m $\Omega$  or so.

The ripple is now on the order of 15 mV pk-pk. Notice too that the measured spike level is also somewhat reduced compared to the previous measurements. This is merely due to the fact that the switch node measurement has been removed. The additional scope probe connected to a noisy signal source was radiating energy that had been subsequently picked up by the ripple measurement probe. It's a good practice to use a single probe when trying to make very accurate ripple measurements. Line regulation over an input range of 15 V to 50 V is measured at approximately 20 mV. This design is completely impervious to additions of large amounts of output capacitance. It requires zero ESR and will always remain well behaved. If the environment is noisy or the layout sub-optimal you simply reduce the time constant of the integrator and produce a bit more signal. Note that this will cause a slight change in the nominal output voltage due to the fact that the bottom, not the average of the ripple triangle is being regulated. If desired, the feedback divider ratio can be adjusted slightly to compensate.

The design procedure for this technique is fairly simple. The impedance of the integrator capacitor should be small compared to the feedback divider impedance at the desired switching frequency. Since the divider in this case is a bit under 1000  $\Omega$  (1000  $\Omega$  in parallel with 3000  $\Omega$ ) the impedance for C7 was chosen to be roughly 100  $\Omega$  at 500 kHz. That calculates to around 3300 pF. Since  $V_{IN} - V_{OUT}$  is very large compared to the ripple voltage being produced you can think of the resistor R4 as being a current source. The current is simply  $(V_{IN} - V_{OUT})/R4$ . The desired ripple voltage was somewhat arbitrarily chosen to be 50 mV pk-pk. A charging capacitor obeys the following:  $I/C = dV/dt$ . At 30V in the on time is roughly 650 ns. The dV term is the 50 mV ripple, and C is 3300 pF. Solving for I yields approximately 250  $\mu$ A.  $R = (30 V - 10 V)/250 \mu A$  so use  $R = 75 k\Omega$ . The AC coupling cap should be 3 to 4 times larger than the integrator so a 0.01  $\mu$ F was chosen. None of these values are very critical.

One thing to observe is that the ripple can grow somewhat when the load gets light enough to force discontinuous conduction mode operation (DCM). In this case the pk-pk ripple approximately doubles at 40 mA out and will increase to about 25 mV pk-pk at zero load. The upper trace is the switch node in DCM. The relatively high frequency ringing is the inductor resonating with the parasitic capacitance on the switch node. This capacitance consists of the diode capacitance, the high-side switch output capacitance, and any stray capacitance associated with the PCB layout. It is completely normal and expected in any regulator operating in DCM.





**Figure 12. DCM Operation**

## 2 Conclusion

It has been shown that a constant-on-time based regulator design is capable of delivering low output ripple while still maintaining much of the original simplicity. COT based regulators with no requirement for output capacitor ESR are quite practical, and the resulting designs are completely free of stability concerns due to large capacitive loads. Performance similar to much more complex clocked PWM systems is attained with none of the added design effort associated with feedback loop stabilization.

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