LP2995

DDR-SDRAM Termination Simplified Using A Linear Regulator

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Application Brief

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With the advent of DDR-SDRAM as the industry standard for memory in desktop computers, laptops and videocards, power management has become a focal point for system designers. Active termination of bus interconnects has required the use of another regulator, increasing cost and system complexity. To specifically address this issue, National Semiconductor has just released the LP2995 DDR Termination Linear Regulator, offering a linear topology in a marketplace dominated by switchers. The implementation of this architecture has been made possible by careful examination of the system requirements. It is the intent of this article to illustrate the actual requirements of DDR-SDRAM termination and compare the two solution topologies.

With the memory migration from SDRAM to DDR-SDRAM, higher bus speeds and data transfer rates are attainable. As a consequence of the increased bandwidth, transmission problems have begun to appear. The length of the memory interconnects, coupled with the multiple stubs that are required for supporting DIMMs result in signal reflection causing data corruption. This problem has required more attention as speeds have increased from DDR200 (100 MHz clock) to DDR266 (133 MHz clock) to the newly released DDR333 (166 MHz clock). Concerned with the integrity of the signals at these high frequencies, JEDEC sought to create an industry standard for low voltage, high speed signaling as an improvement over LVTTL. The result was an active termination scheme called SSTL (Stub Series Termination Logic).

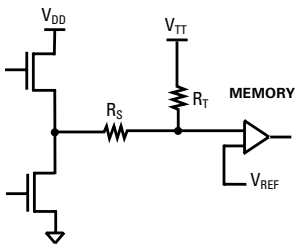

Figure 1: Implementation of SSTL

The JEDEC definition of SSTL-2 for 2.5V memory called for an active termination using a V_{TT} output voltage. This voltage is required to track a reference, V_{REF}, which is created by dividing the memory power rail exactly in half. With the JEDEC specification defining the voltage tolerance on the individual rails, power delivery calculations have been left to the system designers. It is easily identifiable that V_{TT} needs to sink and source current, the problem is determining the magnitude. Historically, numbers were generated based on a macroscopic viewpoint of the system using static worst case conditions. These approximate calculations defined the solution, by stating the following requirements:

- V_{TT} must sink and source current
- Maximum output current is 3A

Based on this definition, only one clear choice existed: a synchronous switcher had to be used. To meet these exacting requirements a plethora of switchers were designed to tackle this exact application from various manufacturers. The end solution was typically a synchronous PWM buck controller. A representation of a typical circuit implementing this topology can be seen in *Figure 2.*

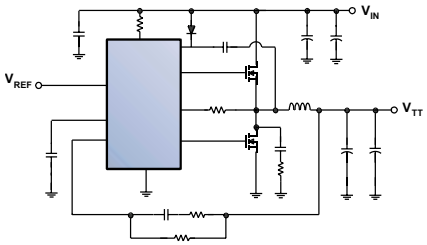

Figure 2: Synchronous PWM Switcher Topology

The synchronous buck switcher, while providing a feasible solution does not present an ideal or even optimal DDR termination regulator. Limitations exist that are inherent with the topology and the practical implementation. Several examples include:

Board Space: Due to the complexity of this solution, a controller with high pin count is required to drive two external MOSFETs. Coupled with an inductor and the associated capacitors this implementation can occupy a significant amount of board area. This can be extremely critical in laptops and videocards where real estate is at a premium.

Cost: The high component count required for the application translates directly into increased cost.

Performance: The most fundamental requirement for any DDR termination regulator is performance. While the task of creating a 1.25V reference signal within a ±200 mV window is trivial, the challenge in designing a switching power supply is limiting the switching noise and EMI. Signal interference resulting in data loss is possible if switching harmonics are present on the bus. Though not impossible to limit, it poses an increase in cost and development time to reduce the effects.

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The initial assumption that 3A were required for the maximum output current, resulting in the selection of the buck switcher, was actually an oversight. The cause of this problem was that the worst case conditions were incorrect resulting in over design of the regulator. To counter this problem, National Semiconductor approached the power delivery calculations from a memory architecture and control point of view to define an entirely new solution. From an in-depth analysis of the PC memory it becomes apparent that 3A are not required. The exact analysis is not included in this article due to length, however, several of the key points have been highlighted:

- DDR-SDRAM is a dynamic system, static assumptions of a 133 MHz clock (266 MHz data rate) are not realistic when applied to the regulator requirements.
- Theoretical peak calculations are not obtainable for sustained durations. Data cannot be clocked every edge indefinitely. Delays such as CAS latencies are an important assessment in every memory access.
- Significant current cancellation can occur from complementary signals such as data strobes.
- Two line conditions are insufficient for a complete model, tri-stating and transitional periods need to be incorporated.
- Even periodic refresh affects the average output current required by the regulator.

Coupled with technical analysis, confirmed by empirical measurements, National Semiconductor found that the average currents required are closer to 200 mA. Worst case conditions, simulated by intensive memory burn-in tests, result in little deviation from this figure. This new design target meant that an entirely new topology can be used: **LINEAR**, bestowing all its advantages.

Leveraging the results found from the measurements, National Semiconductor addressed the shortcomings of the switcher topology and created a new standard in DDR bus termination by releasing the LP2995. The LP2995 utilizes an exclusive linear topology to create the V_{TT} output voltage and the reference output, V_{REF}, for the chipset and DIMMs. A typical application circuit for the LP2995 can be seen in *Figure 3*.

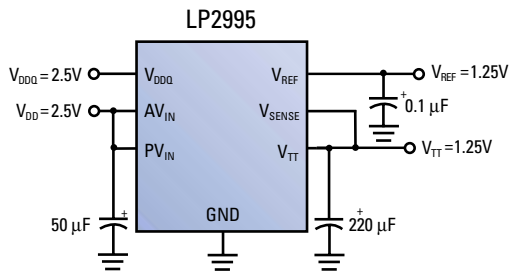

Figure 3: LP2995 Typical Application Circuit

Re-examining the limitations of the switcher and comparing it to the LP2995, the benefits of a linear topology are immediately recognizable.

Size: The external component count has been drastically reduced, permitting the solution to occupy a minimal amount of space. Combined with the LP2995 in an LLP package (Leadless Leadframe Package) an optimal solution can be obtained.

Cost: Removal of the external components creates an instant system cost reduction by 60%.

Performance: By its nature as a linear topology, there is no internal oscillator or switching noise to take into consideration. This results in increased performance, as data integrity can be improved with the absence of switching noise on V_{TT}.

Through careful analysis of the actual memory requirements National Semiconductor was able to provide the optimal solution for DDR termination, the LP2995. Designed with consideration of the end user it offers the highest level of integration while increasing the system performance and lowering the total system cost. The LP2995 offers the perfect solution for any DDR-SDRAM application where space, performance and cost are critical constraints.

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