LM2593HV

Comparing Topologies and the (Design) Rules of the Game

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Technology Edge

Comparing Topologies and the (Design) Rules of the Game

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Abstract
This paper compares the three major DC-DC converter topologies, and sets design guidelines for each, based on a logical understanding of their nuances and their response to input voltage variations.

Introduction
Experienced Power Supply designers working with one major topology who turn their attention to another, know they must shift mental gears quite dramatically. The 'rules of the game' change and those that don't recognize this will run into major design issues.

"Equations for all topologies are available, and one just needs to use them"---- correct? No, in fact even this write-up provides such a set of design equations, but that is just not enough.

Equations are by nature 'single-point' computations. For example if we input a given operating condition: V_{IN}=14V, Vout=5V, I_O =1A, we can use the appropriate Buck converter equation to calculate the input capacitor RMS current for this specific condition. But consider a more practical scenario with V_{IN} anywhere between 7V and 21V, 14V just representing a vague 'nominal' value? At what input voltage would we then get the worst-case input capacitor current? No set of equations, however complete, will point us in the right direction. So if Designer A 'picks' the lowest input voltage 7V, Designer B picks the highest input voltage 21V, and Designer C picks the nominal value of 14V, all of them actually need Designer S ('Senior') to breathe down their necks for a couple of years more! For the correct answer is Vin=10V.

The first step must be to clearly visualize the topologies, their differences and their similarities, and only then proceed towards atenable mathematical design procedure. Certainly the topologies are prima facievastly different ---- one is step-down (Buck), one is step-up (Boost) and the other is an inverting step up/down (Buck-Boost). Butwhat we are certainly not trying to do is to compare apples to oranges. There are very revealing comparisons we can make. Eventually these should help create that 'elusive' mental picture (three pictures actually in this case, one for each topology) that more experienced designers carry around in their heads.

Note that in this entire paper we will only refer to voltages or currents in terms of their magnitudes, thus ignoring any signs, polarities or directions. We are also only concerning ourselves with continuous conduction mode.

Back to the Basics
Changing the connection of the negative terminal of the output capacitor from ground rail to upper input rail can change the Boost to a Buck-Boost. Changing the negative input rail of a standard Buck converter to theoutput rail also changes it into a Buck-Boost. So the topologies may physically just be a 'jumper apart' in terms of their wiring, but the way the energy flows from the input to the output is worth more attention.

They fall into two basic categories. The Boost and Buck-Boost are similar in the sense that during the switch ON-time, energy from the input builds up in the inductor, with none passing to the output. When the switch turns off, the diode conducts, releasing the stored energy into the output sections and load. Contrast this with a Buck converter in which input energy flows through into the output during the switch ON-time. This seemingly innocuous point of difference is actually the defining influence on the entire pattern of behavior ofthe topologies.

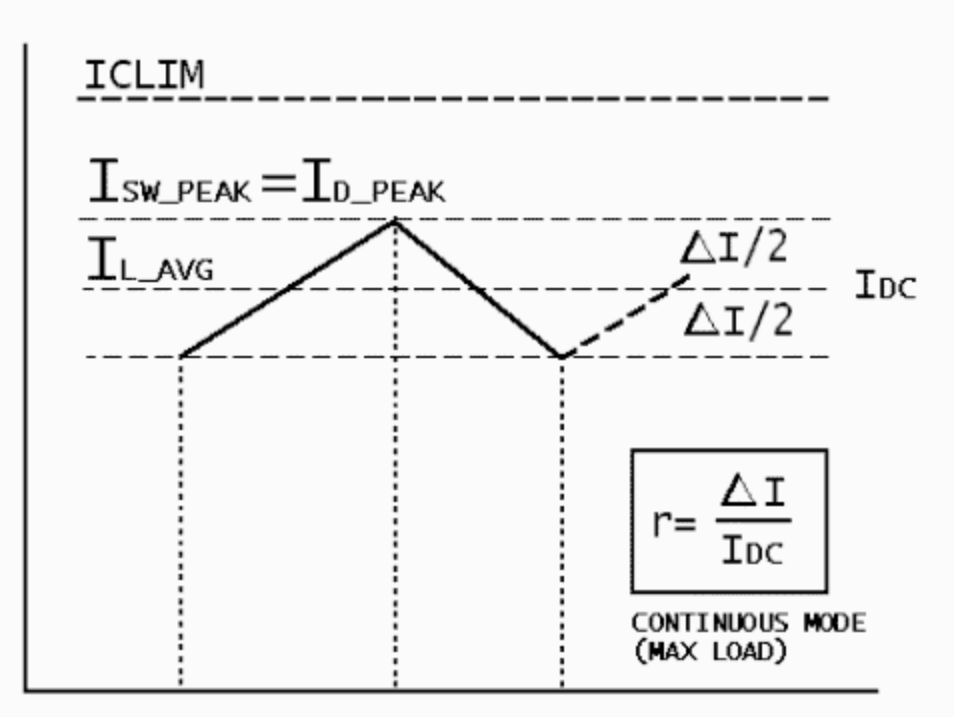


Figure 1

If power from the input to the output flows only during the off-time, all the power to the load must be passing through the diode (where else could it go through?). Therefore in a Boost or Buck-Boost the average diode current must always equal the load current. Not so in a Buck, where it is the average inductor current that equals the load current. See **Figure 1** for the terms we will be using.We will see that the relationships are:

$I_O = I_{L\_AVG} = I_{DC}$ (Buck)

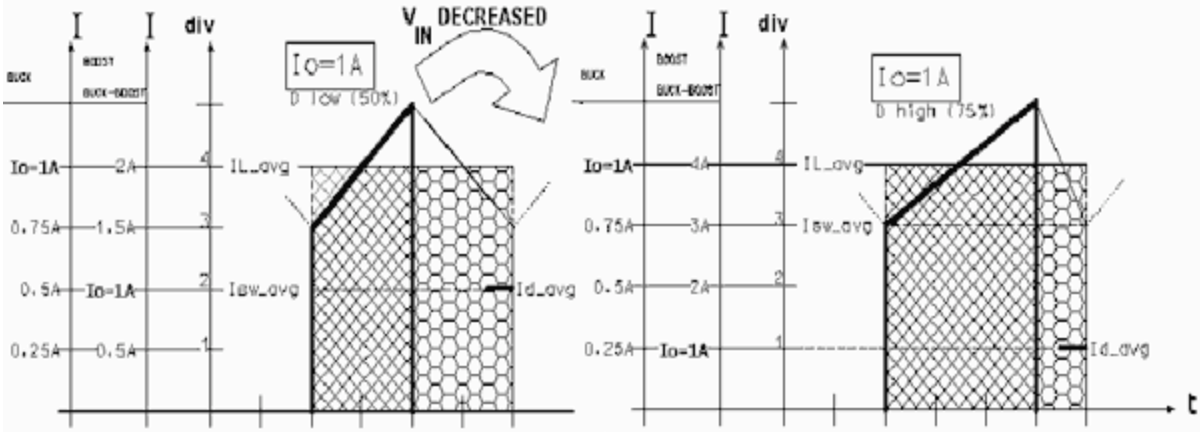
$I_O = I_{D\_AVG} = I_{DC} * (1-D)$ (Boost/Buck-Boost)

'D' is the duty cycle. So the average inductor current is related to load current by:

$I_{DC} = I_O$ (Buck)

$I_{DC} = I_O / (1-D)$ (Boost/Buck-Boost)

For a Buck, if the load is kept constant, the center of the inductor current waveform always remains constant/fixed if input voltage (or D) is varied. For the Boost and Buck-Boost the center starts to climb steeply as D approaches unity.



Average Currents			Buck	Boost	Buck-Boost
Io (A)	D low	(=0.5)	1	1	1
	D high	(=0.75)	1	1	1
IL_avg (A)	D low	(=0.5)	1	2	2
	D high	(=0.75)	1	4	4
Id_avg (A)	D low	(=0.5)	0.5	1	1
	D high	(=0.75)	0.25	1	1
Isw_avg (A)	D low	(=0.5)	0.5	1	1
	D high	(=0.75)	0.75	3	3

Figure 2

In **Figure 2** we illustrate more clearly how the average currents change as D increases. Note that the two curves are not intended to be necessarily of the same size or scale. Firstly we look only at the vertical scale marked 'div' ('div' for divisions). In both plots the trapezoid is replaced by rectangles of equivalent area by connecting through the geometrical center of the ramp portion. Then the arithmetic average is evaluated, which by definition is equal to the height of the rectangle in divs, multiplied by the factor D for average switch current, and by (1-D) for the average diode current. Now we impose the condition that we wish to compare all the topologies at a common reference level of say I_O =1A. Vertical axes can then be generated for each topology by applying the rule for I_O that we learnt above. We discover that the inductor will need to be sized for a continuous current of about 4A for the Boost and Buck-Boost (for operation at the lowest Vin, corresponding to D=0.75). For the Buck, a 1A rating is almost adequate. The peak of the actual current waveshape is actually somewhat higher and does affect the required rating somewhat, but we will discuss this later.

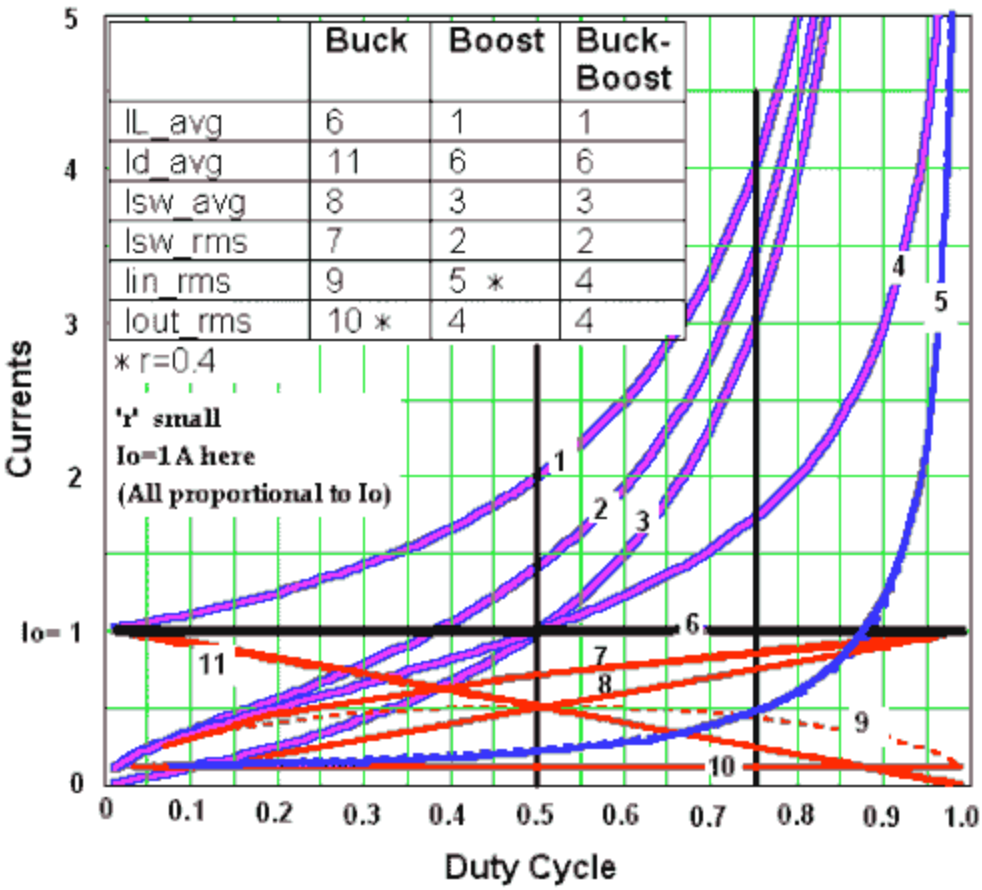


Figure 3

In **Figure 3** we have plotted out the actual values of the various currents as a function of D, all topologies again being compared at 1A load (input was set as 20V, and switch and diode forward drops were both 0.5V). The curves are all proportional to load current, so for a load of say 2A we just multiply the vertical axes by 2. Note that the curves in **Figure 3** apply for any switch frequency and are also virtually independentof the input voltage.

The effect of the average on the peak is nowconsidered. The peak of the inductor current waveform is a sum of its DC valueand half the ramp DI (which is usually comparatively smaller). Further, for any topology, the peak inductor current equals the peak of the switch and diode currents. We can conclude that as D increases all the associated peak currents of a Boost and Buck-Boost converter increase ---- on account of the sharp increase in the DC (average) value of the inductor current. The ramp usually plays a secondary role. So even though for these topologies the ramp portion decreases as D increases, that is not enough to drive the peak value down. For a Buck, the DC value remains fixed, and the ramp portion dominates the calculation of peak value. As D increases, the DI decreases (for constant output voltage), and so does the peak.

For the switch and diode the value of the peak current is relatively irrelevant, since we are mainly concerned only with the dissipation in these components, and that depends on the average current values (or the RMS value for Fet switches). However the peak inductor current is critical as it is directly related to the required energy handling capability of the inductor and therefore its size. In all power supplies, reducing the size of the magnetics is always a key design goal. If the inductor is sized inadequately, it may saturate at peak instantaneous current causing possible destruction of the switch. But making the inductor too large will make the converter unacceptably bulky.

Therefore a Buck inductor design should be done at lowest D (highest V_{IN}), at whichpoint the peak current is the maximum. Forthe Boost and Buck-Boost, the inductordesign should be carried out at lowest V_{IN}.

Inductor Energy Handling Capability

With reference to **Figure 1**, we define a term called 'Current Ripple ratio at maximumload' (applicable only for continuous conduction mode), or 'r'

$r = \Delta I / I_{DC}$

We will see that this is the most crucial parameter for any topology. It is also the entry point for starting any converter design.

So r is simply the ratio of the AC component (defined here as the full ramp ΔI) to the DC component of the inductor current waveform (center of ramp), with the converter delivering maximum load. Its range is from 0 (infinitely large inductance) to 2 (critical inductance i.e. the transition from Continuous Conduction mode to Discontinuous).

A high inductance reduces ΔI and results in lower r (and lower RMS Current in input/output capacitors). For all converters, rmust be the first item of selection in a design process ---- and it is to be chosen at maximum rated load, at the appropriate input voltage end as discussed above. Oncer is fixed, inductance can be calculated. The choice of r is actually the only significant independent variable that is in the hands of the designer. Since its choice impacts all the components of the power supply it be chosen carefully. More on this later.

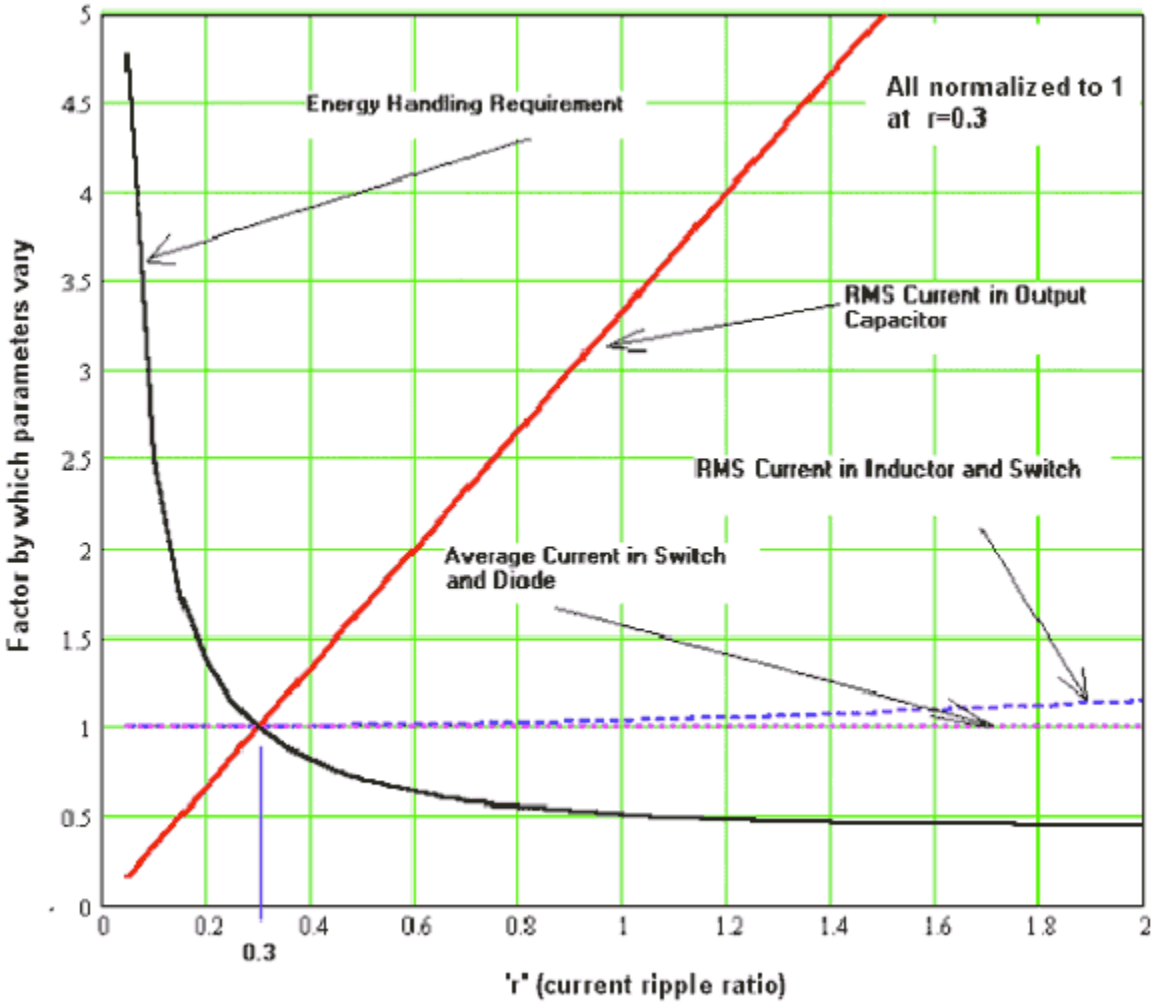


Figure 4

We also define the Voltuseconds ("voltmicroseconds") or 'Et' applied across an inductor. This is the product of the

magnitude of voltage across inductor and the duration of this applied voltage (inmicroseconds). Et can be calculated either during the ON-time or the OFF-time, both will give the same result. In a steady state there is no net change in voltseconds per cycle, or the current at the end of the cycle will not return to the value it started with. So Et is just another way of describing the amount of ramp component (for a given L). The connecting relationship is

$r = Et / (L x I_{DC})$

which is just V= L*dI/dt i.e.Et=V*dt=L*dI, combined with $r=dI/I_{DC}$

The required energy handling capability 'e' of the inductor is

$e = (1/2) \times L \times I_{PK}^{2}$ uJ

where L is in uH.

This can be rewritten for any topology as

$$e = \frac{I_{DC} \bullet Et}{8} \bullet \left[r \bullet \left(\frac{2}{r} + 1 \right)^2 \right] \quad uJ$$

However note that I_{DC} is different ---- it equals I_O for a Buck, and I_O / (1-D) for the Boost and Buck-Boost.

For maximum load and a given output voltage, if we fix the input voltage (Et and I_{DC} are also then fixed) we can design the inductor for any r within its valid range of 0 to 2. Let us plot what happens to e as we vary r in **Figure 4**. Here, as an example, other parameters of a Buck have also been displayed to indicate that the entire power supply is affected by the choice of r. We can see that the energy handling requirement (size of inductor) decreases as current ripple ratio increases (i.e. L is made smaller). But other parameters, chiefly the RMS current of the output cap, go up. So the best value isthe 'knee' corresponding to r of about 0.3 to 0.5. No great improvement in the size of the inductor will take place by increasing the current ripple much more than this, but the RMS Current in the output cap will certainly increase several times.

Fixing r at around 0.4 usually gives the best compromise between the relative sizes of all components. Note that this is a universal rule of sorts for all topologies. Now we see the advantage of talking in terms of r because in terms of L we would not be able to create any such general design rule. The choice of L would depend on the topology and frequency, besides other aspects of operation.

The more astute designer may realize a related fact: for all topologies the load at which the transition from Continuous to Discontinuous conduction modes occurs can be shown by simple geometry to be r/2 times the maximum load. So for example, if the inductance is chosen to be such that r=0.4 (at a max load of 2A, any topology), the transition will occur at 0.2 times 2 Amps, i.e. 400 mA. Note that for r=0.4, the peak current (switch/diode/inductor) is 20% higher than the average value of inductor current. But this average value is either I_O or I_O / (1-D), as we discussed earlier. This is aquick way to check what is the exact current rating requirement of the inductor.

To reiterate ---- current ripple ratio at maximum load r is the most important (and only) real design choice for the power supply designer. Once r is defined everything else follows quite predictably. Therefore all equations in **Table 1** have been written interms of this key parameter r. Which is why this table in the form it is presented, offers a logical, easy and insightful design procedure, as compared to struggling through a minefield of seemingly disconnected or oddly connected equations.

Comparing 'magnetics' in terms of theTransfer function

A visually/graphically revealing comparison of the topologies can be made in terms of the ratio V_{OUT} / V_{IN}, called

‘x’ here. This term intuitively indicates ‘how hard’ the converter is working at doing its job. x=1 corresponds to switch-fully-closed condition for a Buck, or switch-fully-open for a Boost, or a switch operating at 50% duty cycle for a Buck-Boost. x can theoretically lie between 0 and 1 for a Buck, between 1 to ¥ for a Boost and from 0 to ¥ for the Buck-Boost.

Note that high x corresponds to low V_{IN}. So a high x corresponds to a high duty cycle forall the topologies.

What happens to the energy handling capability (for a given r) as a function of x? Also, does a Boost typically require a larger inductance than a Buck-Boost?

Using **Table 1**, we can plot out these resultsin **Figure 5**. We can see that (for a given x), the size of the inductor and the required inductance (for r=0.4) increases 10 times for a tenfold increase in input voltage OR a tenfold decrease in frequency.

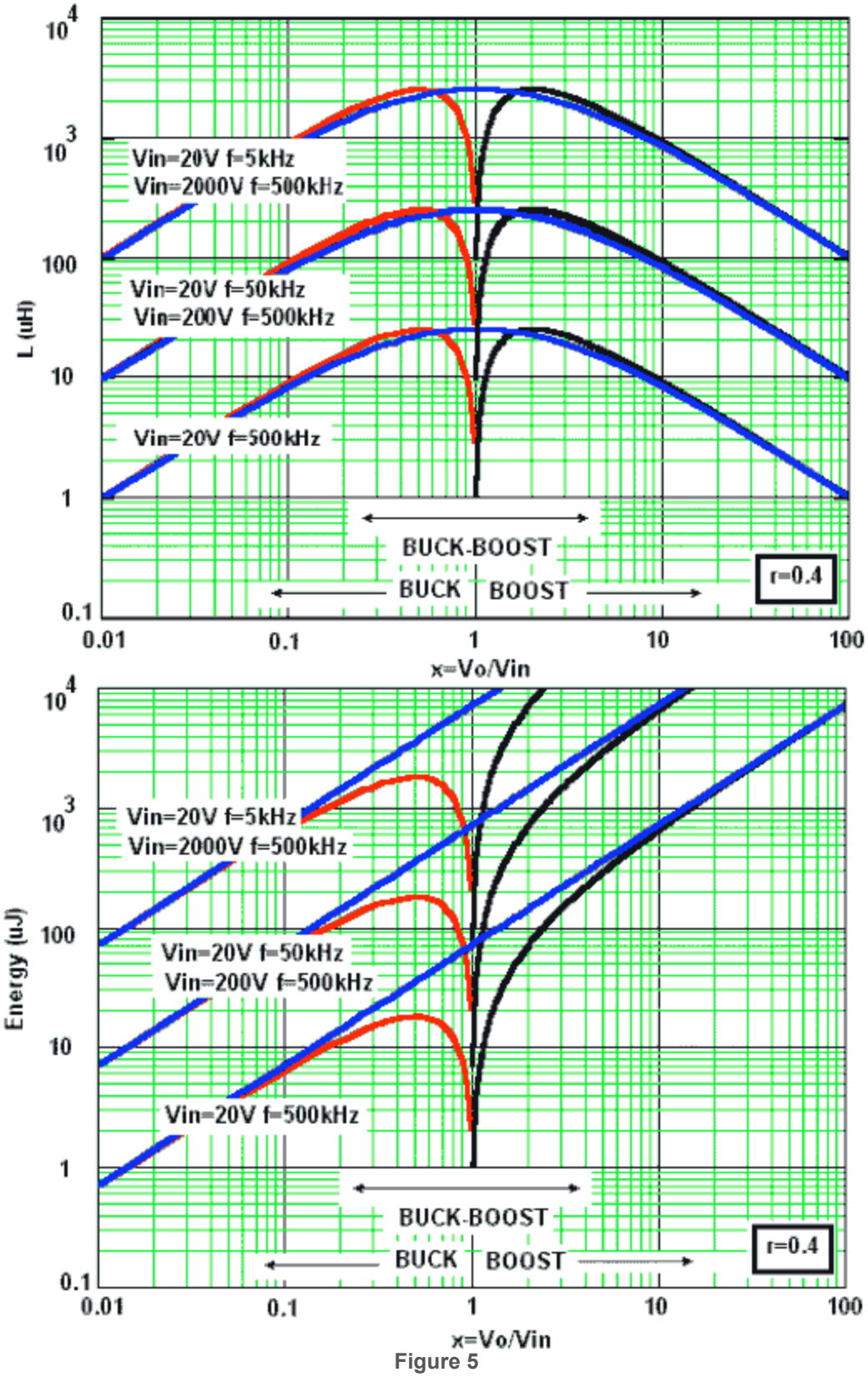


Figure 5

So the relationship is as follows: size and inductance are both proportional to voltage and inversely proportional to frequency for all topologies (for Vo/Vi = constant)

The buck requires the largest inductors for a duty cycle (V_{OUT}/V_{IN} = x = D) of 0.5. For all others, increasing x (i.e. higher D) means alarger inductor.

For inductance, all topologies call for the maximum inductance at V_{IN_50} (which is the input voltage for which the duty cycle is 50%--- from the figure check backwards using the definition of x). Note that for small x, the inductor size and inductance of a Buck-Boost approximates a Buck, and at high x, the Buck-Boost approximates the Boost.

Some of the above conclusions we may have already 'known' from gut feel (or a previous life). But especially where magnetics design is concerned, engineers are warned against relying completely on instincts or intuition, as this is often very misleading (See also **References a and b**).

In fact, the designer who feels he has understood all the above conclusions, now needs to realize that going from a curve of say 20V/500kHz to the upper one of 200V/500kHz, keeping x constant is easier said than done. It is not the same as the usual condition of VO =constant. So does the required inductance really change?? Intuition…..?!

Lastly, we note that **Figure 5** is drawn up to serve as a design chart. It does not directly reveal what happens to a given power supply as input voltage is changed. Therefore r is fixed at 0.4 for all the curves in **Figure 5**. Whereas in an actual power supply, as we change input voltage r changes. The actual variations of a real power supply in response to changes ininput voltage will be discussed in the next section.

Parameters	Buck	Boost	Buck-Boost
Duty Cycle	$\frac{V_O + V_D}{V_{IN} - V_{SW} + V_D}$	$\frac{V_O - V_{IN} + V_D}{V_O - V_{SW} + V_D}$	$\frac{V_O + V_D}{V_{IN} + V_O - V_{SW} + V_D}$
V_{IN_50} *(V)*	$(2 \bullet V_O) + V_{SW} + V_D$ $\approx 2 \bullet V_O$	$\frac{1}{2} \bullet [V_O + V_{SW} + V_D]$ $\approx V_O/2$	$V_O + V_{SW} + V_D$ $\approx V_O$
Output Voltage, V_O *(V)*	$V_{IN} \bullet D - V_{SW} \bullet D - V_D \bullet (1-D)$	$\frac{V_{IN} - V_{SW} \bullet D - V_D \bullet (1-D)}{1-D}$	$\frac{V_{IN} \bullet D - V_{SW} \bullet D - V_D \bullet (1-D)}{1-D}$
Et *(Vμsec)*	$\frac{V_O + V_D}{f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{f} \bullet D \bullet (1-D) \bullet 10^6$	$\frac{V_O + V_D}{f} \bullet (1-D) \bullet 10^6$
L *(μH)*	$\frac{V_O + V_D}{I_O \bullet r \bullet f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{I_O \bullet r \bullet f} \bullet D \bullet (1-D)^2 \bullet 10^6$	$\frac{V_O + V_D}{I_O \bullet r \bullet f} \bullet (1-D)^2 \bullet 10^6$
'r'	$\frac{V_O + V_D}{I_O \bullet L \bullet f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{I_O \bullet L \bullet f} \bullet D \bullet (1-D)^2 \bullet 10^6$	$\frac{V_O + V_D}{I_O \bullet L \bullet f} \bullet (1-D)^2 \bullet 10^6$
ΔI *(A)*	$\frac{V_O + V_D}{L \bullet f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{L \bullet f} \bullet D \bullet (1-D) \bullet 10^6$	$\frac{V_O + V_D}{L \bullet f} \bullet (1-D) \bullet 10^6$
RMS Current in Input Cap *(A)*	$I_O \bullet \sqrt{D \bullet \left[1 - D + \frac{r^2}{12}\right]}$	$\frac{I_O}{1-D} \bullet \frac{r}{\sqrt{12}}$	$\frac{I_O}{1-D} \bullet \sqrt{D \bullet \left[1 - D + \frac{r^2}{12}\right]}$
I_{PP} in Input Capacitor *(A)*	$I_O \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O \bullet r}{1-D}$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$
RMS Current in Output Cap *(A)*	$I_O \bullet \frac{r}{\sqrt{12}}$	$I_O \bullet \sqrt{\frac{D + \frac{r^2}{12}}{1-D}}$	$I_O \bullet \sqrt{\frac{D + \frac{r^2}{12}}{1-D}}$
I_{PP} in Output Capacitor *(A)*	$I_O \bullet r$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$
Energy Handling Capability *(μJoules)*	$\frac{I_O \bullet Et}{8} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$	$\frac{I_O \bullet Et}{8 \bullet (1-D)} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$	$\frac{I_O \bullet Et}{8 \bullet (1-D)} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$
RMS Current in Inductor *(A)*	$I_O \bullet \sqrt{1 + \frac{r^2}{12}}$	$\frac{I_O}{1-D} \bullet \sqrt{1 + \frac{r^2}{12}}$	$\frac{I_O}{1-D} \bullet \sqrt{1 + \frac{r^2}{12}}$
Average Current in Inductor *(A)*	I_O	$\frac{I_O}{1-D}$	$\frac{I_O}{1-D}$
RMS Current in Switch *(A)*	$I_O \bullet \sqrt{D \bullet \left[1 + \frac{r^2}{12}\right]}$	$\frac{I_O}{1-D} \bullet \sqrt{D \bullet \left[1 + \frac{r^2}{12}\right]}$	$\frac{I_O}{1-D} \bullet \sqrt{D \bullet \left[1 + \frac{r^2}{12}\right]}$
Peak Current Switch/Diode/ Inductor *(A)*	$I_O \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$
Average Current in Switch *(A)*	$I_O \bullet D$	$I_O \bullet \frac{D}{1-D}$	$I_O \bullet \frac{D}{1-D}$
Average Current in Diode *(A)*	$I_O \bullet (1-D)$	I_O	I_O

$r = \Delta I / I_{DC}$, Et in Vμsecs, L in μH, f in Hz, All voltages and currents are magnitudes

Table 1

The 'Stress Spider'

A comprehensive table of design information (**Table 1**) is provided for all the three main topologies: the Buck, the Buck-Boost and the Boost. Now we return to a more conventional (though less visually aesthetic) visualization of a power supply. Our condition here is that we have a power supply based of any topology, operating at constant (maximum) load, with a fixed output voltage. We now vary the input voltage. The duty cycle variation factors inthe input voltage variation. We predict the response of a given parameter to there sulting variation in duty cycle, and thereby figure out the worst case input condition for test or design. We plot the normalized variations of all key parameters as a function of duty cycle D in **Figure 6**, nicknamed the 'stress spider' here. Notice that each

parameter is shown individually normalized to unity value at V_{IN_50}. This is not the same as **Figure 3** where the currents were all absolute values stated for I_O =1A. The conclusions are summarized in **Table 2**, which serves as a quick lookup for design/test to establish worst-case operating points.

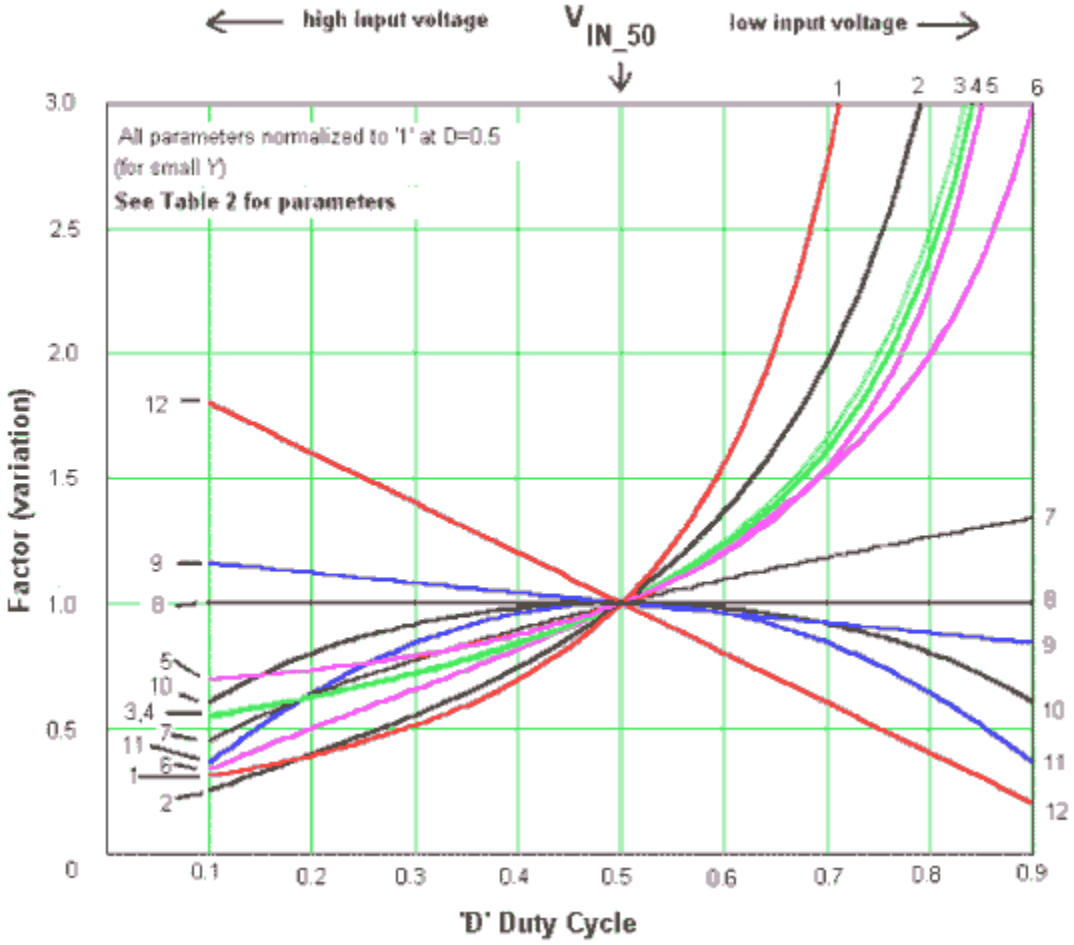


Figure 6

"Small 'r'" as mentioned in **Figure 6** means we are close to a 'flat-top' approximation. This is equivalent to a large inductance. Smaller inductances will generally lead to even higher RMS/peak currents.

Parameters	Buck	Boost	Buck-Boost
ΔI (I_{AC} in Inductor)	V_{IN_MAX} 12	V_{IN_50} 11	V_{IN_MAX} 12
Core Loss	V_{IN_MAX}	V_{IN_50}	V_{IN_MAX}
Inductor Energy/ Core Saturation	V_{IN_MAX}/ V_{IN} 8	V_{IN_MIN} 1	V_{IN_MIN} 1
Average Current in Inductor	V_{IN} 8	V_{IN_MIN} 3	V_{IN_MIN} 3
RMS Current in Inductor	V_{IN_MAX}/ V_{IN} 8	V_{IN_MIN} 3	V_{IN_MIN} 3
Copper Loss/Temperature of Inductor	V_{IN_MAX}/ V_{IN}	V_{IN_MIN}	V_{IN_MIN}
RMS Current in Input Capacitor	V_{IN_50} 10	V_{IN_50} 11	V_{IN_MIN} 6
Input Voltage Ripple	V_{IN_MAX}/V_{IN} 8	V_{IN_MAX} 12	V_{IN_MIN} 3
RMS Current in Output Capacitor	V_{IN_MAX} 12	V_{IN_MIN} 6	V_{IN_MIN} 6
Output Voltage Ripple	V_{IN_MAX} 12	V_{IN_MIN} 3	V_{IN_MIN} 3
RMS Current in Switch	V_{IN_MIN} 7	V_{IN_MIN} 2	V_{IN_MIN} 2
Average Current in Switch	V_{IN_MIN}	V_{IN_MIN}	V_{IN_MIN}
Peak Current in Switch/Diode/Inductor	V_{IN_MAX} 9	V_{IN_MIN} 4	V_{IN_MIN} 5
Average Current in Diode	V_{IN_MAX} 12	V_{IN} 8	V_{IN} 8
Temperature of Diode	V_{IN_MAX} 12	V_{IN} 8	V_{IN} 8

"V_{IN}" means there is no real dependency on input voltage

Table 2

We now analyze the key parameter variations with respect to D using **Table 1**.

a) Average Inductor Current:

$I_{DC} = I_O$ = constan t (BUCK)

$I_{DC} = [I_O/(1-D)] \mu 1/(1-D)$ (BOOST/BUCK-BOOST)

See **Figure 6** for the plots.

This reiterates that the inductor design must be conducted at minimum input voltage for a Boost or Buck-Boost. For a Buck regulator, as a first pass selection, we often simply pick an inductor with a current rating equal to the load current, irrespective of input voltage.

b) Inductor ramp current

For all topologies, this AC component is completely responsible for the core loss (which does not depend on I_{DC} , provided the inductor is not saturating).

Now, for all the topologies, there is an applied voltage 'V_{ON}' across the inductor when the switch is ON. This causes acertain AC ramp component 'ΔI' across the inductor from the basic equation $V_{ON}=L*\Delta I/(D/f)$ or $\Delta I=V_{ON}*D/(L*f)$, where f is the frequency. As the input voltage falls, V_{ON} also decreases, but D increases. So what is the net effect on ΔI? From **Table 1**

$\Delta I \mu (1 - D)$ (BUCK/BUCK-BOOST)
$\Delta I \mu D \bullet (1 - D)$ (BOOST)

See **Figure 6** for the plots.

If the input voltage range does not include V_{IN_50}, we must choose either V_{IN_MIN} or V_{IN_MAX}, whichever happens to be closer to V_{IN_50}.

c) Current Ripple ratio at max load 'r'

$r = (\Delta I/I_{DC}) = (\Delta I/I_O)$ (BUCK)

$r = (\Delta I/I_{DC}) = (\Delta I/I_O) \bullet (1-D)$ (BOOST/BUCK-BOOST)

See **Figure 6** for the plots.

The formal design procedure for any converter design can now be summarized:

First the inductor design is to be done. This is to be performed at lowest input for a Boost and Buck-Boost, and at highest input voltage for a Buck, by choosing r to be about 0.4. Then L can be calculated using Table 1. Since r varies as the input voltage changes, it can be recalculated at any input voltage, again by using **Table 1** and the L we have calculated. So if we are interested in finding the value of any parameter at any another specific input voltage, we can use the required equation from **Table 1**. But we might find that that requires an input value for r. The value of r to be used here must be the (recalculated) value of r at that particular input voltage. **Figure 6** will quickly indicate what input voltage is to be used if we want the worst-case value for the parameter.

d) Input Capacitor RMS current

This determines the basic/minimum selection criterion for the input capacitor since the capacitor must be rated at least for the worst case RMS current that will pass through it. A capacitor operated with an RMS current higher than its rated value, is not guaranteed to have any specific life by most manufacturers. And any published life expectancy vs. temperature curves/equations may not be valid.

For small r, we can see that this goes as

$$I_{IN} \propto \sqrt{D \bullet (1-D)} \quad \text{(BUCK)}$$

$$I_{IN} \propto \frac{r}{1-D} \propto \frac{D \bullet (1-D)^2}{1-D} = D \bullet (1-D)$$

(BOOST)

$$I_{IN} \propto \frac{1}{(1-D)} \bullet \sqrt{D \bullet (1-D)} = \sqrt{\frac{D}{1-D}}$$

(BUCK-BOOST)

See **Figure 6** for the plots.

So the temperature of the capacitor must also be evaluated at the correct input voltages. Again, if the input voltage range does not include V_{IN_50}, we must choose either V_{IN_MIN} or V_{IN_MAX}, whichever happens to be closer to V_{IN_50}.

e) Output Capacitor RMS Current

For small r, we can see that this goes as

$$I_{OUT} \propto r \propto (1-D) \quad \text{(BUCK)}$$

$$I_{OUT} \propto \sqrt{\frac{D}{1-D}} \quad \text{(BOOST/BUCK-BOOST)}$$

See **Figure 6** for the plots.

So the temperature of the output capacitor must also be evaluated at the correct input voltage.

f) Output Peak to Peak Current

We are also concerned with the peak to peak current, I_{PP_OUT} through the output capacitor as this determines the output voltage ripple. $DV_{OUT}=I_{PP\_OUT}$ *ESR_{OUT}, where ESR_{OUT} is the Equivalent Series Resistance of the output capacitor. This output ripple is a major component of the noise spectrum at the output of the power supply.

For small r, we can see that this goes as

$I_{PP\_OUT} \mu r \mu$ (1-D) (BUCK)
$I_{PP\_OUT} \mu$ (1/(1-D)) (BOOST/BUCK-BOOST)

So,
I_{PP_OUT} ---> maximum at highest input voltage for Buck
I_{PP_OUT} ---> maximum at lowest inputvoltage for Boost/Buck-Boost

g) Switch RMS Current

For a MOSFET switch we need to calculate the conduction loss as given by I^2_{RMS}*rds. The crossover losses are lowest at the minimum input voltage. But since they are usually a small fraction of the conduction losses, they are ignored here. The IRMS ofthe switch varies in the following manner

For small r, we can see that this goes as

$$I_{RMS} \propto \sqrt{D} \quad \text{(BUCK)}$$

$$I_{RMS} \propto \frac{\sqrt{D}}{1-D} \quad \text{(BOOST/BUCK-BOOST)}$$

Plotting these out in **Figure 6** we can see that

I_{RMS} ---> maximum at lowest input voltagefor Buck/Boost/Buck-Boost

Note that for a Buck, the dissipation in the switch goes up only slightly at low input voltages, but for the remaining topologies,the dissipation goes up quite steeply at low input voltages, leading to a large drop inefficiency. In **Table 1**, the average switch current is also provided, for calculation of dissipation in bipolar switches.

h) Average Diode Current

For a diode we need to calculate the forward loss as given by V_D * I_{D_AVG}, where 'V_D' is the drop across the diode when it conducts. For the Boost and the Buck-Boost, the average diode current is the load current, so it is not going to change with duty cycle. But for the Buck it does vary.

$I_{D\_AVG} \mu$ (1-D) (BUCK)

$I_{D\_AVG} \mu$ constan t (BOOST/BUCK-BOOST)

See **Figure 6** for the plots.

We know that the dissipation in the switch of a Buck remains relatively constant as input voltage increases (ignoring crossover losses), but now we see that the diode dissipation increases as we do so. So we expect the efficiency of a Buck regulator to fall at high input voltages on account of increased diode dissipation (assuming $V_{SW}<V_D$ where V_{SW} is the forward drop across the switch). For the Boost and Buck-Boost, the diode dissipation does not change as input voltage falls, but the switch dissipation increases dramatically. So we expect the efficiency of a Boost or a Buck-Boost to fall at low input voltages on account of increased switch dissipation (unless crossover losses are very large, in which case the reverse is occasionally found to be true).

For testing diode temperature, we need to test a Buck regulator at the highest input voltage. For the other topologies, it does not matter much. This is indicated as 'V_{IN}' in **Table 2**, implying any input voltage should be OK to design to or for test.

i) Inductor Energy

For our analysis here, we first make an approximation for the rather complicated term in **Table 1** for 'e' involving r. Assuming r to be small this term becomes

$$r \bullet \left[\frac{2}{r}+1\right]^2 \approx r \bullet \left[\frac{2}{r}\right]^2 \propto 1/r$$

Then

$$e \propto \frac{Et}{r} \propto \frac{(1-D)}{(1-D)} = 1 \quad \text{(BUCK)}$$

$$e \propto \frac{Et}{(1-D)\bullet r} \propto \frac{D\bullet(1-D)}{D\bullet(1-D)^3} \propto \frac{1}{(1-D)^2}$$

(BOOST)

$$e \propto \frac{Et}{(1-D)\bullet r} \propto \frac{(1-D)}{(1-D)^3} \propto \frac{1}{(1-D)^2}$$ (BUCK-BOOST)

See **Figure 6** for the plots. They are what we expected from previous discussions.

j) Average Inductor Current

If r is small, the average and RMS values of the inductor current are the same, 'I_L'. The copper loss in the inductor is I_L^2*R, where r is the winding resistance. This loss is usually very large compared to the core loss (which depends on DI, as discussed earlier), and it largely determines the temperature rise of the inductor.

For small r, we can see that the RMS/Avg current goes as

$I_L \mu$ constan t (BUCK)

$I_L \mu$ (1/(1-D)) (BOOST/BUCK-BOOST)

See **Figure 6** for the plots.

k) Peak Switch Current

This parameter is important because every controller has a current limit for the switch, and if the calculated peak exceeds the lowest value possible of the switch current limit, anywhere in the input voltage range, the required output power cannot be delivered. The peak current in a Buck is just a little higher than the load current, and so for example, the LM2593HV 'Step Down (Buck) regulator' IC from National Semiconductor, which is designed for '2A load', has a minimum set value of 2.3A for the switch current limit. Yet, as seen from the datasheet of this device, this Buck IC can be operated as a 'positive to negative' regulator, which is actually a standard Buck-Boost topology. In this mode, the peak current is much higher, and it depends on the duty cycle/input voltage too. So it may not be possible to get 2A load.

For small r, we can see that the peak currentgoes as:

$$I_{PEAK} \propto \left[1 + \frac{r}{2}\right] \propto \left[2 + (1-D)\right] = (3-D)$$

(BUCK)

$$I_{PEAK} \propto \frac{\left[1 + \frac{r}{2}\right]}{1-D} \propto \frac{\left[2 + (D\bullet(1-D)^2)\right]}{1-D}$$

(BOOST)

$$I_{PEAK} \propto \frac{\left[1 + \frac{r}{2}\right]}{1-D} \propto \frac{\left[2 + (1-D)^2\right]}{1-D}$$

(BUCK-BOOST)

See **Figure 6** for the plots.

Therefore Current Limiting must be ruled out at minimum input voltage for the Boost and Buck-Boost, but for the Buck we must go to the highest input voltage.

Summing Up

The visualizations and curves presented are an important part of trying to understand the topologies. The transformer-based topologies are not much different. For example the flyback has a design parameter called 'V_{OR}' or reflected output voltage (= V_O* (Np/Ns)) which is actually the output voltage of an equivalent Buck-Boost. The more experienced designer can easily extend the concepts presented here to transformer-based topologies. The 'mentalpicture' hopefully acquired here, also applies to them.

References

a) "Off-the-shelf Inductors for Buck-converters" by Sanjaya Maniktala, Electronic Engineering, August2001
b) "Current Ripple Ratio Simplifies Selection of Off-the-shelf Inductors for Buck-converters" by Sanjaya Maniktala, Power Electronics Technology, October2001
c) "Reducing Converter Stresses - Part 1" by Sanjaya Maniktala Power Electronics Technology, May 2002
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e) http://power.national.com

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