AN-2202 LM34927 Integrated Secondary Side Bias Regulator for Isolated DC-DC Converters

1 Introduction

An isolated bias supply is implemented in this evaluation board with LM34927 Constant-On-Time regulator. The LM34927 regulator integrates both the high and low side power switches essential for creating isolated buck converter.

The board specifications are as follows:

- Input Range: 20 V to 100 V
- Primary Output Voltage: 10 V
- Secondary (Isolated) Output Voltage: 9.5 V
- Maximum Load Current (Primary + Secondary): 300 mA
- Maximum Power Output: 3 W
- Nominal Switching Frequency: 750 kHz
- Efficiency (FIN = 48 V, IOUT2 = 300 mA): 76 percent
- Board size: 2 inch x 2 inch

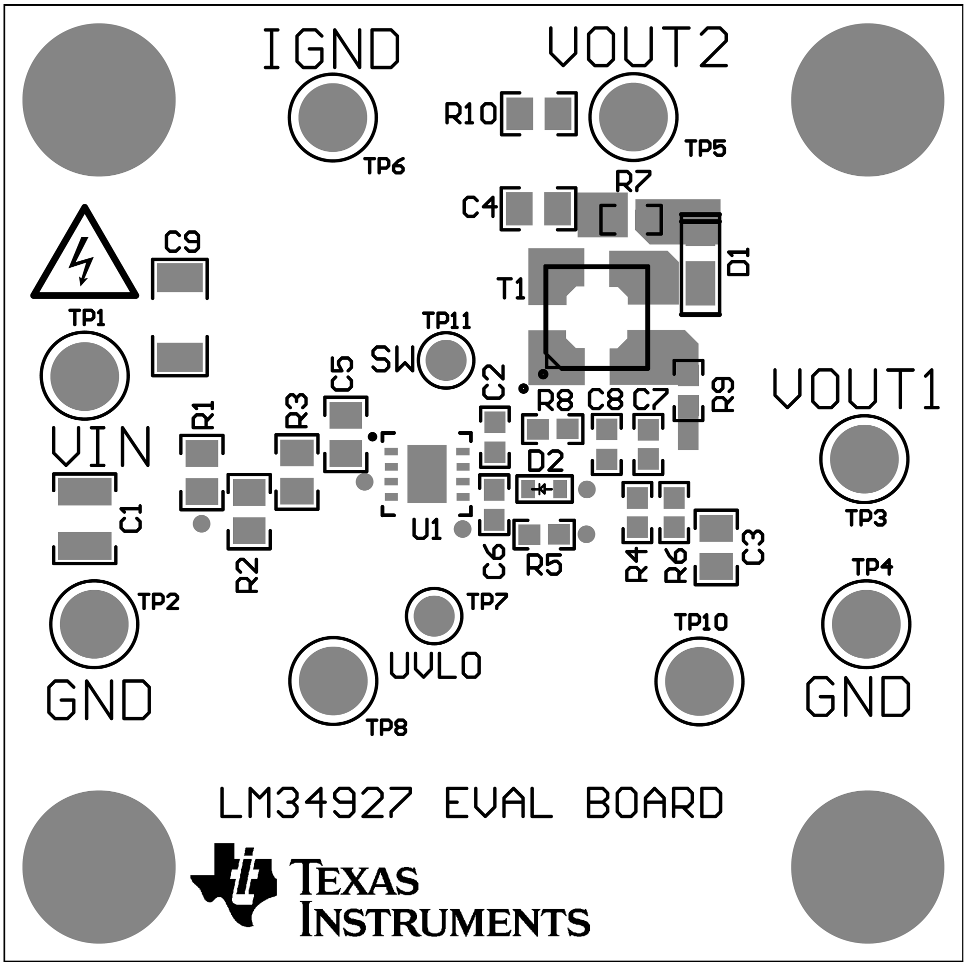

Figure 1. LM34927 Evaluation Board (Top View)

2 UVLO Threshold and Hysteresis

The UVLO resistors are selected using the following two equations:

$$V_{IN(HYS)} = I_{HYS}R_1 \tag{1}$$

and

$$V_{IN\ (UVLO,rising)} = 1.225V \times \left(\frac{R_1}{R_2} + 1\right) \tag{2}$$

On this evaluation board R1 = 127 kΩ and R2 = 8.25 kΩ, resulting in UVLO rising threshold at VIN = 20.5 V and a hysteresis of 2.54 V.

3 Board Connection And Start-Up

The input connections are made using TP1 (VIN) and TP2 (GND) terminals. The primary output appears at TP3 (VOUT1) and TP4 (GND). The secondary (isolated) output is available across TP5 (VOUT2) and TP6 (IGND). The input voltage should be gradually increased above UVLO set point of 20.5 V. Both the outputs (VOUT1 and VOUT2) should be close to 10 V at this point. This board is designed to function with input voltage range of 20 V to 100 V. The minimum VIN threshold can be changed by changing the UVLO resistors R1, R2. VIN should not exceed 100 V.

The magnetics in this design is optimized for solution size, and therefore limits the output power. **The total load at the output should not exceed 300 mA otherwise the coupled inductor will saturate/overheat which can destroy both the coupled inductor and the regulator IC U1.** If a sustained over-current situation is to be tolerated, a coupled inductor with higher saturation and rms ratings should be used. The board schematic is shown in Figure 2.

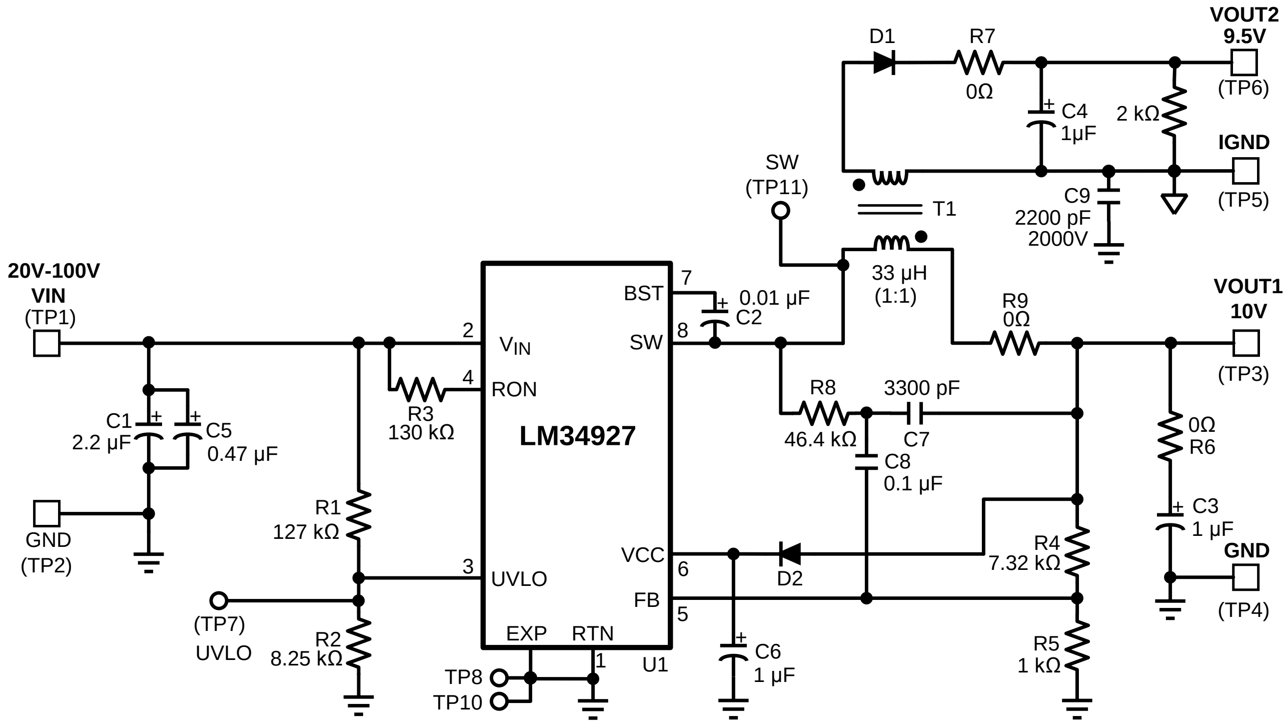

Figure 2. Complete Evaluation Board Schematic

4 Bill of Materials

Table 1. Bill of Materials

Item	Description	Mfg., Part Number	Package	Value
U1	Sync Switching Regulator	Texas Instruments, LM34927	LLP-8	100V, 0.6A
T1	Coupled Inductor, 1500 VDC	Coilcraft, LPD5030V-333ME	5mm x 5mm	33uH, 0.47A
	Alternate Part	Wurth, 750312750	8.26mm x 6.60mm	22uH, 0.76A
D1	Schottky Diode	Diodes Inc., DFLS1100-7	Pwr–DI123	100V, 1A
D2	Schottky Diode	Diodes Inc., SDM10U45-7	SOD–523	40V, 100mA
C1	Ceramic Capacitor	TDK, C3225X7R2A225K	1210	2.2uF, 100V, X7R
C2	Ceramic Capacitor	TDK, C1608X7R1C103K	0603	0.01uF, 16V, X7R
C3, C4	Ceramic Capacitor	TDK, C2012X7R1E105K	0805	1uF, 25V, X7R
C5	Ceramic Capacitor	Murata, GRM21BR72A474KA73L	0805	0.47uF, 100V, X7R
C6	Ceramic Capacitor	TDK, C1608X7R1C105K	0603	1uF, 16V, X7R
C7	Ceramic Capacitor	Murata, GRM188R72A332KA01D	0603	3300pF, 100V, +/-5%
C8	Ceramic Capacitor	AVX, 0603YC104KAT2A	0603	0.1uF, 16V, X7R
C9	Ceramic Capacitor	Johanson, 202R29W222KV4E	1808	2200pF, 2000V, X7R
R1	Resistor	Vishay/Dale, CRCW0805127KFKEA	0805	127k ohm, 1%
R2	Resistor	Vishay/Dale, CRCW08058K25FKEA	0805	8.25k ohm, 1%
R3	Resistor	Vishay/Dale, CRCW0805130KFKEA	0805	130k ohm, 1%
R4	Resistor	Panasonic, ERJ-3EKF7321V	0603	7.32k ohm, 1%
R5	Resistor	Panasonic, ERJ-3EKF1001V	0603	1.0k ohm, 1%
R6	Resistor	Yageo, RC0603JR-070RL	0603	0 ohm
R7, R9	Resistor	Yageo, RC0603JR-070RL	0603	0 ohm
R8	Resistor	Panasonic, ERJ-3EKF4642V	0603	46.4k ohm, 1%
R10	Resistor	Panasonic, ERJ-6GEYJ202V	0805	2k ohm, 5%

5 Performance Curves

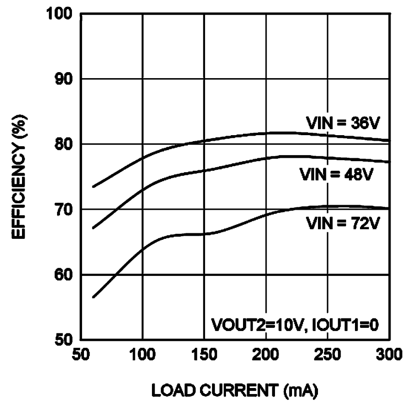

Figure 3. Efficiency at 750 kHz, VOUT1=10V

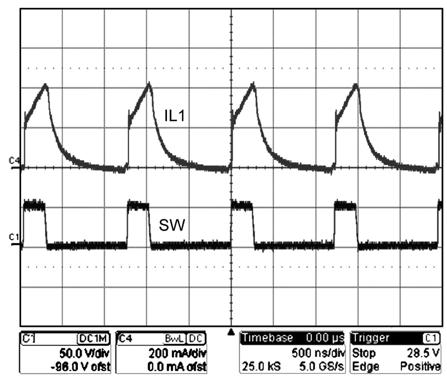

Figure 4. Steady State Waveform (VIN=48V, IOUT1= 100mA, IOUT2= 200mA)

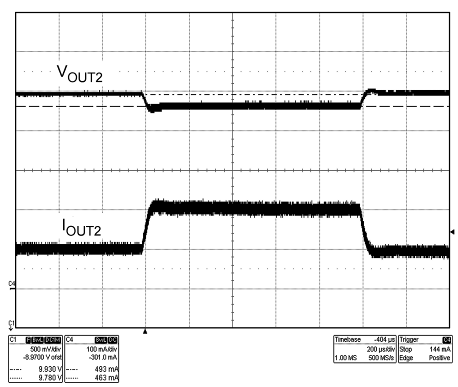

Figure 5. Step Load Response (VIN=48V, IOUT1=0, Step Load on IOUT2=100mA to 200mA)

6 PC Board Layout

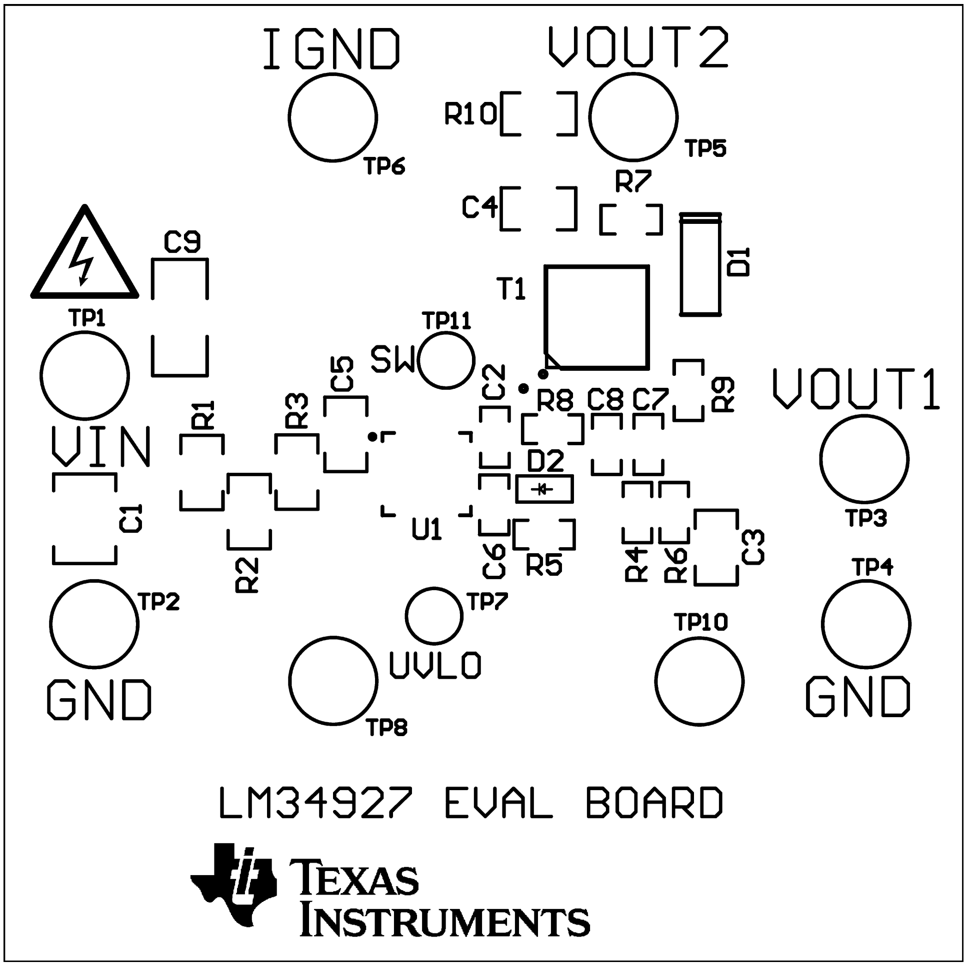

Figure 6. Board Silkscreen

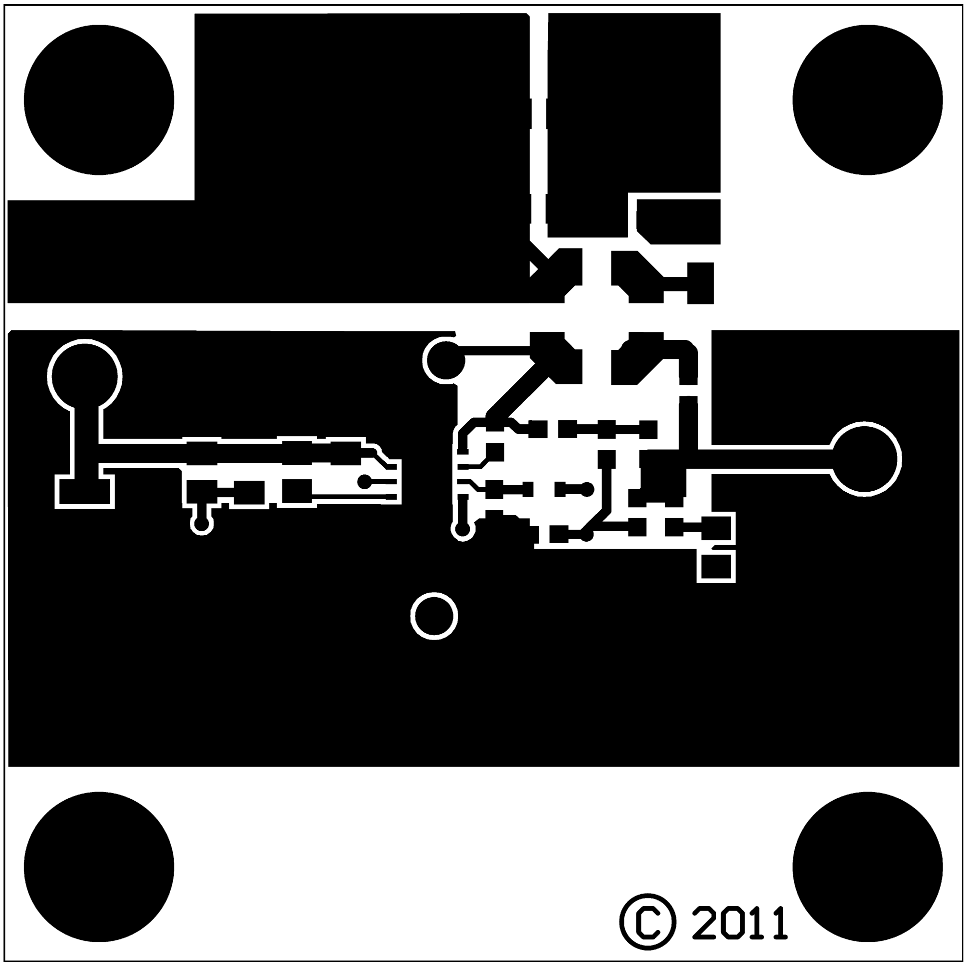

Figure 7. Board Top Layer

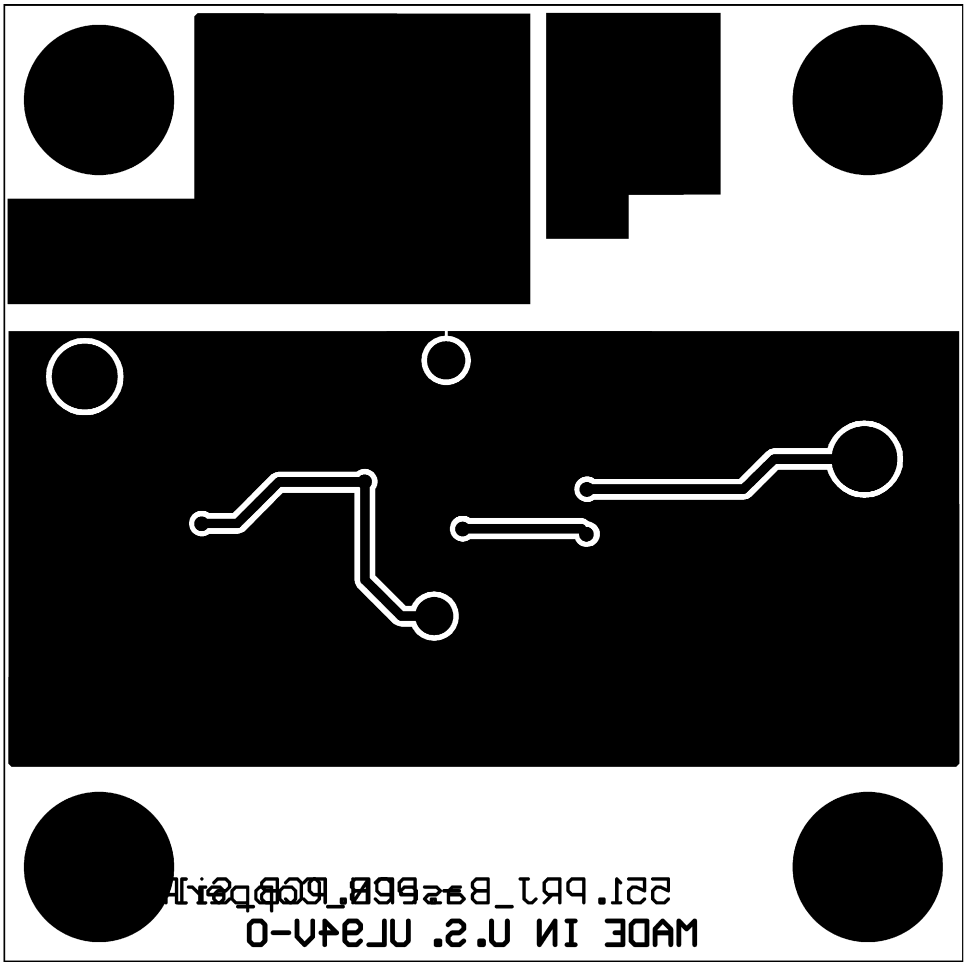

Figure 8. Board Bottom Layer

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