Application Report
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TPS92314 THD Design Consideration

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ABSTRACT

The TPS92314 device can be implemented in an LED driver with primary-side regulation and flyback topology. It is an off-line controller specifically designed with the primary-side sensing, constant on-time and quasi-resonant switching techniques. The TPS92314 application circuitry gives high power factor (PF), good EMI performance, and high system efficiency. Also, using the TPS92314 device allows easy design of low external component count application solutions. This paper describes the design consideration for THD and PF, as well as the design example.

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1 Introduction: THD (Total Harmonic Distortion) and PF (Power Factor)

PF correction is inherent if the TPS92314 device is operated in the constant on-time mode with an adaptive algorithm, and single stage flyback topology like PMP4347.

Considering a specific condition:

AC input voltage (RMS): V_{AC}; Line AC frequency: f_{AC}; Rating Power: Pin

Output voltage: Vo; Transformer turn ratio: n = Np/Ns;

Let: $\omega = 2\pi f_{AC}$;

In the primary side, it is essential that the transition mode single stage can generate the following switching current and input average current shown in Figure.1. During a high-frequency switching cycle $t \in [\tau, \tau + T_{sw}]$, the duty cycle and primary-side peak current should follow the following equations:

$$D(t) = \frac{t_{ON}}{t_{ON} + t_{off} + 2 \times t_{Dly}}; \quad i_{peak}(t) = \frac{\sqrt{2} V_{AC} t_{ON}}{L_p} Sin(\omega t)$$

$$t_{off} = \frac{t_{ON} \times \sqrt{2} V_{AC}}{n \times V_o}$$

Here a delay time can be defined in Figure 1.

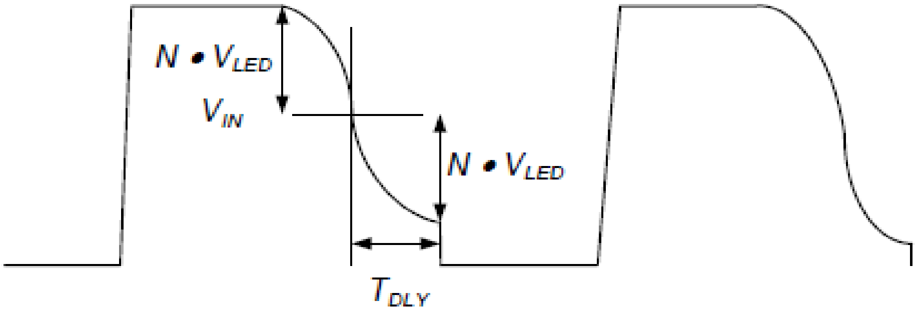


Figure 1. The Delay Time Definition

Let: $K = \frac{\sqrt{2}V_{AC}}{nV_o}$, $m = \frac{2t_{Dly}}{t_{ON}} + 1$,

And $I_m = \frac{\sqrt{2}V_{AC}}{2L_p} t_{ON}$ (Eq.1)

Then the duty cycle:

$D(t) = \frac{1}{m + K \times Sin(\omega t)}$; and peak current $i_{peak}(t) = 2I_m Sin(\omega t)$

As a results, during a high-frequency switching cycle t∈[τ, τ+T_{sw}], the input continuous current can be derived as shown in Equation 2:

$$i_{in}(t) = I_m \frac{Sin(\omega t)}{m + K \times Sin(\omega t)} \quad \text{(Eq.2)}$$

Considering the practical design for the peak current mode, the K should be greater than m.

Equation 2 showed that the input current is not a pure SINE waveform, but that it contains high-order harmonic elements.

The input total RMS current can be derived as shown in Equation 3:

$$I_{in} = \sqrt{\frac{\int_0^{\pi} i_{in}{}^2(t)\, d\omega t}{\pi}} = \frac{I_m}{\sqrt{\pi}} \sqrt{\int_0^{\pi} \frac{Sin^2(\omega t)}{(m + K \times Sin(\omega t))^2} d\omega t}$$

Then,

$$I_{in} = \frac{I_m}{\sqrt{\pi}K} \sqrt{\pi - 4\frac{K}{m} + 2\frac{(2K^2 - m^2)}{(K^2 - m^2)}\left(\frac{K}{m} + m\frac{Ln\left(\frac{(K - \sqrt{K^2 - m^2})}{m}\right)}{\sqrt{K^2 - m^2}}\right)} \quad \text{(Eq.3)}$$

Considering the harmonics elements of the input current, the first harmonics RMS current should be:

$$I_{1RMS} = \frac{1}{\sqrt{2}} \frac{2}{\pi} \int_0^{\pi} i_{in}(t) Sin(\omega t) d\omega t = \frac{\sqrt{2}}{\pi} \int_0^{\pi} I_m \frac{Sin^2(\omega t)}{m + K \times Sin(\omega t)} d\omega t$$

Then:

$$I_{1RMS} = \frac{\sqrt{2}I_m}{\pi K^2}\left[2K - m\pi + \frac{2m^2 Ln\left(\frac{(K + \sqrt{K^2 - m^2})}{m}\right)}{\sqrt{K^2 - m^2}}\right] \quad \text{(Eq.4)}$$

" I_{1RMS} " is the fundamental harmonic element of the input current.

Practically, the input power comes from the fact that the input line AC voltage times the first harmonics RMS current. Equation 5 shows the total harmonics distortion (THD):

$$THD = \frac{\sqrt{I_{in}^2 - I_{1RMS}^2}}{I_{1RMS}^2} \qquad \text{(Eq.5)}$$

Figure 2 shows how THD changes with different "K".

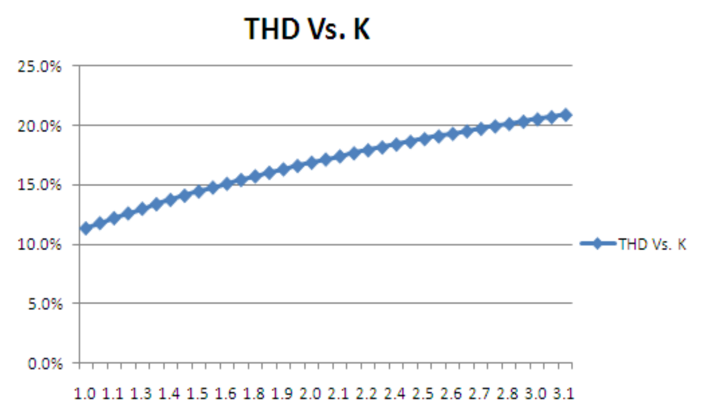


Figure 2. THD versus K (K = Vp/nVo)

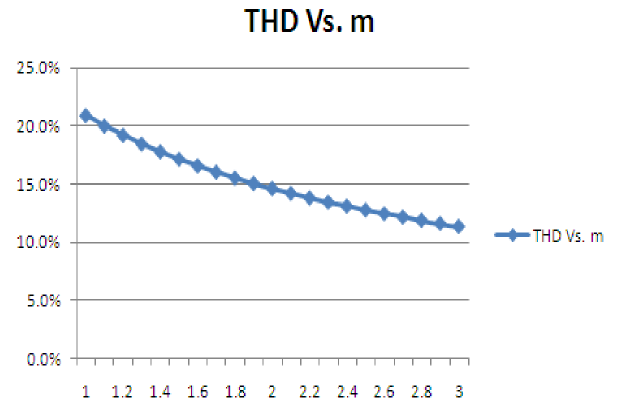


Figure 3. THD versus m (K = 3)

Figure 2 shows that increasing K causes an increase of THD. Thereby the transformer turn ratio, n (n = Np/Ns) should be high enough to realize a lower K. Hence, the higher the input voltage, the higher the THD.

Meanwhile, the increasing m causes a decreased THD. It means if delay time is increased during the off-time of the switching, the THD can decrease (see Figure 3).

It is possible to increase the m by increasing t_{Dly}. It is known that:

$$t_{Dly} = \frac{\pi\sqrt{L_p C_{ds}}}{2} \qquad \text{(Eq.6)}$$

So that the larger L_p or C_{ds} can improve THD. For example, an additional capacitor in C_{ds} can improve THD.

According to the TPS92314 data sheet, the DLY delay time can be programmed as shown in Figure.4.

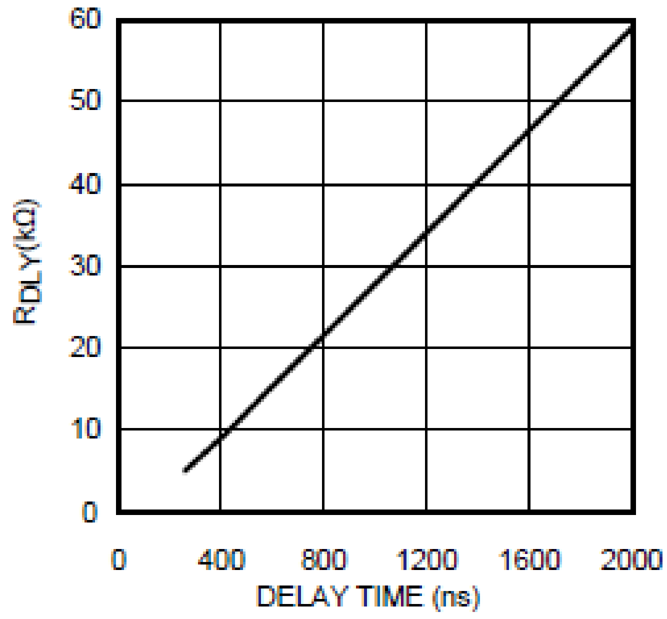


Figure 4. TPS92314 Delay Time Definition

The equation is: $R_{DLY} = K_{DLY}(t_{Dly} - 105ns)$ (Eq.7)

Where: $K_{DLY} = 32M\Omega / ns$

Therefore, based on Equation 5 and Equation 6, improved THD results are possible.

2 TPS92314 Loop Design Consideration

The TPS92314 device employs a discontinuous current mode with adaptive frequency. Figure 5 shows the internal block diagram of the TPS92314 device.

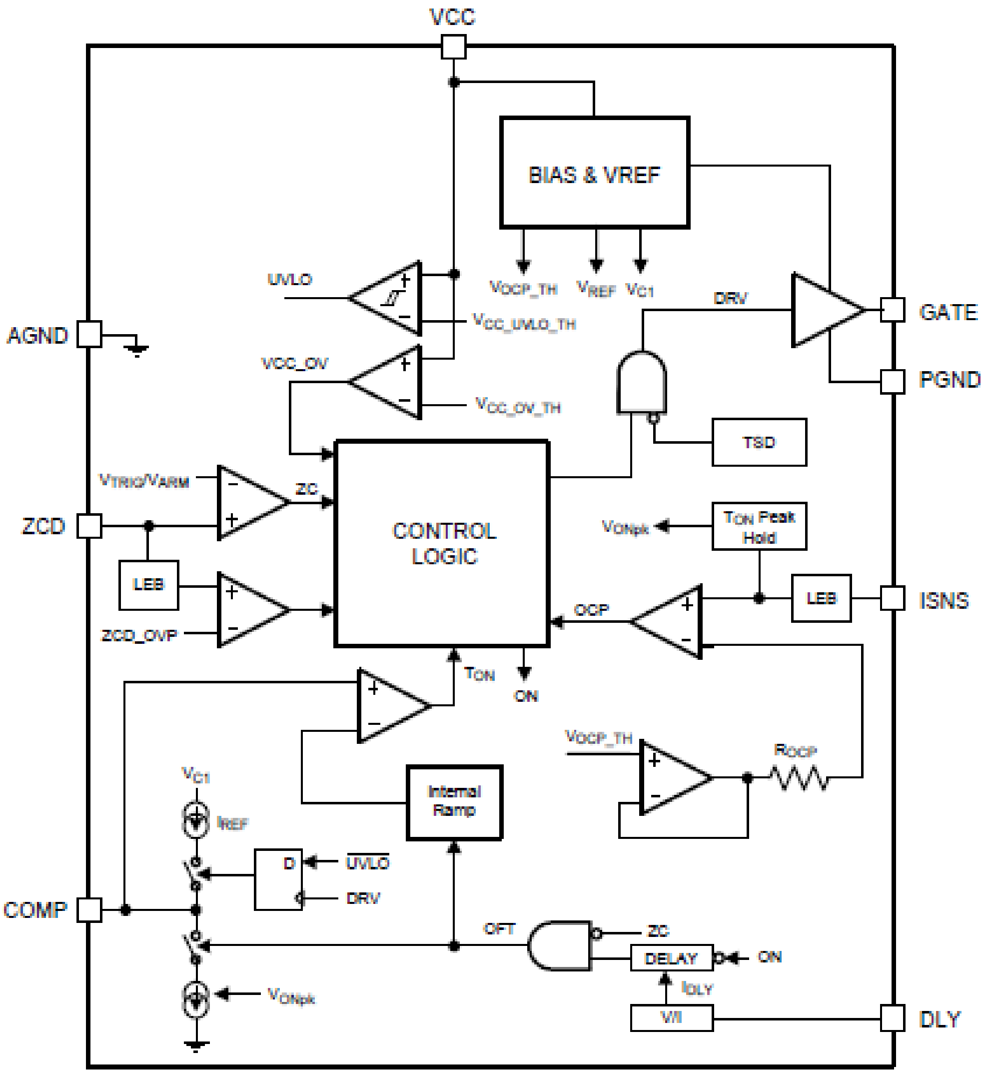
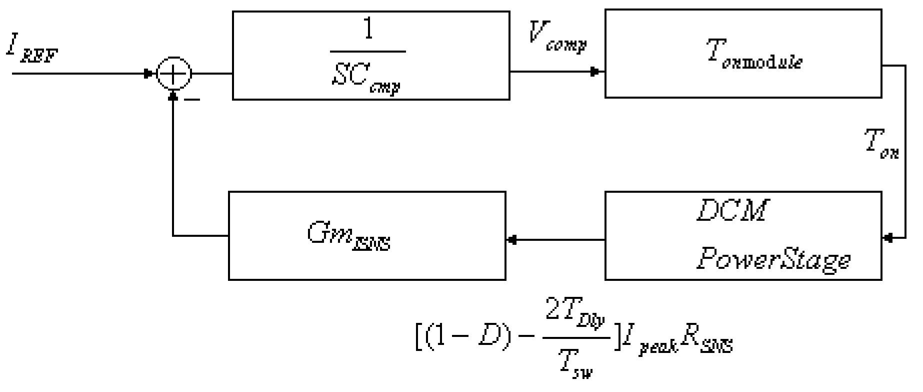


Figure 5. Internal Block Diagram of TPS92314 Device

Figure 6 shows the control block diagram of the TPS92314 device.



$$[(1-D)-\frac{2T_{Dly}}{T_{sw}}]I_{peak}R_{SNS}$$

Figure 6. Control Block Diagram of TPS92314 Device

According to the TPS92314 data sheet:

Here: $I_{REF} = 27uA; Gm_{ISNS} = 96umho; T_{on\,module} = 21us/v$

And, by the DCM analysis, $[(1-D)-\frac{2T_{Dly}}{T_{sw}}]I_{peak}R_{SNS} = 2\times I_{LED}\times R_{SNS}\big/ n$

For the DCM flyback power stage, according to reference [3], it is possible to get the small-signal circuitry shown in Figure 7

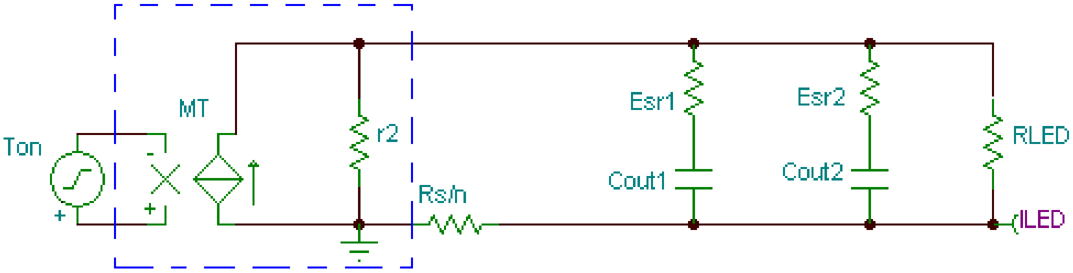


Figure 7. Small-Signal Circuitry for DCM Power Stage

Here, $M_T = \dfrac{V_I^2}{2L_p(m+\dfrac{V_I}{nV_{out}})V_{out}}$; $r_2 = \dfrac{2L_p(m+\dfrac{V_I}{nV_{out}})^2 V_{out}^2}{V_I^2 t_{on}}$ (Eq.8)

Therefore, the overall small-signal circuitry shown in Figure 8 can be obtained.

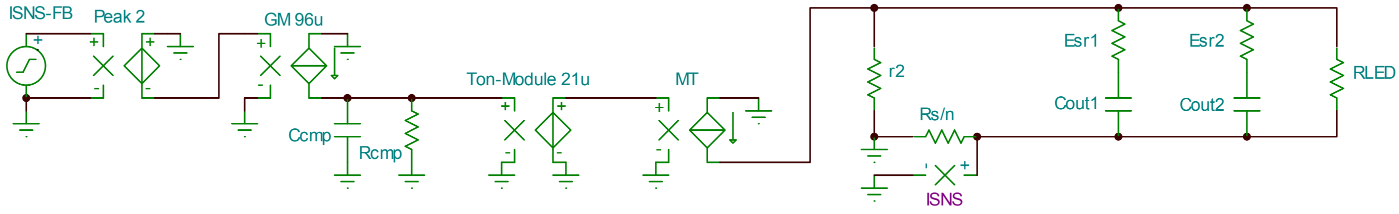


Figure 8. TPS92314 Overall Small-Signal Circuitry

3 TPS92314 THD Design Consideration

A design example: with 90 to 264 VAC universal AC input, and 40 V/20 W T8 LED driver with 420-mA current.

In the original design, the primary side to secondary side transformer turn ratio is 3:1, and the primary side inductor is 460 μH.

According to the PMP4347 reference design, with the 6.8k resistor in DLY (pin 5), Table 1 lists the test results:

Vin (Vac)	PF	THD (%)	Vo (V)	Io (A)	Pin (W)	Eff (%)
264	0.915	23.9	40.07	0.428	19.33	88.7
220	0.944	21.7	40.03	0.423	18.92	89.5
180	0.965	19.1	40	0.419	18.66	89.8
110	0.99	12.8	39.94	0.414	18.72	88.3

Table 1. PMP4347 Test Results

With less than 20 percent THD requirement, the THD in Table 1 must be improved.

According the calculations based on the preceding equations, the following expected results are derived:

<table>
<tr><th>Vin (Vac)</th><th>Vout (V)</th><th>n</th><th>m</th><th>Lp (uH)</th><th>Iout (A)</th><th>Ton (us)</th><th>r2</th><th>MT (k)</th><th>Pin (W)</th></tr>
<tr><td>264</td><td>40</td><td>3</td><td>1.6</td><td>460</td><td>0.42</td><td>1.1</td><td>213.73</td><td>803.99</td><td>20</td></tr>
<tr><td colspan="10"></td></tr>
<tr><th>I1RMS (A)</th><th>Iin (A)</th><th>Ipeak (A)</th><th>THD</th><th>Toff-Max (μs)</th><th>tDLY (ns)</th><td colspan="4" rowspan="2">Remark: It is based on a 7.5k resistor in pin 5 (DLY) of the TPS92314 device.</td></tr>
<tr><td>0.076</td><td>0.077</td><td>0.89</td><td>16.7%</td><td>4.07</td><td>339.4</td></tr>
</table>

Table 2. Calculated Results Based on Equations 1 Through 5

We can increase the delay time, or the m, by adding a 220-pF capacitor between drain and source of the Q1 MOSFET. Meanwhile, we can increase the delay setup resistor in pin 5 of the TPS92314device, from 6.8k to 7.5k; this provides the related delay time setup according to Equation 7.

Therefore, the test results with 7.5k DLY resistor are obtained as listed in Table 3:

Vin (Vac)	PF	THD (%)	Vo (V)	Io (A)	Pin (W)	Eff (%)
264	0.92	19.6	40.05	0.425	19.75	86.2
220	0.948	17.6	40	0.418	19.04	87.8
180	0.969	15.8	39.92	0.413	18.55	88.9
110	0.992	10.6	39.88	0.407	18.58	87.4

Table 3. The Improved THD Test Results

Figure 9 shows the comparison between Table 1 and Table 3.

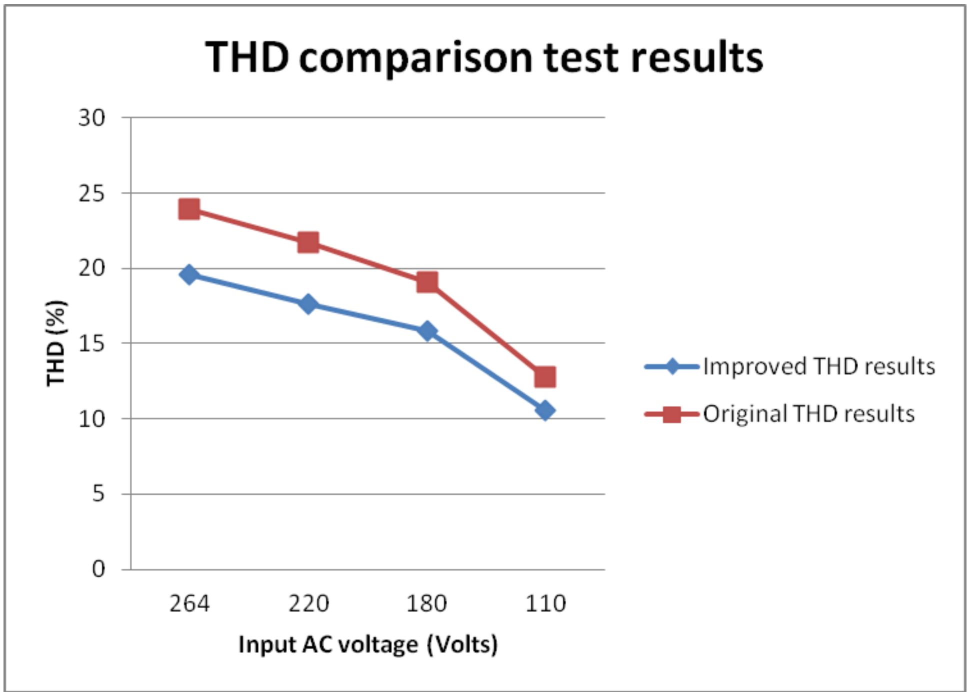


Figure 9. THD Results Comparison

Figure 9 shows approximately 4 percent THD reduction with 26-VAC input.

Compared the Table 2 calculation with the Table 3 test results, with 26-VAC input, there is still some THD gap with 16.7 percent versus 19.6 percent.

According to the preceding discussion and related equations, with 264-VAC input, PMP4347 small-signal circuitry can be obtained, as shown in Figure 10:

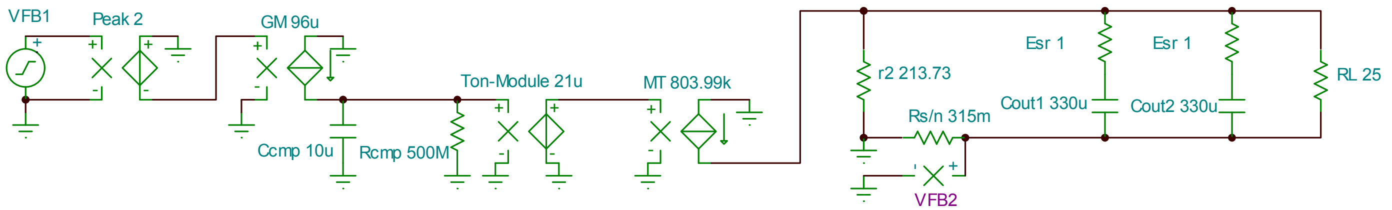


Figure 10. PMP4347 Related Small-Signal Circuitry

Figure 11 shows the simulation results. This figure shows the cross-over frequency is 49 Hz and the phase margin is 91 degrees.

It is known that the input 2 ≥ x 50 Hz needs a lower cross-over frequency to damp. A larger capacitor can be implemented in the COMP pin of the TPS92314 device. We can change it from 3.3 µF to 6.9 µF. After the update, the cross-over frequency is 23 Hz and the phase margin is 92 degrees.

Therefore, with the capacitor change, the test results showed a new THD:

THD = 17.8% @ Vin = 264 VAC. It is much lower than the THD test results with 264 VAC input in Table.3.

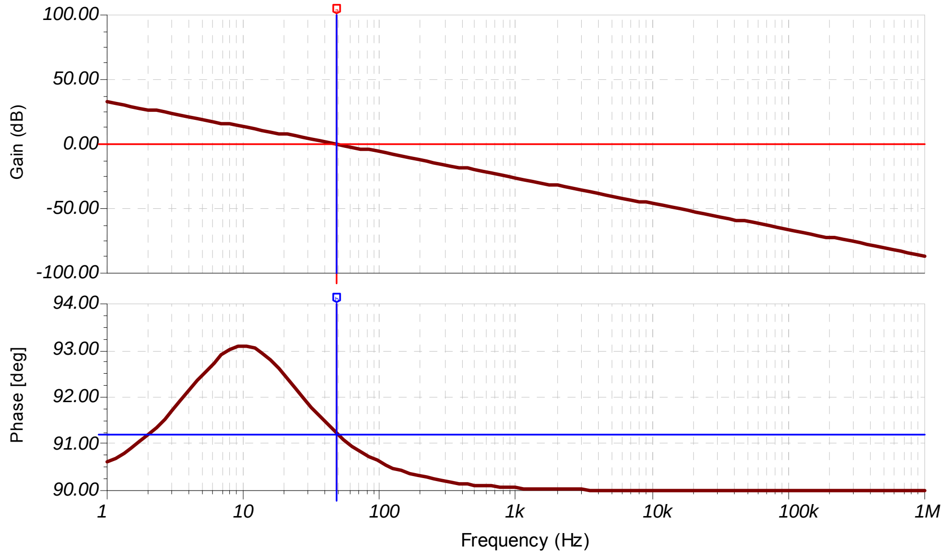


Figure 11. Simulation Results With 3.3-µF COMP Capacitor

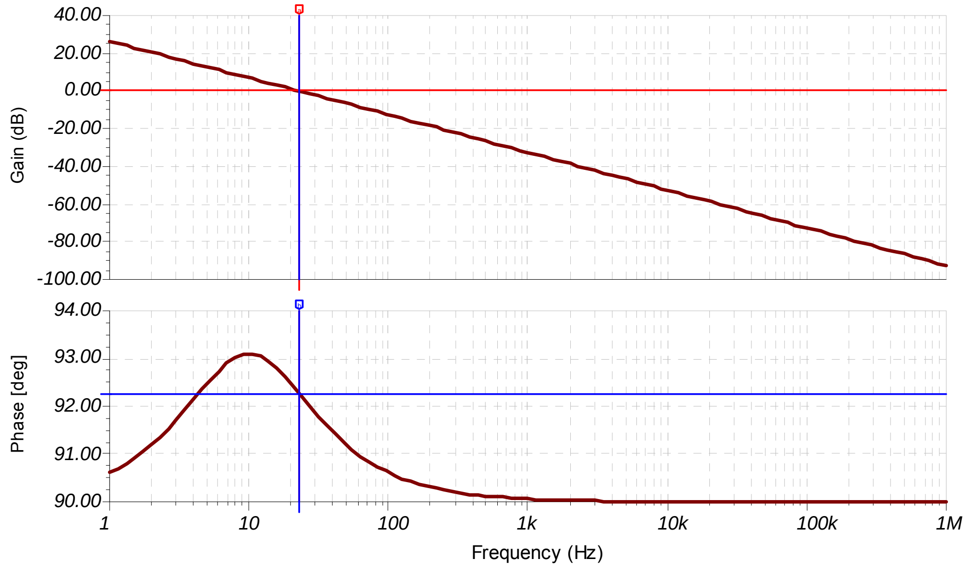


Figure 12. Simulation Results With 6.9-µF COMP Capacitor

4 Conclusion

This application note provides the analysis about single-stage flyback in the LED driver, and the solution to improve the THD results in the LED driver based on the TPS92314 device. Meanwhile, a practical design has been implemented. This paper explained the solutions and proved they are effective.

5 References

1. Texas Instruments, SNVS856A, TPS92314 data sheet

2. Linda Ye, Texas Instruments, PMP4347 reference design

3. Tony Huang, Texas Instruments, SLUA625, *LED Driver Based on UCC28060 Interleaved ACDC Single Stage Flyback*

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