Application Report
SNVA778–October 2017

LM3627x Layout Guidelines

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ABSTRACT

This document describes the optimized layout for the LM3627x family of white LED backlight + LCD display bias power IC's. The goal of utilizing a good layout is to minimize the PCB trace inductance in the high di/dt current paths, to limit capacitive coupling from high dV/dt nodes onto other traces, and to ensure proper GND connections. The layout described here is not the only method for arranging the external components around the device. There can be alternative methods; however, this layout is proven and will most likely provide the best operation of the device due to the optimization of PCB trace inductance and the suggested grounding method. The land patterns used in this layout guide do not imply any specific size or type of component. They are there to simply show the placement of the component in its optimum position with respect to the IC. The LM36274 is a versatile white LED backlight + LCD bias power source and therefore the size and value of the components can vary greatly depending on the operating conditions.

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1 Typical Application Circuit

Figure 1 shows the typical application circuit for the LM36274 with the component names used in this layout guideline document.

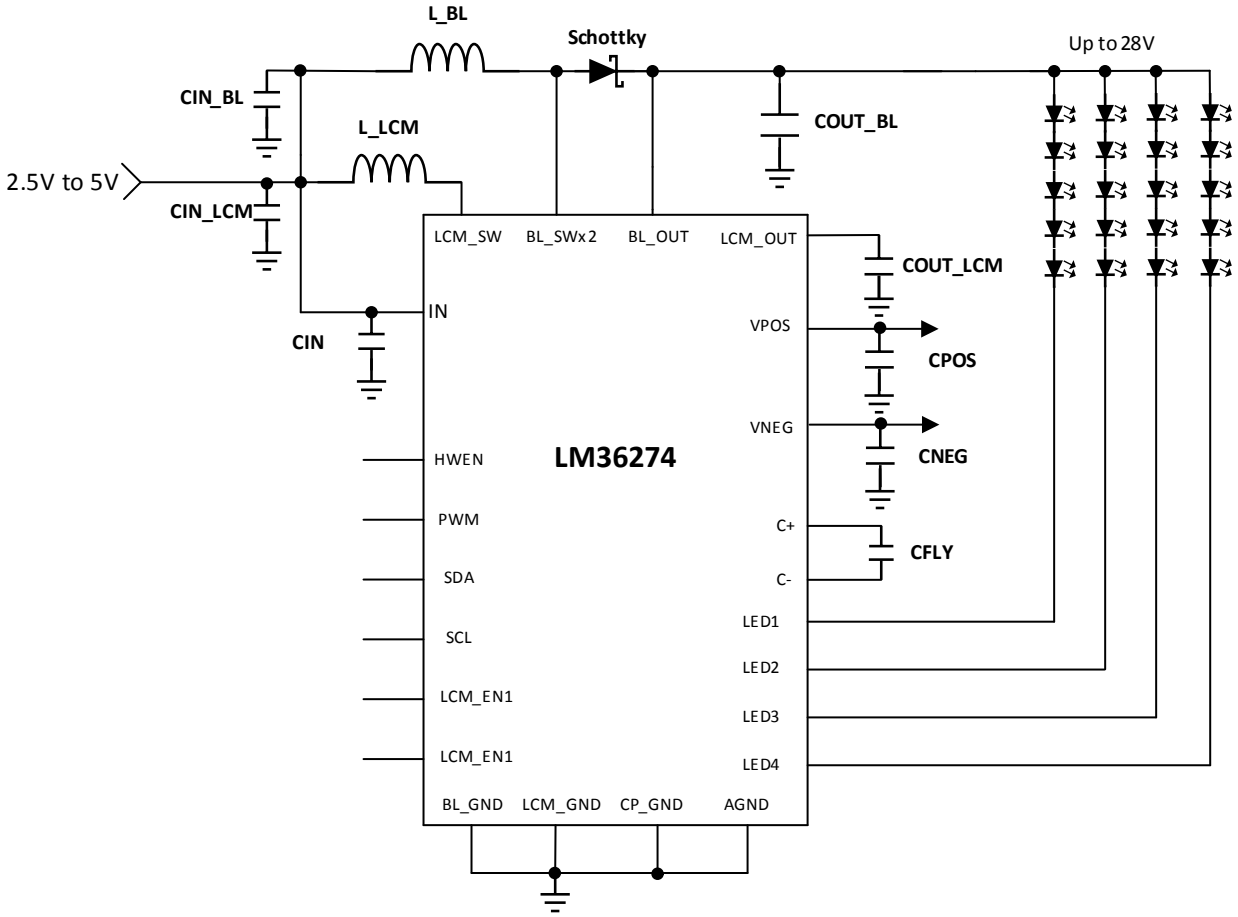

Figure 1. Typical Application Circuit

2 Layout Procedure

The 15 steps in the following sections detail the step-by-step procedure for connecting the external components around the IC beginning with the most important component to the least. Because the backlight boost carries the highest peak current and highest voltage, the layout guidelines begin with the placement of the backlight boost components, most specifically the backlight boost output capacitor.

2.1 Backlight Output Capacitor (COUT_BL)

First, place COUT_BL (or the parallel combination of multiple capacitors) on the same layer as the LM3627X. COUT_BL will carry the highest dI/dt in the circuit. The dI can be up to the peak current of the backlight boost (1.8 A) and dt is around 1ns, therefore a low inductance placement of this component is the most critical. Low inductance means avoiding vias and placing COUT_BL as close as possible to GND and the Schottky diode cathode. The GND side of COUT_BL (COUT_BL-) must connect as close as possible to the BL_GND and LCM_GND bump connection at the IC. The positive terminal (COUT_BL+) is placed so that the Schottky diode cathode and COUT_BL+ have the shortest possible connection.

Figure 2 shows the placement of two parallel capacitors. Having a single capacitor is possible given the single capacitor provides enough capacitance at the operating voltage and temperature. See the LM3627x data sheets for the recommended capacitor values.

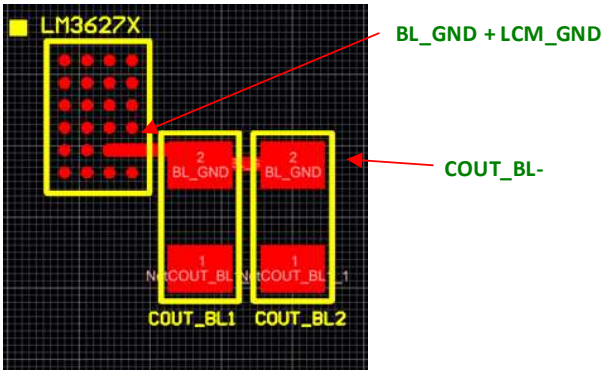

Figure 2. Backlight Output Capacitor Placement

2.2 Schottky Diode

Place the Schottky diode on the same layer as COUT_BL and as close as possible to the (COUT+ terminal and the BL_SW bump). The same discontinuous inductor current that goes through COUT_BL also conducts through the Schottky. Therefore, having a short connection from BL_SW to Schottky anode and from Schottky cathode to COUT_BL+ minimizes the PCB inductance and minimizes any high frequency voltage spikes.

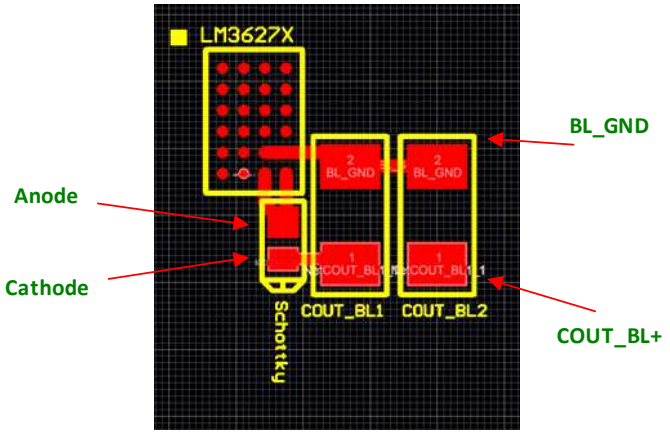

Figure 3. Schottky Diode Placement

2.3 Backlight Inductor Placement

Connect the backlight inductor (L_BL) to the backlight switching node (Schottky anode and BL_SW bump connection). The connection from L_BL to BL_SW should be as small in area as possible in order to reduce possible capacitive coupling to nearby traces and to minimize the capacitance at BL_SW to as little as possible. Any extra capacitance at this node will be extra switching loss in the backlight circuit.

The BL_SW capacitive switching loss is ½ × $C_{SW(TOTAL)}$ × V_{OUT}^2 × f_{SW}, so even 20 pF of extra capacitance can account for over 7 mW, which can lead to a 2% efficiency reduction at light loads.

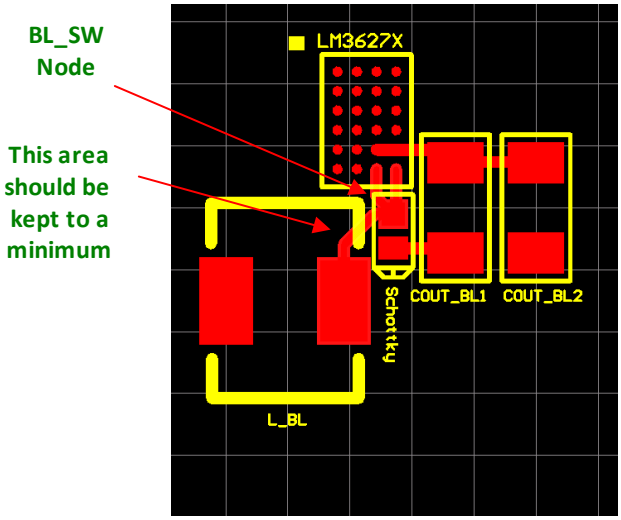

Figure 4. Backlight Inductor Placement

2.4 Backlight Inductor Input Bypass Capacitor (CIN_BL)

Connect an input bypass capacitor (CIN_BL) as close to L_BL(IN) as possible. A close connection to L_BL(IN) are for two main reasons:

1. First, CIN_BL reduces the effect of any inductance seen between the backlight inductor and the input source (VBATT). Inductance between VBATT and the backlight inductor can lead to higher than expected current ripple at the input of L_BL. This ripple comes as a result of an under damped LC circuit between VBATT and L_BL. This underdamped (high Q) circuit can have a resonant frequency near to the switching frequency of the boost.
2. Second, CIN_BL will filter the input ripple generated from the BIAS portion of the LM3627X. When the BIAS portion of the LM3627X is used, it operates in a PFM mode for much of the VPOS and VNEG loading (except high currents). This PFM mode causes a low frequency burst, with a load dependent frequency. This can generate a low frequency voltage ripple at VIN which can appear as a fast line transient at the backlight input. A closely placed CIN_BL will reduce this input disturbance and help prevent noise from being generated on the backlight output. This bypass capacitor works together with CIN_LCM, and when L_BL and L_LCM are place close together the inductors can share their input bypass capacitor

The GND side of CIN_BL can connect down to a lower layer GND plane where it will return back to the BL_GND, LCM_GND connection.

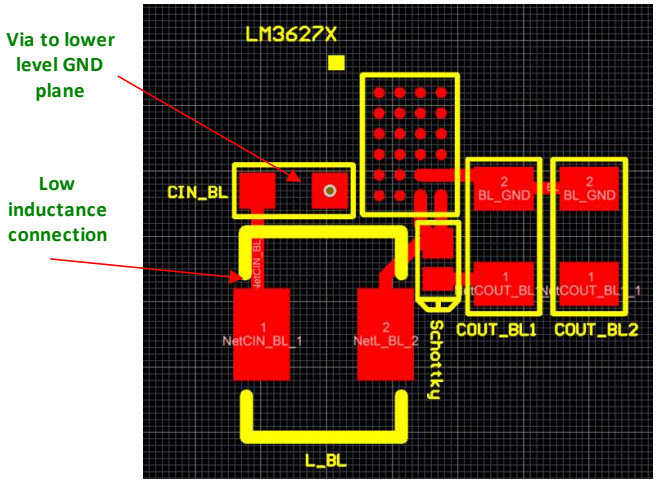

Figure 5. Backlight Inductor Input Bypass Capacitor Placement (CIN_BL)

2.5 BIAS Boost Output Capacitor (COUT_LCM)

Place the BIAS Boost output capacitor positive terminal (COUT_LCM+) as close as possible to the LCM_OUT bump and connect the BIAS boost output capacitor negative terminal as close as possible to (COUT_LCM-). Close placement of this capacitor minimizes the inductance seen in series with COUT_LCM. This path carries the discontinuous LCM boost inductor current which can have a high di/dt. The di can be as high as the peak inductor current of the LCM_BOOST (around 1A) and dt can be < 1 ns. Reducing the inductance in series with this discontinuous current minimizes the high frequency voltage spike generated at LCM_OUT.

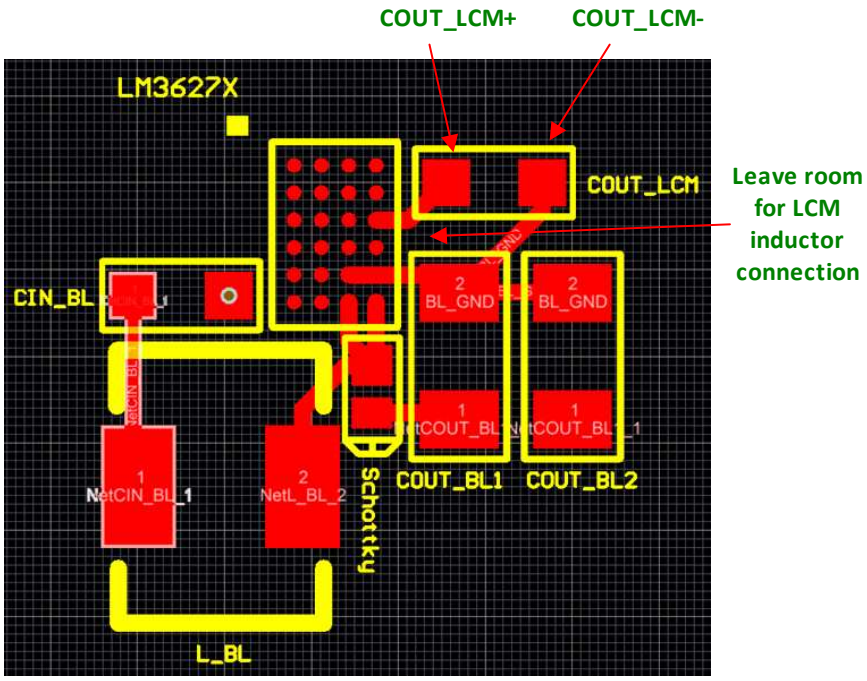

Figure 6. BIAS Boost Output Capacitor Placement (COUT_LCM)

2.6 BIAS Boost Inductor (L_LCM)

Connect the LCM inductor (L_LCM) to the LCM_SW bump. The connection from L_LCM to LCM_SW should be as small in area as possible in order to reduce possible capacitive coupling to nearby traces and to minimize the capacitance at LCM_SW to as little as possible. The same reasoning that applies to the L_BL also applies to L_LCM with regards to extra PCB capacitance and efficiency reduction.

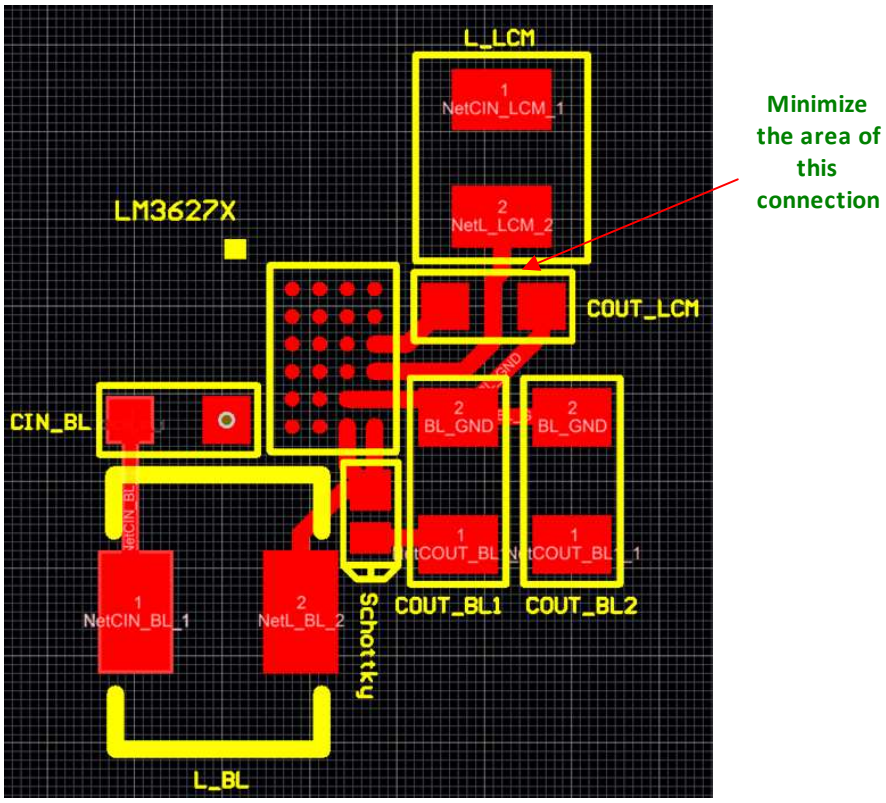

Figure 7. BIAS Boost Inductor Placement (L_LCM)

2.7 BIAS Boost Input Capacitor (CIN_LCM)

Connect an input bypass capacitor (CIN_LCM) as close as possible to the input of L_LCM. (CIN_LCM+) must connect very close to the inductor input. The GND side of CIN_LCM can via down to the lower lavel GND plane. CIN_LCM is necessary for two reasons:

1. First, CIN_LCM reduces the effect of any inductance seen between the BIAS inductor and the input source (VBATT). Inductance between VBATT and L_LCM can lead to higher than expected current ripple at the inductor input. This ripple comes as a result of an underdamped LC circuit between VBATT and the inductor. This underdamped (high Q) circuit can have a resonant frequency near to the switching frequency of the boost.
2. Second, CIN_LCM helps filter the input ripple generated from the BIAS boost of the LM3627X. When the BIAS portion of the LM3627X is used, it operates in a PFM mode for much of the VPOS and VNEG loading (except high currents). This PFM mode causes a low frequency burst, with a load dependent frequency. This can generate a low frequency voltage ripple at VIN. A closely placed CIN_LCM reduces this input disturbance and help prevent noise from being generated on the input. This bypass capacitor works together with CIN_BL. If L_BL and L_LCM are place close together the inductors can share a single input bypass capacitor.

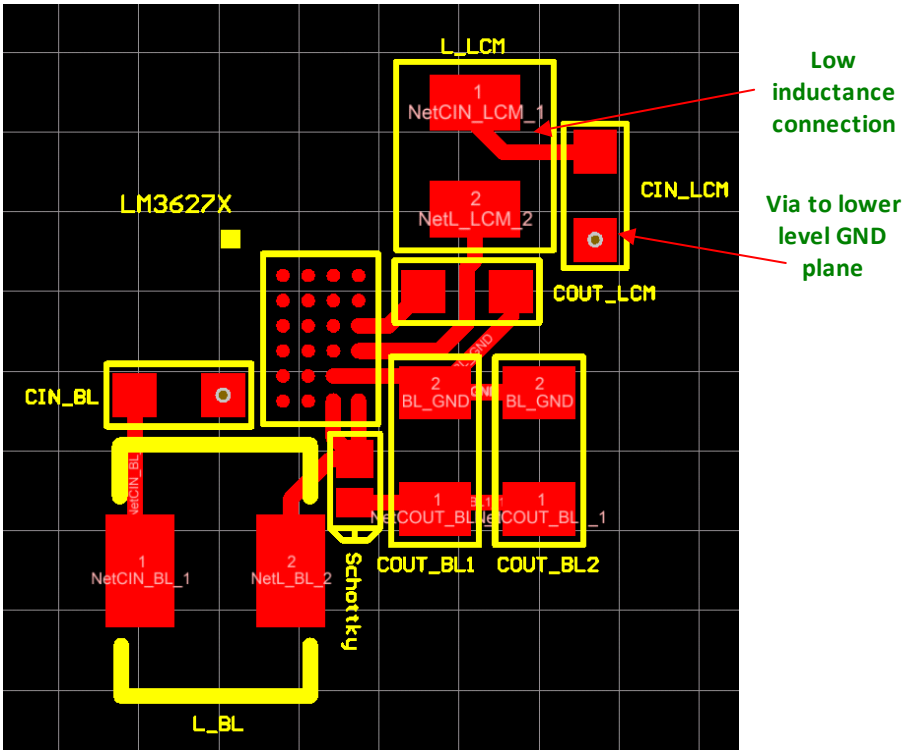

Figure 8. BIAS Boost Input Capacitor Placement (CIN_LCM)

2.8 Flying Capacitor (CFLY)

Connect the flying capacitor for the negative charge pump as close as possible to the C- and C+ bumps. The flying capacitor can have a high di/dt (up to 1A/ns). Minimizing the connections from the C+ and C- bumps minimizes this inductance and reduce the conducted noise. Additionally, limiting this connection length limits the area of the PCB trace and thus minimize the added PCB capacitance and help maximize efficiency in th BIAS supply.

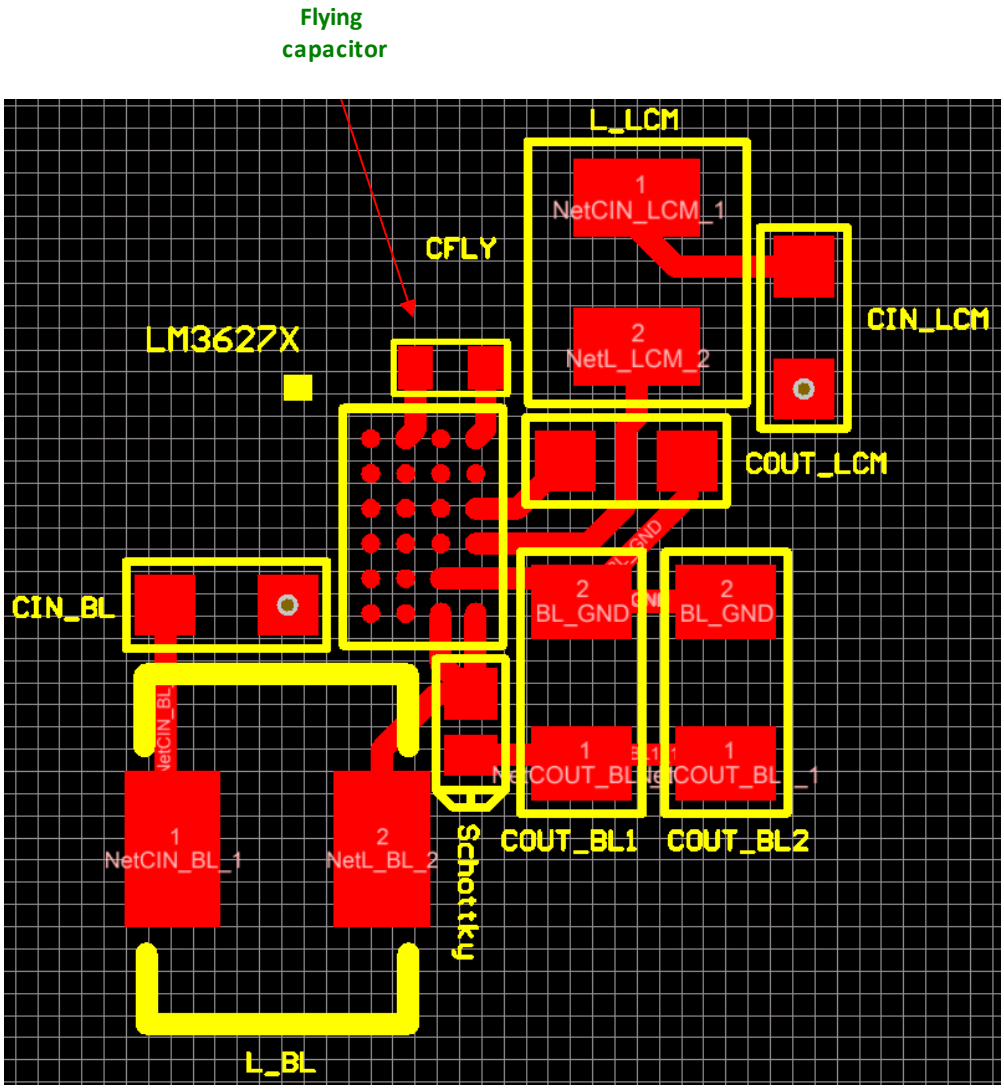

Figure 9. Flying Capacitor Placement (CFLY)

2.9 VNEG Output Capacitor (CNEG)

Connect the inverting charge pump output capacitor (CNEG) as close as possible to the NEG bump. This capacitor can see relatively high di/dt when VNEG is active. Limiting the connection from NEG to CNEG+ limits the high frequency noise generated from the charge pump onto the VNEG line. The GND side of this capacitor can via down and connect back to CP_GND through a lower level layer. The connection from CNEG– to CP_GND should be routed as short as possible.

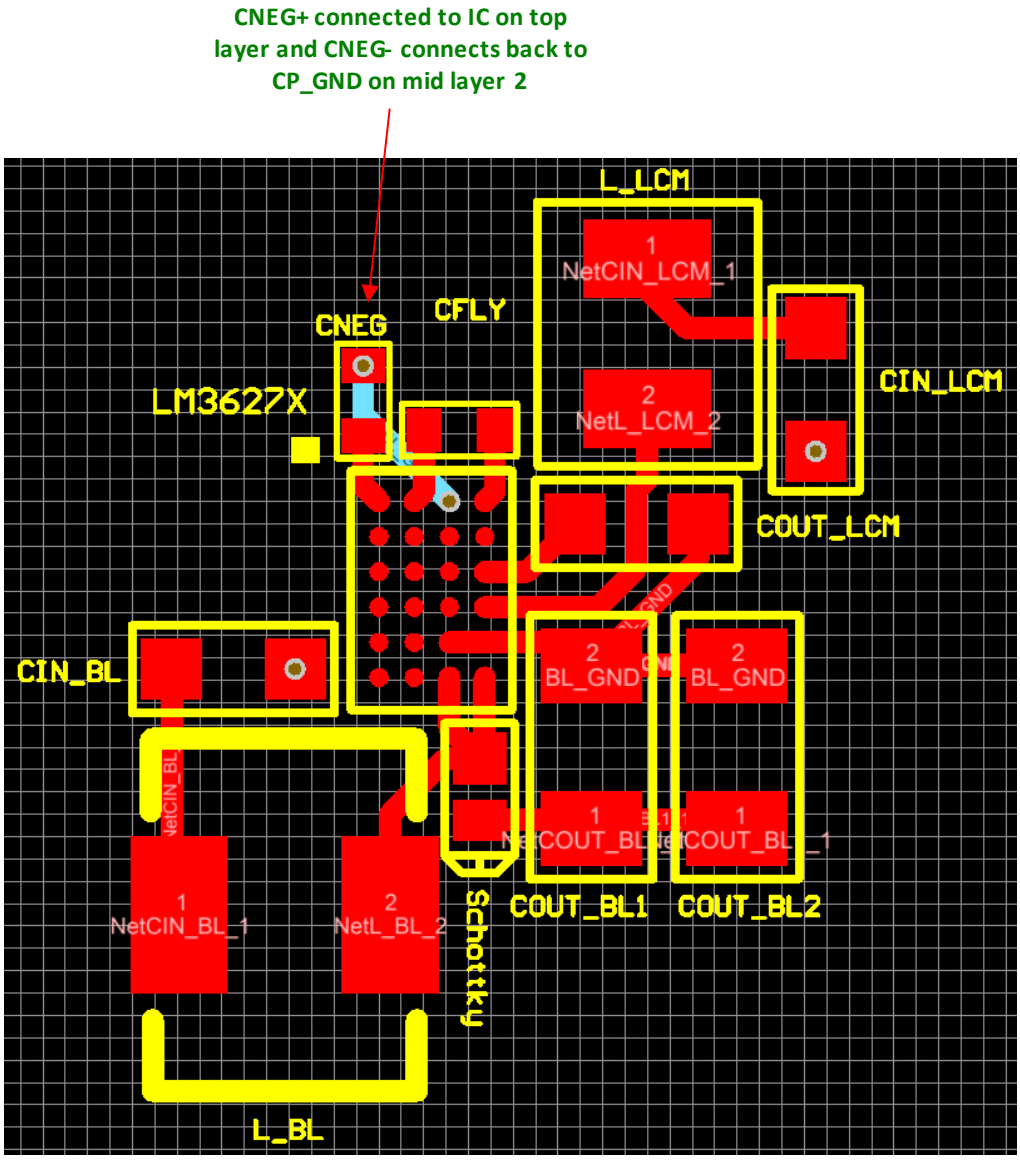

Figure 10. Inverting Charge Pump Output Capacitor Placement (CNEG)

2.10 Positive LDO Output Capacitor(CPOS)

Connect CPOS as close to the part as possible. CPOS can connect to the POS bump and to CP_GND through vias on a lower level plane. This is the least critical component in the BIAS power path because of its continuous output and GND current, although close placement of this capacitor to the IC minimizes the trace area of the CPOS+ and CPOS– connection and help reduce any possible conducted noise generated due to the LCM BIAS boost switching and capacitively coupled noise from LCM_SW.

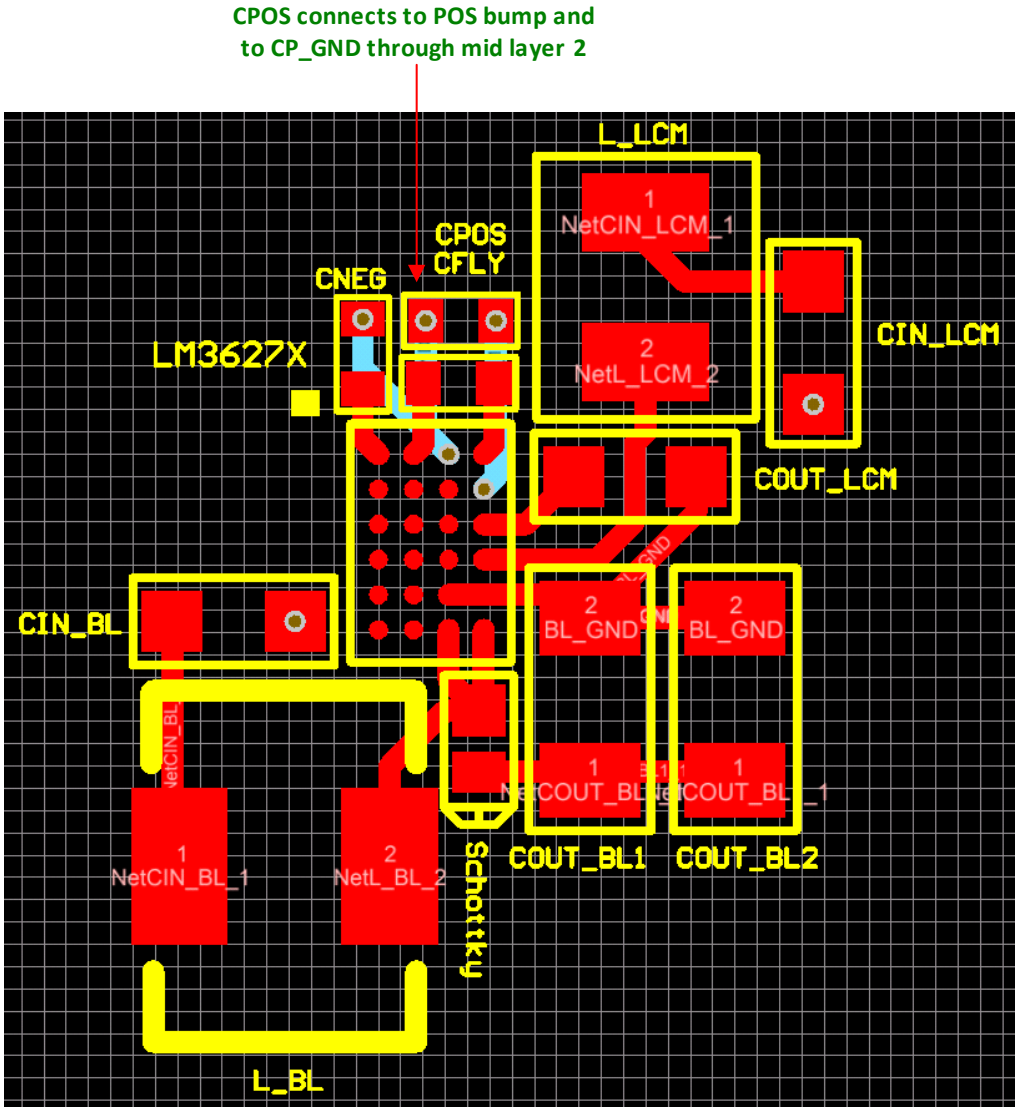

Figure 11. Positive LDO Output Capacitor Placement (CPOS)

2.11 Input Bypass Capacitor (CIN)

Connect the input bypass capacitor CIN as close as possible to IN. CIN+ connects directly to the IN bump of the device. CIN– can via down to the lower level GND plane. This capacitor provides for a low impedance path for the driver circuits in the LM3627x; therefore, placing CIN very close to the device ensures the lowest impedance source for the fast di/dt required for the IC's FET drivers.

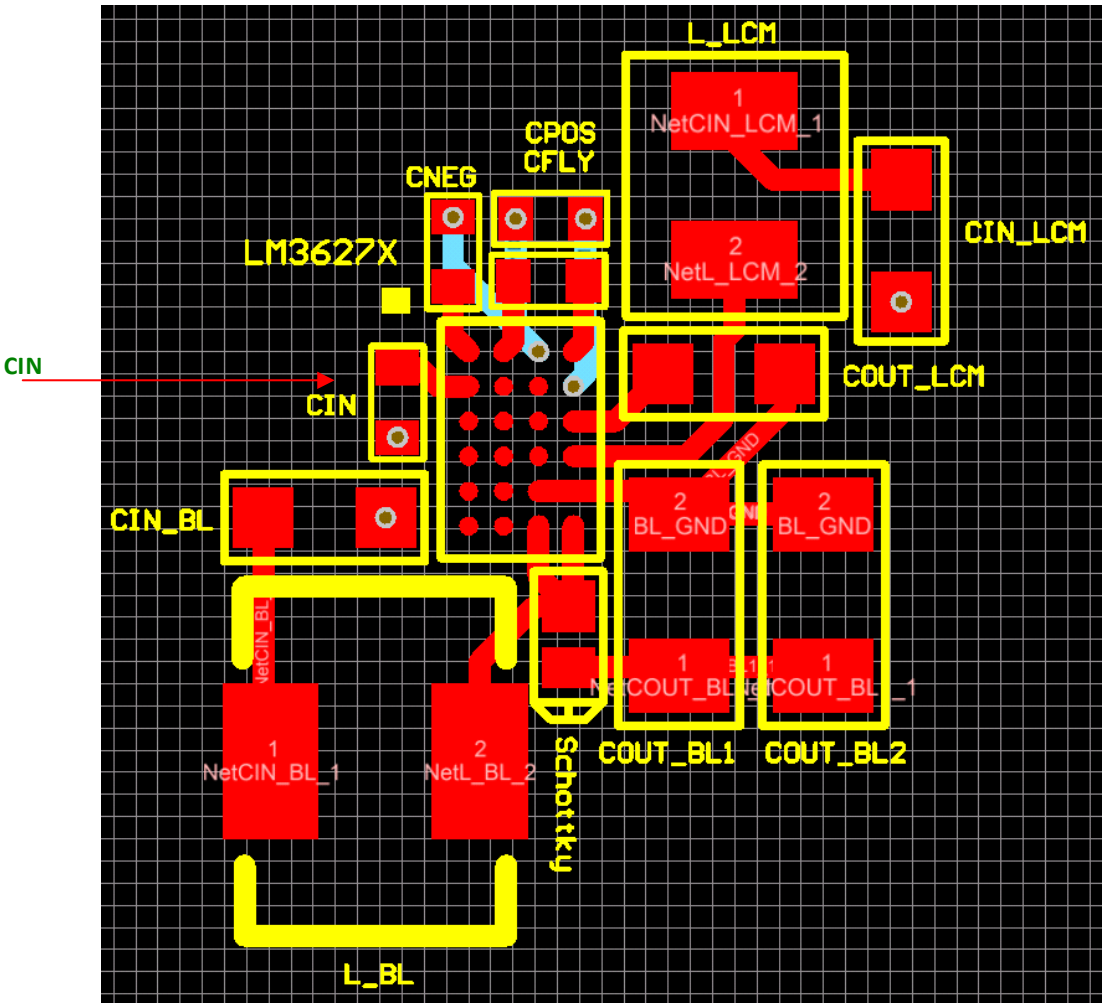

Figure 12. IN Bypass Capacitor Placement (CIN)

2.12 Mid Layer Ground Plane

Connect CIN_BL–, CIN–, CP_GND, BL_GND, LCM_GND, and CIN_LCM– to a lower level GND plane. This GND plane should go directly underneath the BL_SW and the LCM_SW. This creates a distributed PCB capacitance directly underneath the high dV/dt switching nodes and provides for a low impedance to GND for these high frequency voltages. Additionally, placing the GND plane directly beneath the BL_SW and LCM_SW prevents any traces from being placed underneath these high dV/dt nodes, which can lead to unwanted capacitive coupling and interference.

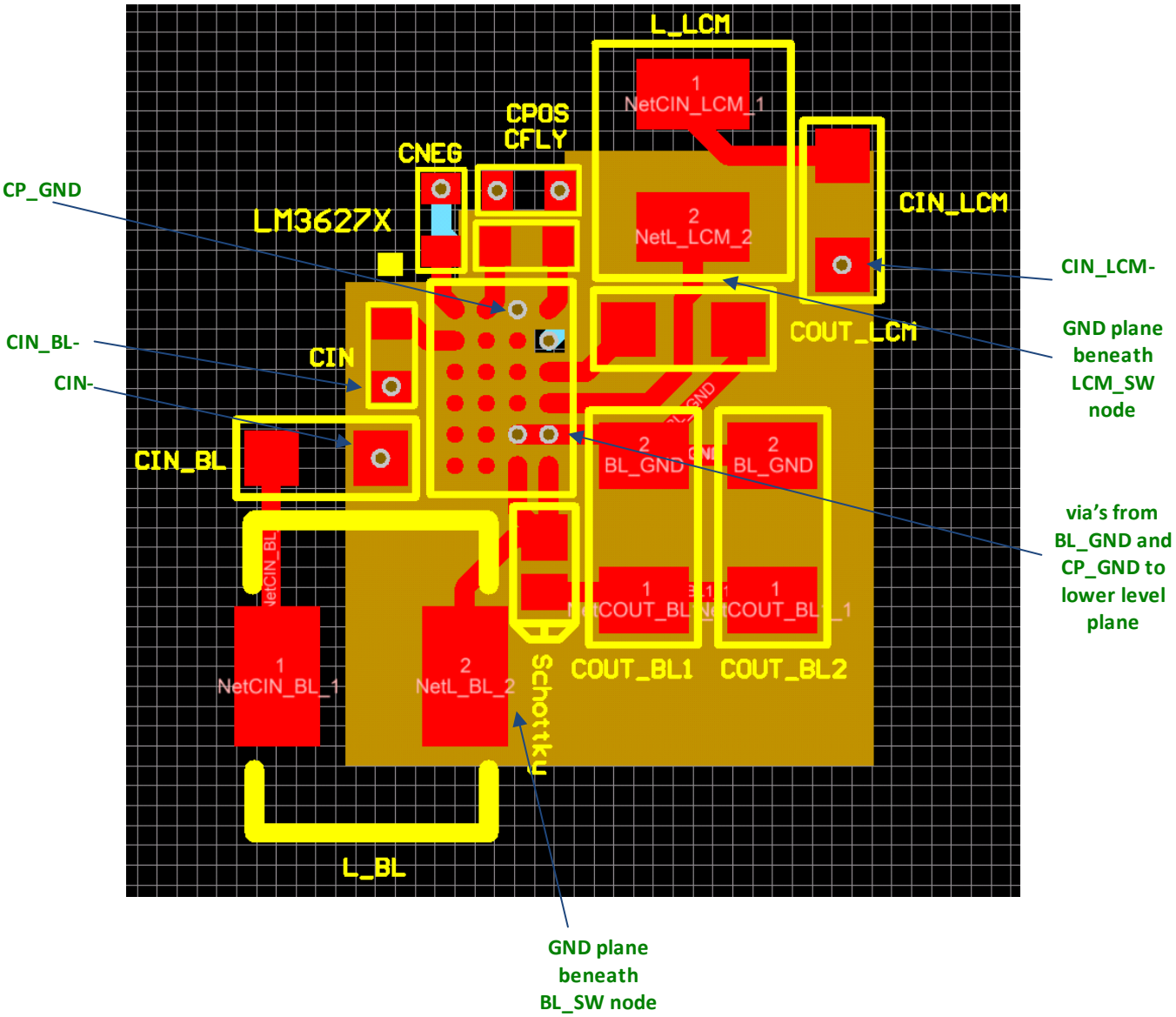

Figure 13. Connecting to the Mid Layer GND Plane

2.13 AGND Connection

13. Connect AGND to the LCM_GND, and BL_GND. AGND can connect directly to LCM_GND on the top layer (as shown in Figure 14) or AGND can connect directly to the lower level GND plane along with LCM_GND and BL_GND. The important thing to ensure is that the return current of the power devices (COUT_BL, COUT_LCM, CIN_BL, CIN_LCM, CIN, and CP_GND have a low impedance path back to BL_GND and LCM_GND. This path should not share any current between AGND and the LCM_GND/BL_GND connection.

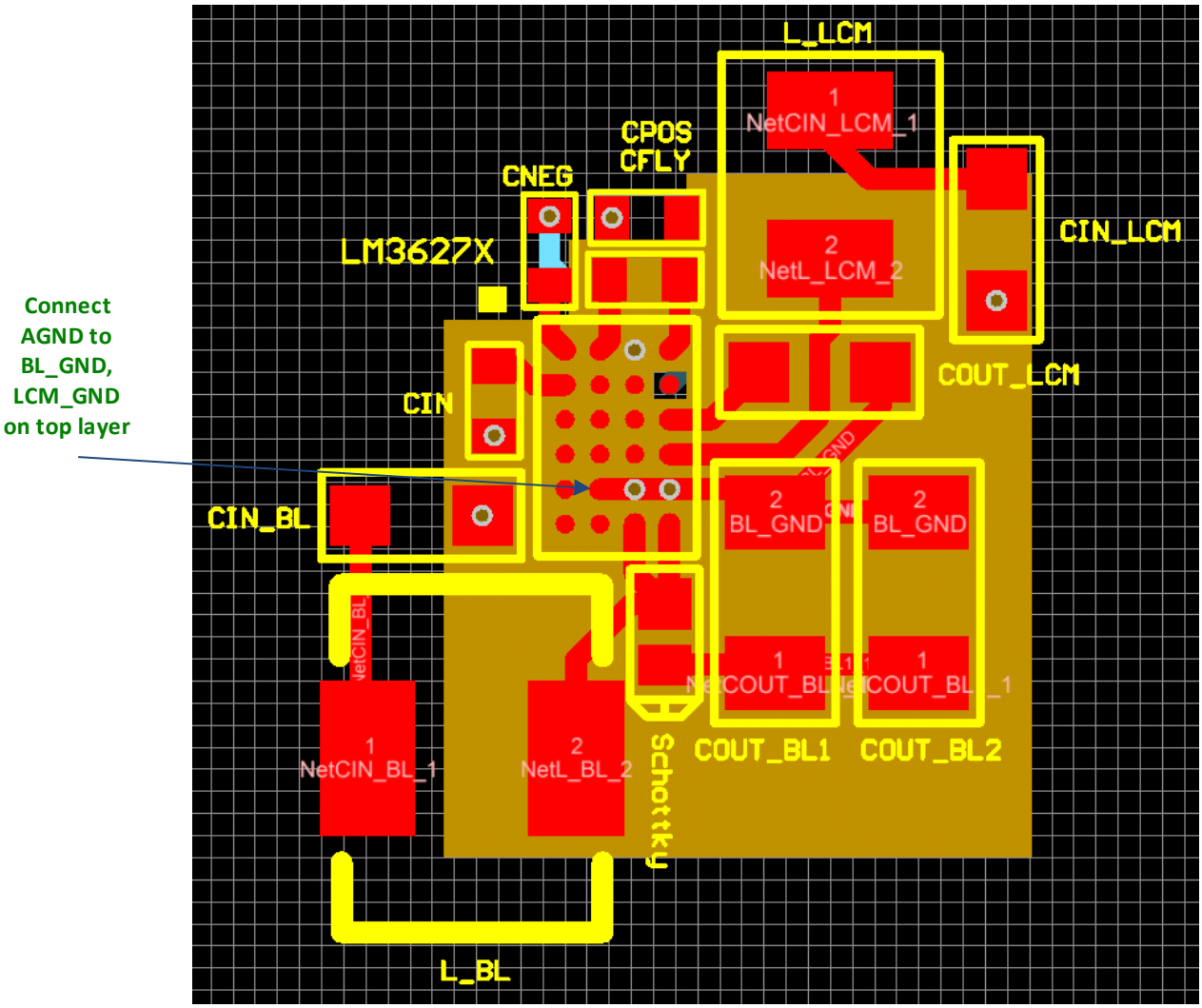

Figure 14. Connecting AGND to the Power Ground (BL_GND and LCM_GND)

2.14 Adding More Vias

Add more via's to further decrease the impedance between the top layer GND nodes and the mid layer GND plane.

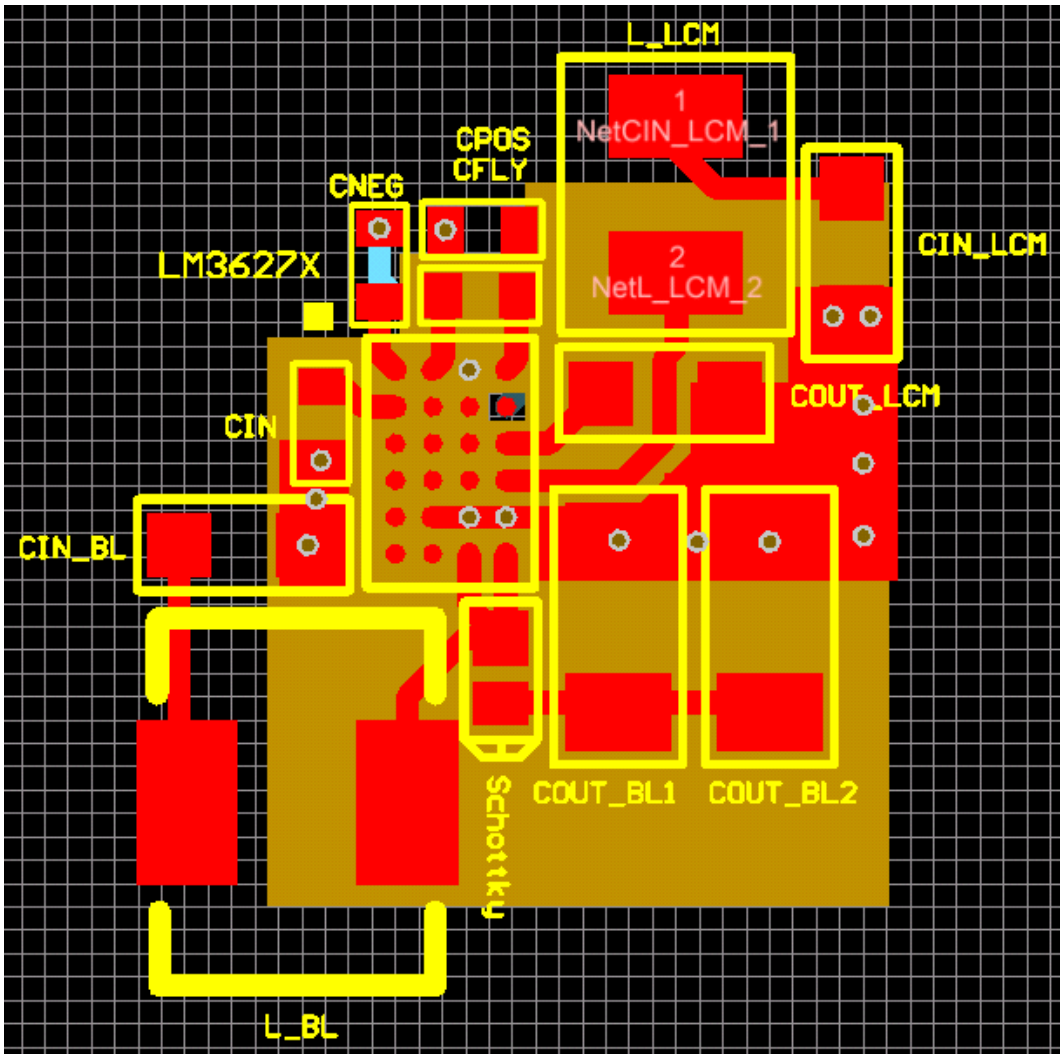

Figure 15. Via's Connecting BL_GND/LCM_GND to Mid Layer Plane

2.15 Connect BL_OUT to COUT_BL+

Connect the positive terminal of the backlight output capacitor to the BL_OUT bump. BL_OUT serves as the sense for overvoltage (OVP). BL_OUT is a high impedance input, so a short connection is not critical. However placing the lower level GND plane beneath the BL_OUT to COUT_BL+ trace prevents coupling from BL_SW.

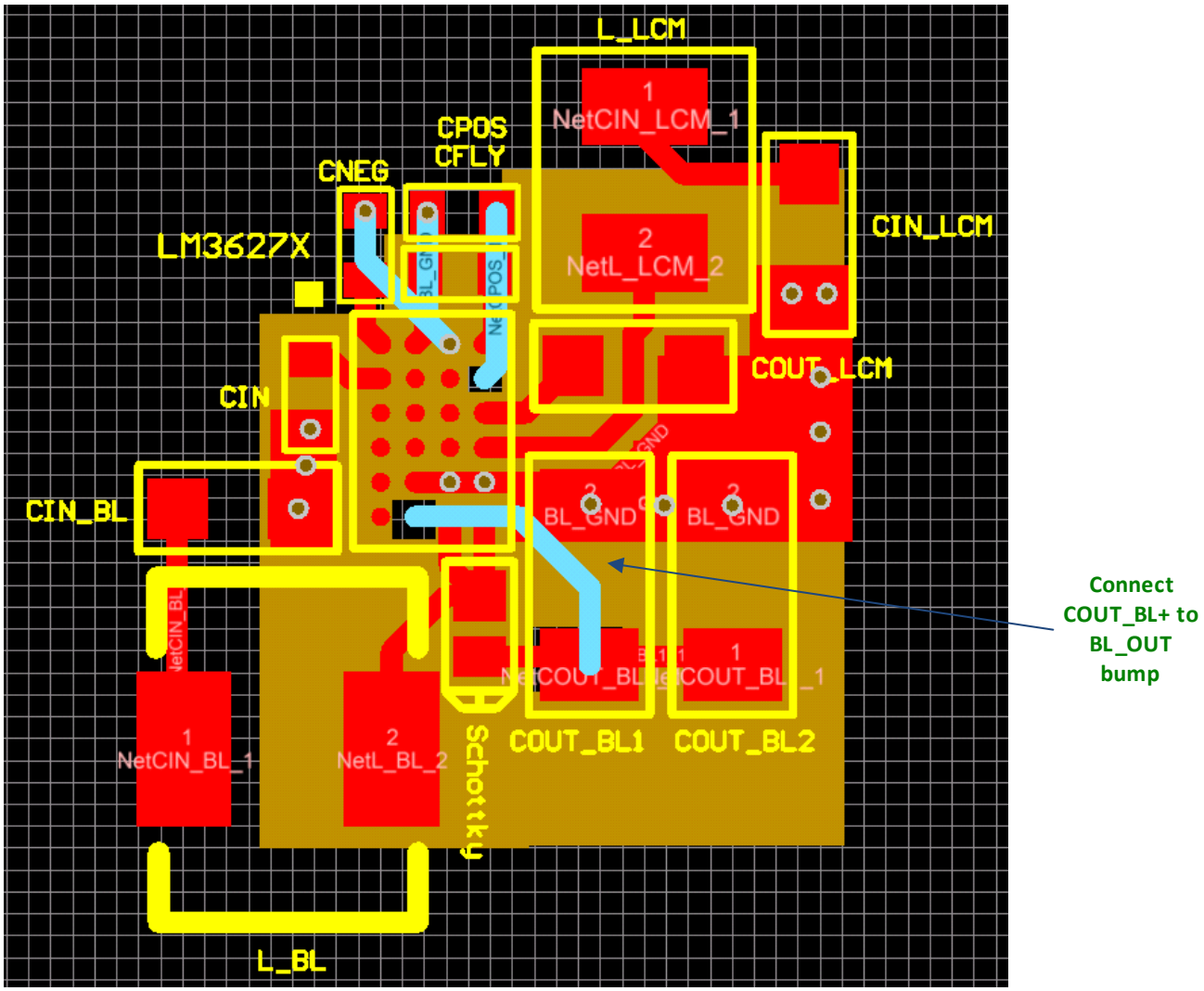

Figure 16. Connecting Backlight Output Sense

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