Application Report
SNVA793–September 2017

How to Evaluate the Maximum Inductor in an Internal Compensation PCM Buck Converter

Vincent Zhang

ABSTRACT

With simple frequency compensation, *Peak Current Mode* (PCM) control is commonly used in integrated circuits (IC) to improve the line and load transient performance. Slope compensation is implemented to prevent sub-harmonic oscillations at a duty cycle greater than 50%. Usually the inductor is considered as a current source in a simplified PCM buck converter model, which actually has a significant impact of the main pole as well as whole loop Bode plot. This application report provides detailed analysis of the inductance impact in an accurate PCM buck converter, explains how the phase margin is reduced by the inductor pole, and inductance design based on a practical IC is presented.

The features of peak current mode control are described in Section 1. Section 2 provides simplified and accurate PCM buck converter modeling. Inductor design based on LMR14020-Q1 is calculated in Section 3. Finally, Section 4 shows the Mathcad® calculations, Simplis® simulations, and bench tests to verify the theory.

Contents

List of Figures

List of Tables

Trademarks

Mathcad is a registered trademark of PTC, Inc..
Simplis is a registered trademark of SIMetrix Technologies Ltd..
All other trademarks are the property of their respective owners.

1 Peak Current Mode Introduction

Peak Current Mode (PCM) control is a popular control mode, benefitting low cost and stability. Compared to average current mode control, PCM control simplifies the internal current loop compensation, making it popular for use in an IC.

PCM employs a current-sampling RAMP to compare with the output of the *Error Amplifier* (EA), to generate the regulated duty cycle. PCM also benefits the fast response by input or load transient, with current and voltage loops to realize higher crossover frequency.

2 Simplified and Accurate PCM Buck Converter Modeling

2.1 Simplified Transfer Function

Figure 1 shows the PCM implementation block diagram including three parts, voltage divider, error amplifier, and switching modulator.

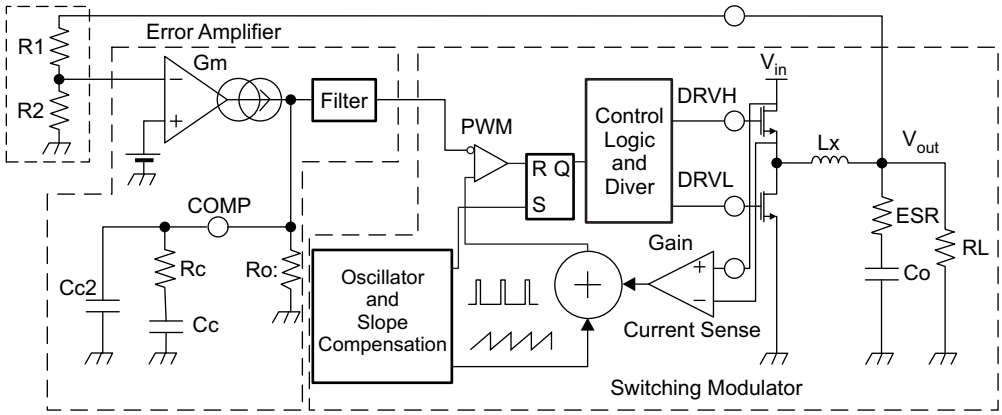

Figure 1. PCM Implementation

Considering the inductor current ripple is 20% smaller than the load, the inductor could be simplified to a current source here. The simplified *Current Mode Control* (CMC) block diagram is shown in Figure 2. G_{vi} is the ratio of compensation voltage to inductor current.

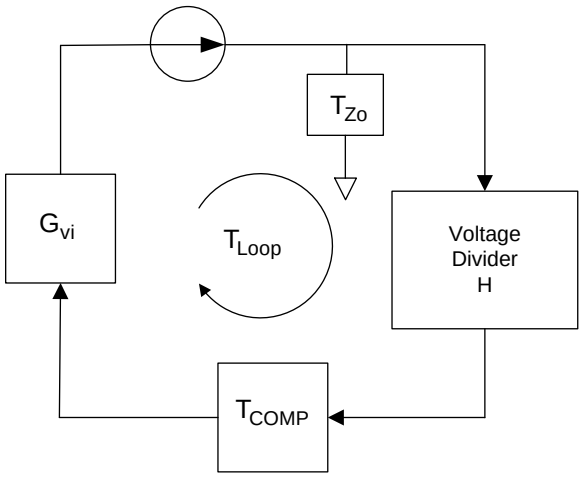

Figure 2. Simplified CMC Block Diagram

Comparing the *Figure 1* and *Simplified CMC Block Diagram*, the transfer function of the voltage divider is shown in Equation 1:

$$H = \frac{R_1}{R_1 + R_2} \quad (1)$$

where

- R_1 and R_2 are the feedback resistor

The transfer function of EA is shown in Equation 2:

$$T_{comp} = G_m \times \left(R_c + \frac{1}{s \times C_c} \right) // \frac{1}{s \times C_{c2}} \quad (2)$$

where

- G_m is gain of EA
- R_c ,C_c, and C_{c2} are the internal compensation network

The transfer function of the output impedance is shown in Equation 3:

$$T_{zo} = R_L // \left(ESR + \frac{1}{s \times C_o} \right) \quad (3)$$

where

- R_L is effective load resistor
- C_o is total output capacitor

Combine Equation 1 through Equation 3 and G_{vi}, the transfer function of the loop is shown in Equation 4:

$$T_{Loop\_simplified} = H \times T_{comp} \times G_{vi} \times T_{zo} \quad (4)$$

Equation 4 shows the transfer function of the main circuit has two poles and one zero. The first pole is at zero frequency and the other is generated by output capacitor and load. The zero is contributed by the internal RC compensation. This structure makes the gain curve go across 0 dB with –20 dB/dec slew rate and obtain enough phase margin. However, in practical circuits the inductor also brings in a pole, making the simplified CMC phase margin higher than the measured value.

2.2 Slope Compensation and Sample Hold Modeling

Simplified CMC has two simplifications: one is ignoring the inductor ripple to consider the inductor as a current source, the other is to use the simple on-resistor of the high side switch to indicate the current sense gain.

In a practical PCM circuit, a slope compensation is usually required to avoid the sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of the next switching cycle. Further, the current mode control exhibits characteristics which can only be explained with the discrete-time modeling, so it is necessary to model the current-sampling function and converted into continuous-time representation and combined with the rest of the power stage and feedback modes.

Figure 3 is the PCM overall control implementation. The inductor current (i_L) disturbance includes two parts: input voltage and duty cycle, which is generated by the comparison of a current sampling RAMP and the output of the EA.

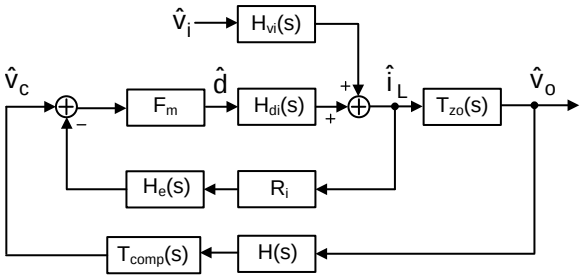

Figure 3. Overall Control Implementation

Where

- $H_{vi}(s)$ is the input to i_L transfer function
- $H_{di}(s)$ is the duty cycle to i_L transfer function
- R_i is the current sample resistor
- $H_e(s)$ is the sample-and-hold system gain function
- $T_{comp}(s)$ is the gain function of the error amplifier
- H(s) is the gain of the divided resistor network

As the current waveform is in conjunction with the external ramp, the modulator gain of the circuit F_m is:

$$F_m = \frac{1}{(S_n + S_e) \times T_s} \quad (5)$$

where

- T_s is the switching period
- S_n is the on-time slope of the sensed-current waveform
- S_e is the external ramp

The accurate transfer function of the loop is shown in Equation 6:

$$T_{Loop\_simplified} = H \times T_{comp} \times H_{comp2I} \times T_{zo} \quad (6)$$

The transfer function of compensation to inductor current and sample-hold are shown in Equation 7 and Equation 8:

$$H_{comp2I} = \frac{F_m \times H_{di}(s)}{1 + F_m \times H_{di}(s) \times H_e(s) \times R_i} \quad (7)$$

$$H_e(s) = \frac{T_s \times S}{e^{Ts \times S} - 1} \approx 1 - \frac{S}{2/T_s} + \frac{S^2}{(\pi/T_s)^2} \quad (8)$$

2.3 Inductance Impact of Accurate PCM Buck Converter

At the low frequency period, $H_{di}(s)$ could be simplified to V_{IN} / (sL) and $H_e(s)$ is 1, Equation 7 can be simplified to Equation 9.

$$H_{comp2I\_simplified} = \frac{F_m \times V_{IN}}{sL + F_m \times V_{IN} \times R_i} \tag{9}$$

The inductor pole is located at:

$$f_{pole\_L} = \frac{1}{2\pi} \times \frac{F_m \times V_{IN} \times R_i}{L_f} = \frac{1}{2\pi} \times \frac{V_{IN} \times R_i}{(V_{IN} - V_{OUT}) \times R_i \times T_s + S_e \times T_s \times L_f} \tag{10}$$

From Equation 10, it is observed that the LC double pole is divided into two separate poles by enlarging the inductor pole to high frequency, that is why the current mode could be considered as a one-order system for easier compensation than voltage mode control. If the slope compensation is too much, which means either S_e or the inductor is too large, the pole will locate around the output capacitor pole, then the current mode control is like the voltage mode control and the loop becomes unstable.

3 Inductor Design

This section introduces the inductor design based on LMR14020QDPR.

3.1 Bode Plot of Simplified PCM Converter

The system level parameters are shown in Table 1.

Table 1. System Parameters

Parameter	Example Value
Input voltage, V_{IN}	12 V_{DC}
Output voltage, V_{OUT}	5 V_{DC}
Maximum output current , I_{O_MAX}	2 A_{DC}
Switching frequency, F_{SW}	1000 kHz
Output capacitor, C_{OUT}	47 µF

According to the output and reference voltage, the voltage divider here is:

$$H = \frac{V_{ref}}{V_{OUT}} = \frac{0.75}{5} = 0.15$$

where

- V_{ref} is the reference voltage of LMR14020QDPR (11)

LMR14020QDPR has an internal RC compensation. The EA gain is 40 µA/V and R = 360 kΩ, C = 60 pF, so the transfer function of EA T_{comp} is:

$$T_{comp} = G_m \times \left(R + \frac{1}{sC}\right) = 40 \times \left(360 \times 10^3 + \frac{1}{s \times 60 \times 10^{-12}}\right) \quad (12)$$

The output capacitor is GRM32ER61C476ME15L, which is a 47-µF, 16-V, X5R ceramic capacitor with 4-mΩ ESR. So, the output impedance is:

$$T_{zo} = \left(ESR + \frac{1}{s \times C_{OUT}}\right) // R_L = \frac{\left(4 \times 10^{-3} \times 47 \times 10^{-6} \times s + 1\right) \times 2.5}{1 + \left(4 \times 10^{-3} + 2.5\right) \times 47 \times 10^{-6} \times s} \quad (13)$$

G_{vi} of LMR14020QDPR is 5.1, combining Equation 11–Equation 13, the calculated loop response is plotted as Figure 4 shows:

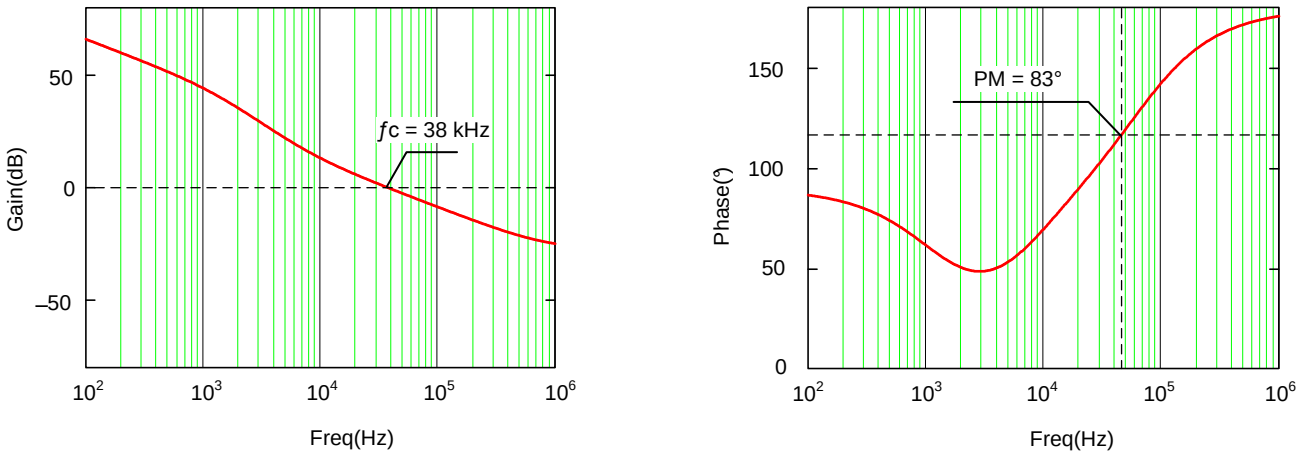

Figure 4. Calculated Bode Plot of Simplified Model

Build a Simplis model to verify the calculated Bode plot. Figure 5 and Figure 6 are the simulation schematic and results. Comparing Figure 4 and Figure 5, observe that simulation results and calculated results match with each other very well.

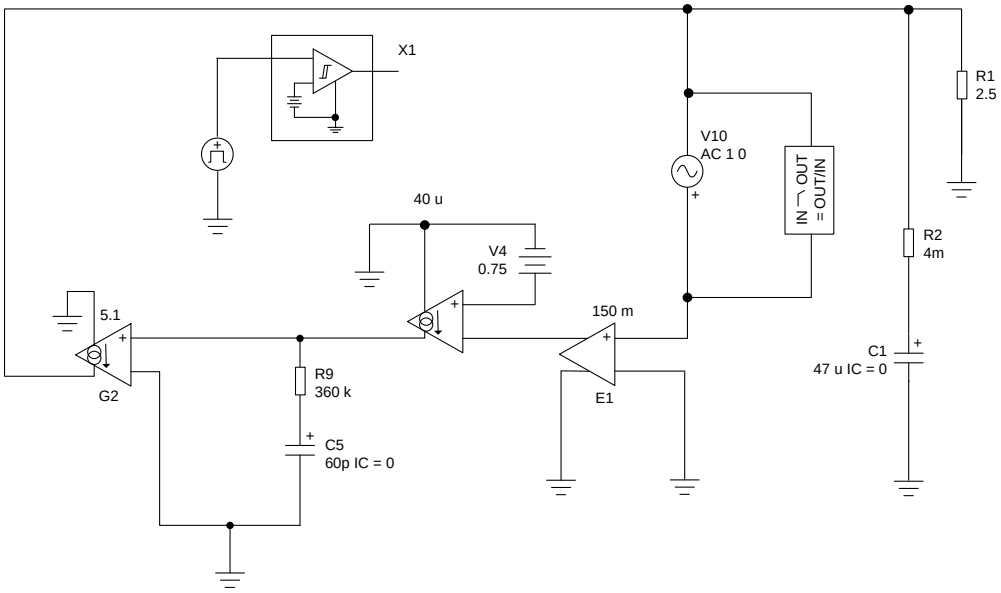

Figure 5. Simplified PCM Simplis Model Schematic

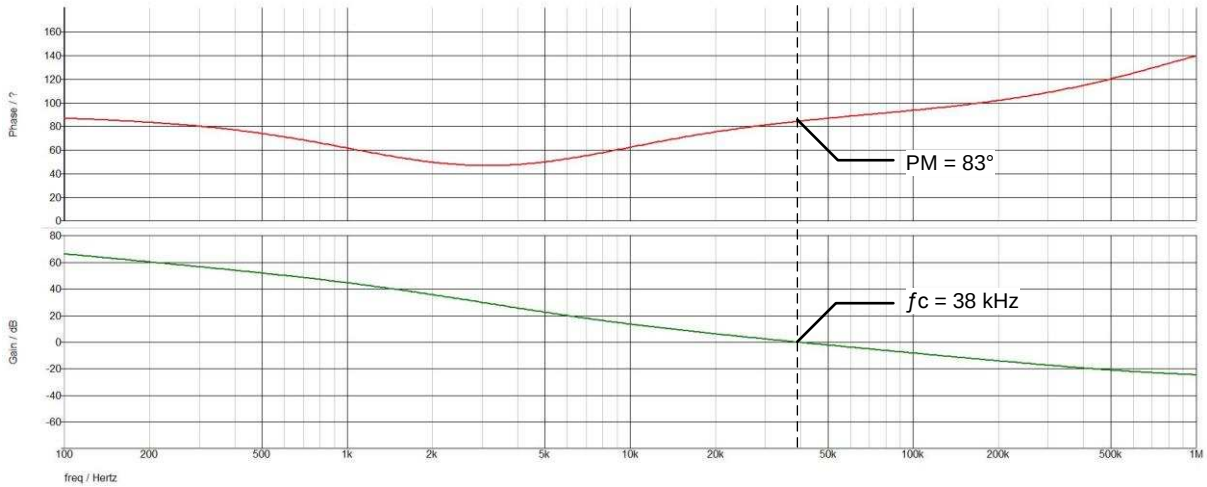

Figure 6. Simplified Model Simulation Results

3.2 Inductor Design

Figure 7 is a diagram of a simplified model Bode plot. The diagram shows a pole generated by output capacitor and load, and the zero generated by internal RC compensation. The gains are:

$$G_1 = 20\log\left(\frac{V_{ref}}{V_{OUT}}\right) + 20\log(G_{vi}) + 20\log(G_m \times R_c) + 20\log(R_L) + 20\log\left(\frac{C_{OUT} \times (ESR + R_L)}{R_c \times C_c}\right) = 43.5\,dB \quad (14)$$

$$G_2 = 20\log\left(\frac{V_{ref}}{V_{OUT}}\right) + 20\log(G_{vi}) + 20\log(G_m \times R_c) + 20\log(R_L) - 20\log\left(\frac{C_{OUT} \times (ESR + R_L)}{R_c \times C_c}\right) = 14.1\,dB \quad (15)$$

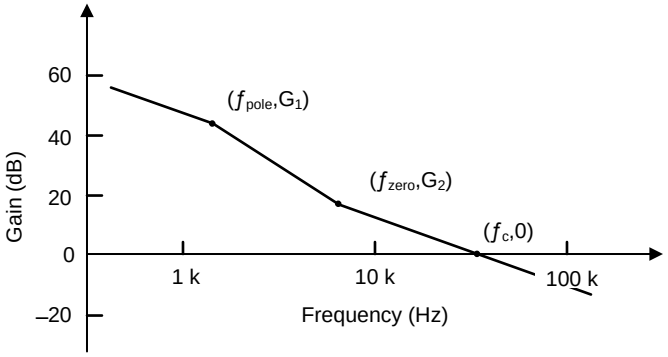

Figure 7. Simplified Model Bode Plot Diagram

In a simplified model, the inductor is considered as a current source, the gain curve goes across 0 dB with –20 dB/dec slew rate, so the crossover frequency is no relative with inductance. f_c is derived in Equation 16:

$$f_c = 20\log(G_m \times R_c) + 20\log\left(\frac{C_{OUT} \times (ESR + R_L)}{R_c \times C_c}\right) = 37.2\ kHz \quad (16)$$

In an accurate model, the inductor generated a pole, the gain curve slew rate decreases to –40 dB/dec. If the gain curve goes across 0 dB with –40 dB/dec slew rate, there will not be enough phase margin for the system, so the pole frequency generated by the inductor should be smaller than f_c, maximum inductance is derived in Equation 17:

$$L_{f\_max} = \frac{1}{2\pi} \times \frac{F_m \times V_{IN}}{G_{vi} \times f_c} = 9.7\ \mu H \quad (17)$$

Table 2 lists different inductances for comparison, and calculated Bode plots are compared in Figure 8. It is obvious that an inductor brought in one pole makes the phase margin smaller than the simplified model. Further, if the pole frequency is smaller than f_c, the phase margin will not be enough.

Table 2. Different Inductance Comparison

Inductance (µH)	Simplified fc (kHz)	Simplified PM (°)	Inductance Pole (kHz)	Accurate fc (kHz)	Accurate PM (°)
2.2	37.2	83	164.3	37.32	70.63
10	37.2	83	36.98	29.65	41.29
22	37.2	83	16.4	22.9	22.74
47	37.2	83	7.69	16.9	6.62

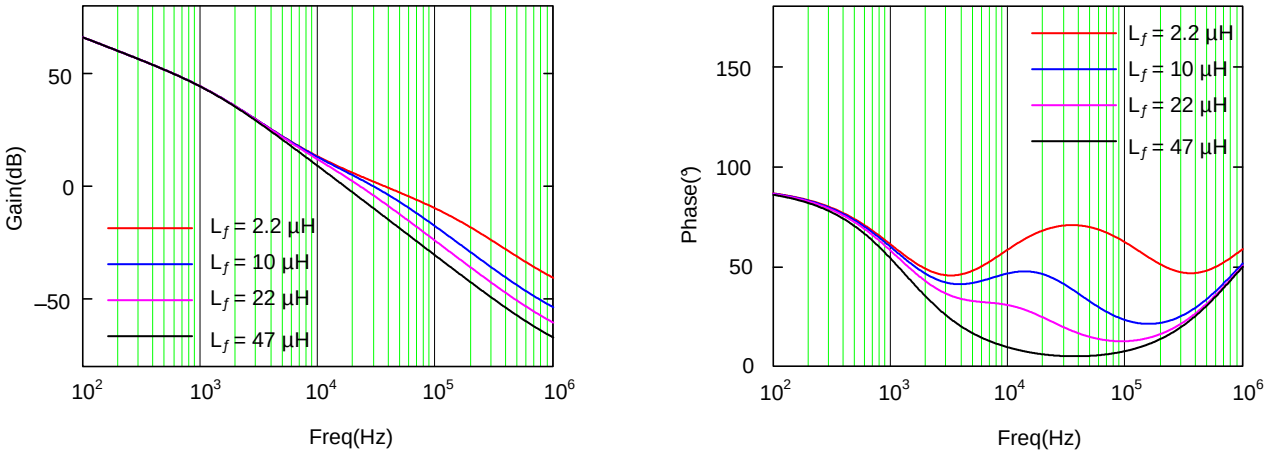

Figure 8. Bode Plot of Different Inductors

4 Bench Verification

Figure 9 and Figure 10 are the schematic of the evaluation module (EVM) and Simplis model. In order to match with the practical bench setup, make the following modifications in the simulation model:

1. Add an input LC filter to simulate practical long input cables and capacitors
2. Change the output capacitor to 33 µF/50 mΩ according to the DC bias rating and ESR-frequency curve
3. Modify the EA Gain to 45 µA/V to compensate the temperature variation
4. Add feedback to the GND capacitor to simulate the practical situation

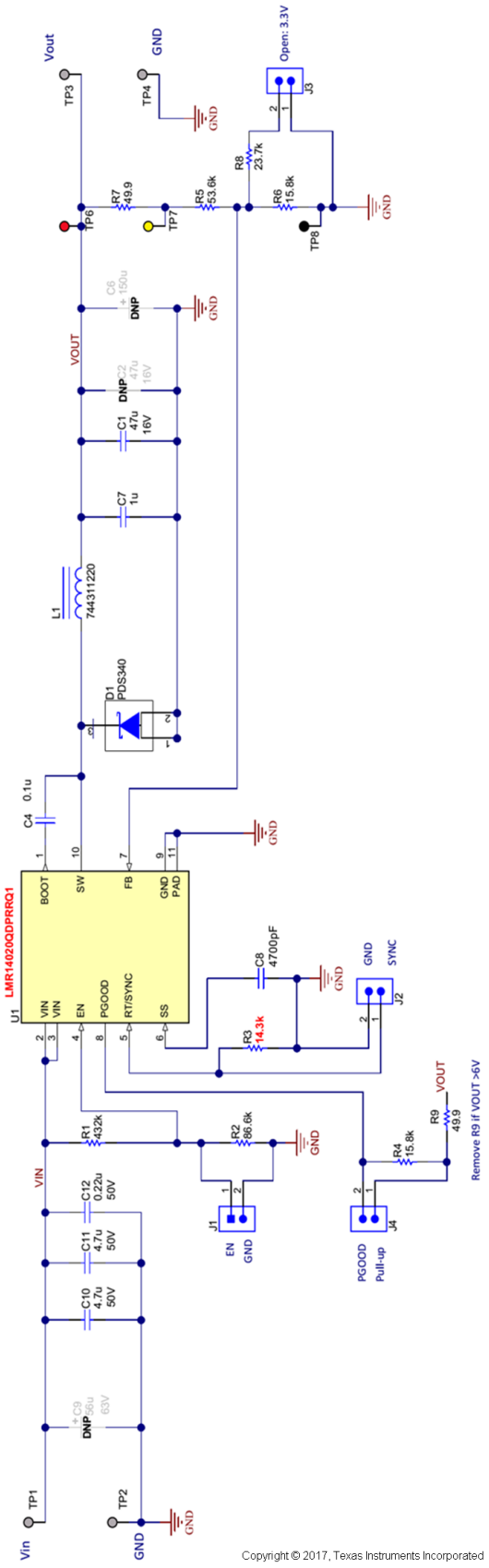

Figure 9. EVM Schematic

Figure 11 shows the calculated Bode plot with practical parameter correction.

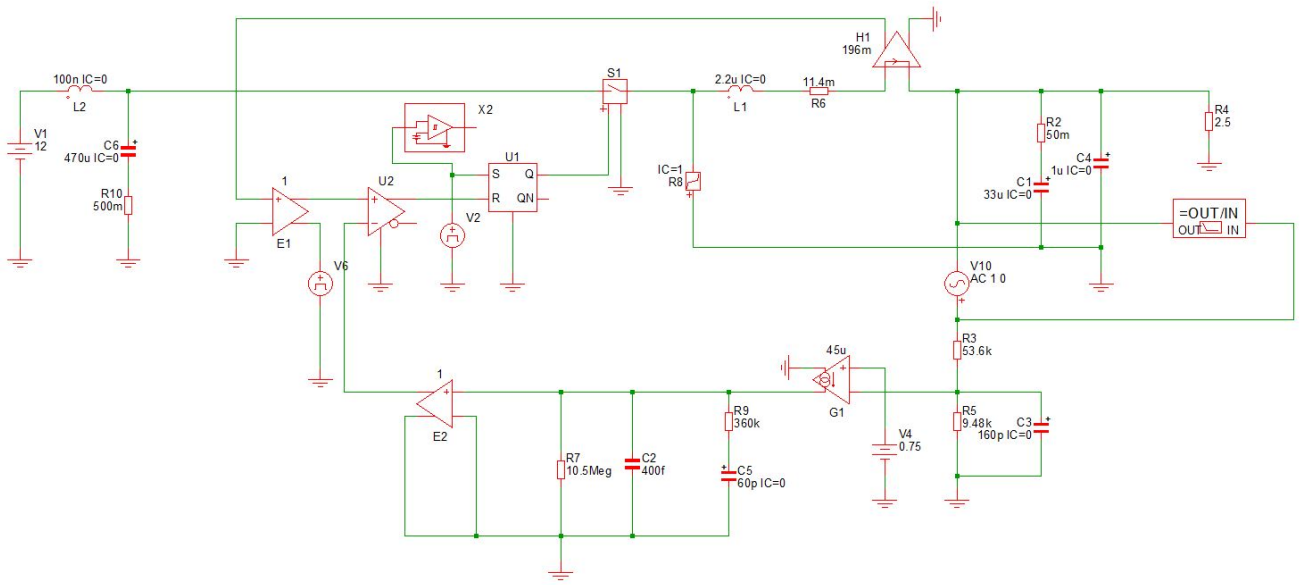

Figure 10. Simplis Model Schematic

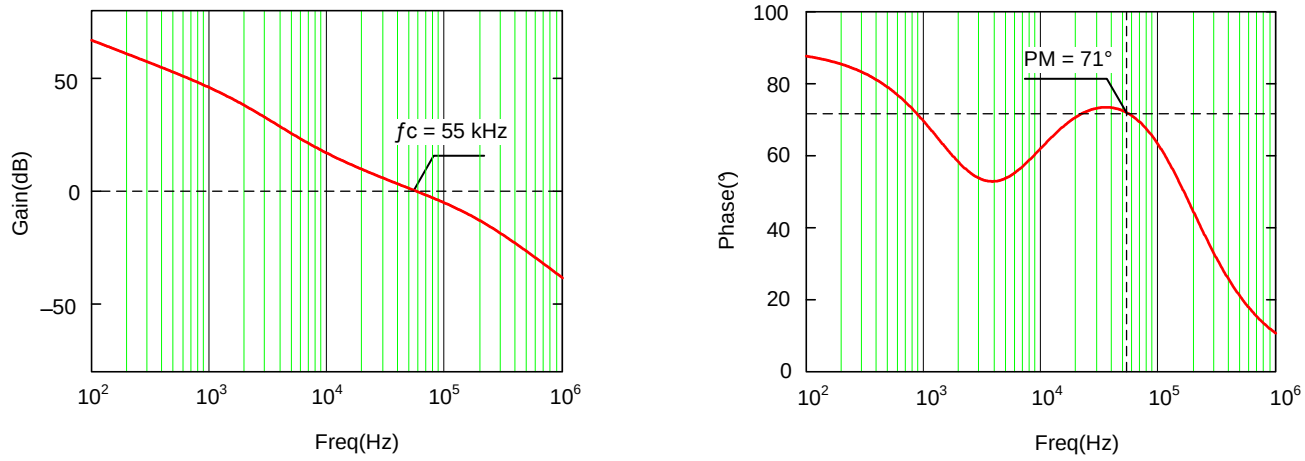

Figure 11. Calculated Bode Plot of Accurate Model

Figure 12 and Figure 13 are the simulation and bench results. Calculated results, Simplis model, and bench measurement match with each other well.

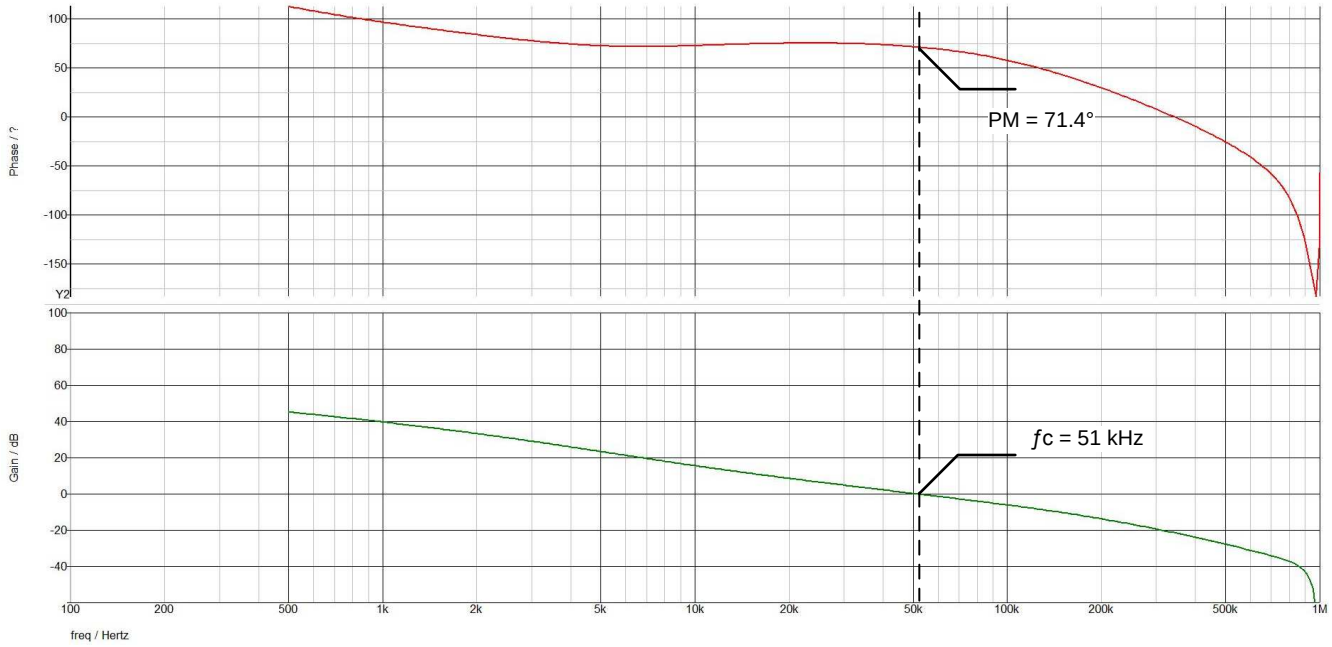

Figure 12. Bode Plot of Accurate Simplis Model

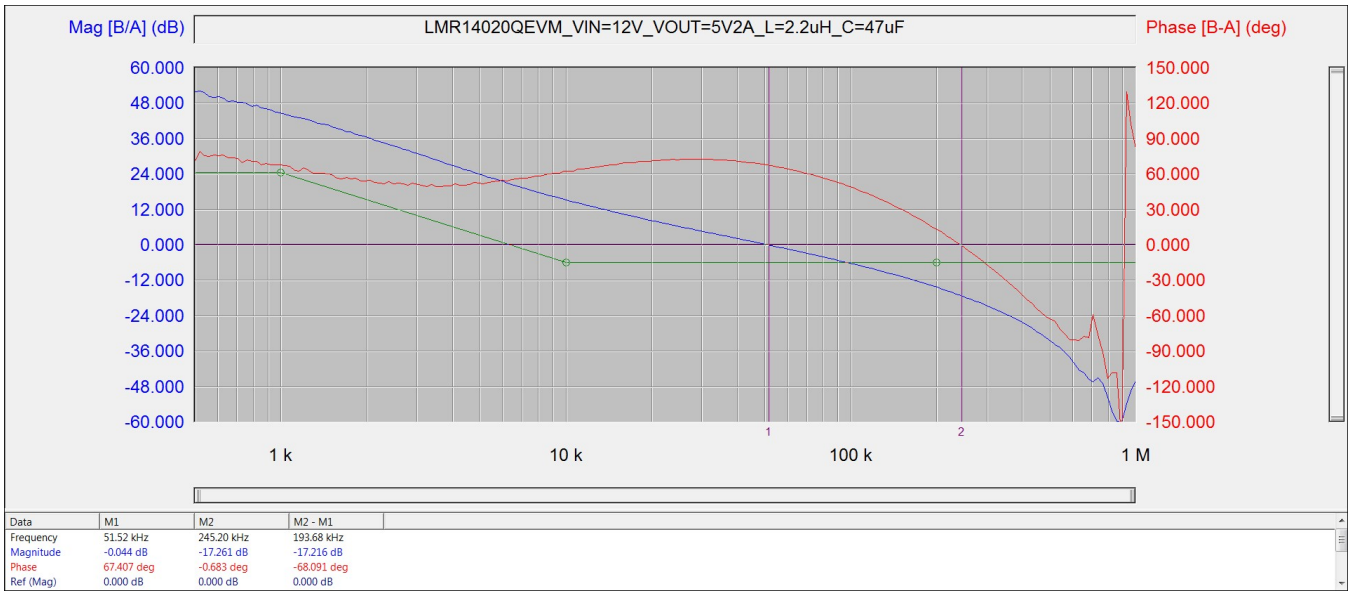

Figure 13. EVM Bode Plot

Figure 14–Figure 21 are the transient and frequency performance with different inductance. The test condition is: V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT}: 0–2 A, 1 A/µs slew rate. Observe that large inductance does not have enough phase margin as well as loop transient performance. In this condition, 10-µH inductance is the maximum value to get 45° phase margin to make the system stable.

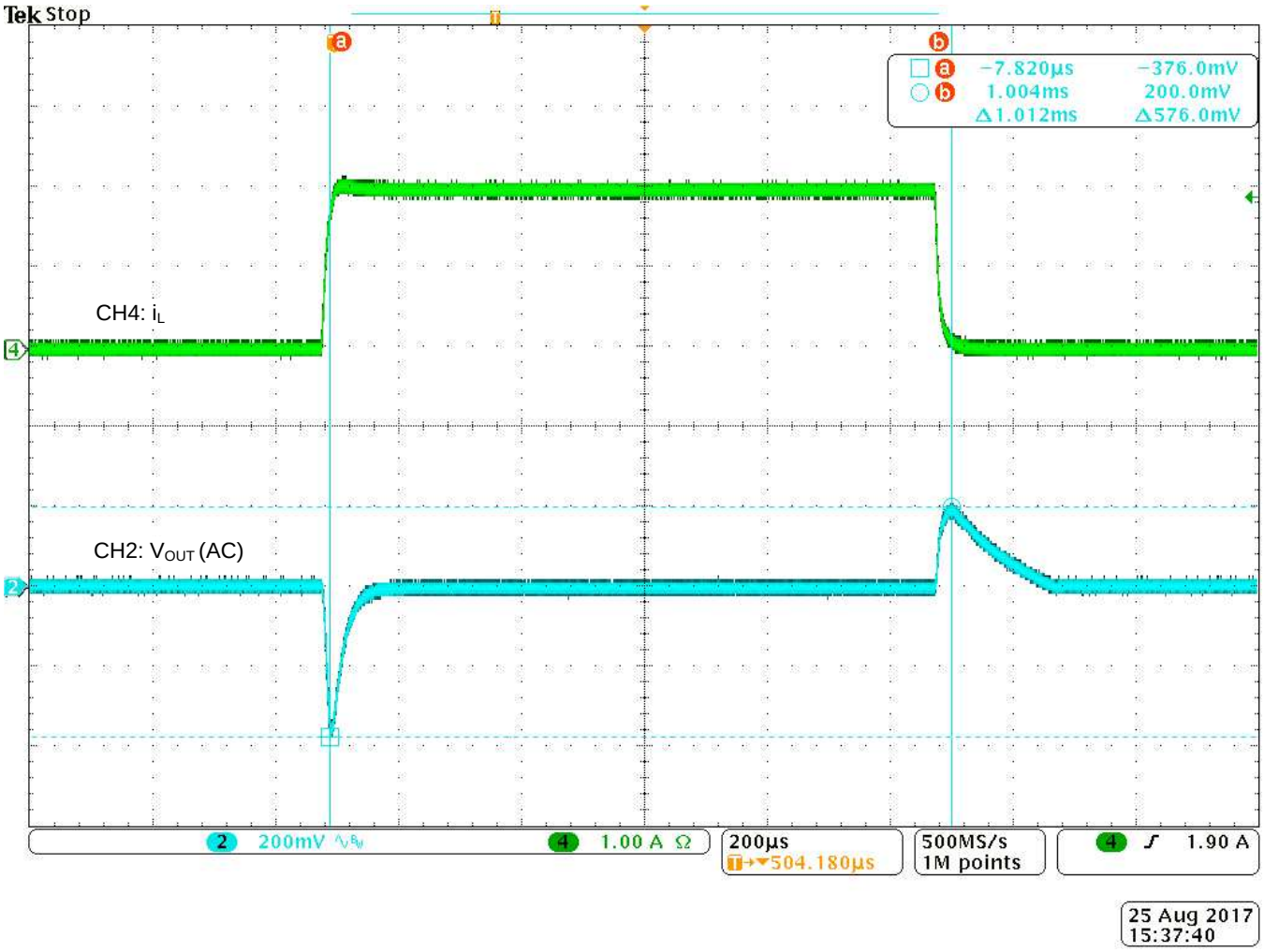

Figure 14. Transient Performance, L_f = 2.2 µH, V_{pp} = 576 mV

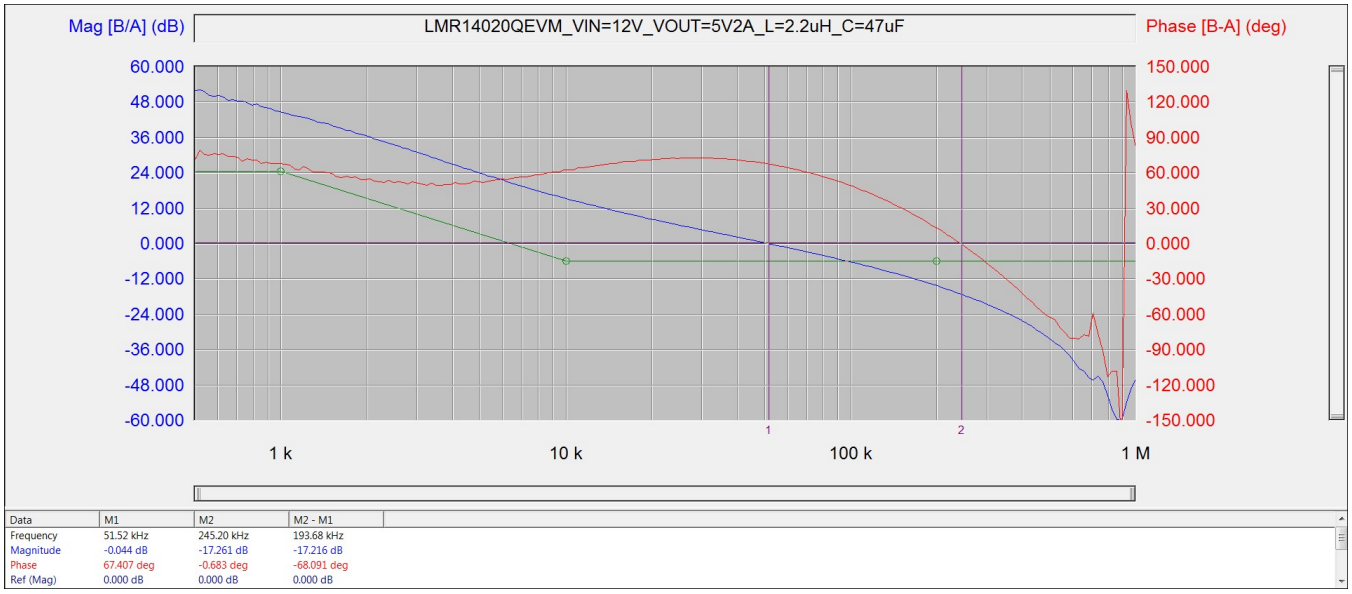

Figure 15. Loop Response, L_f = 2.2 µH, f_c = 51.5 kHz, PM = 67.4°

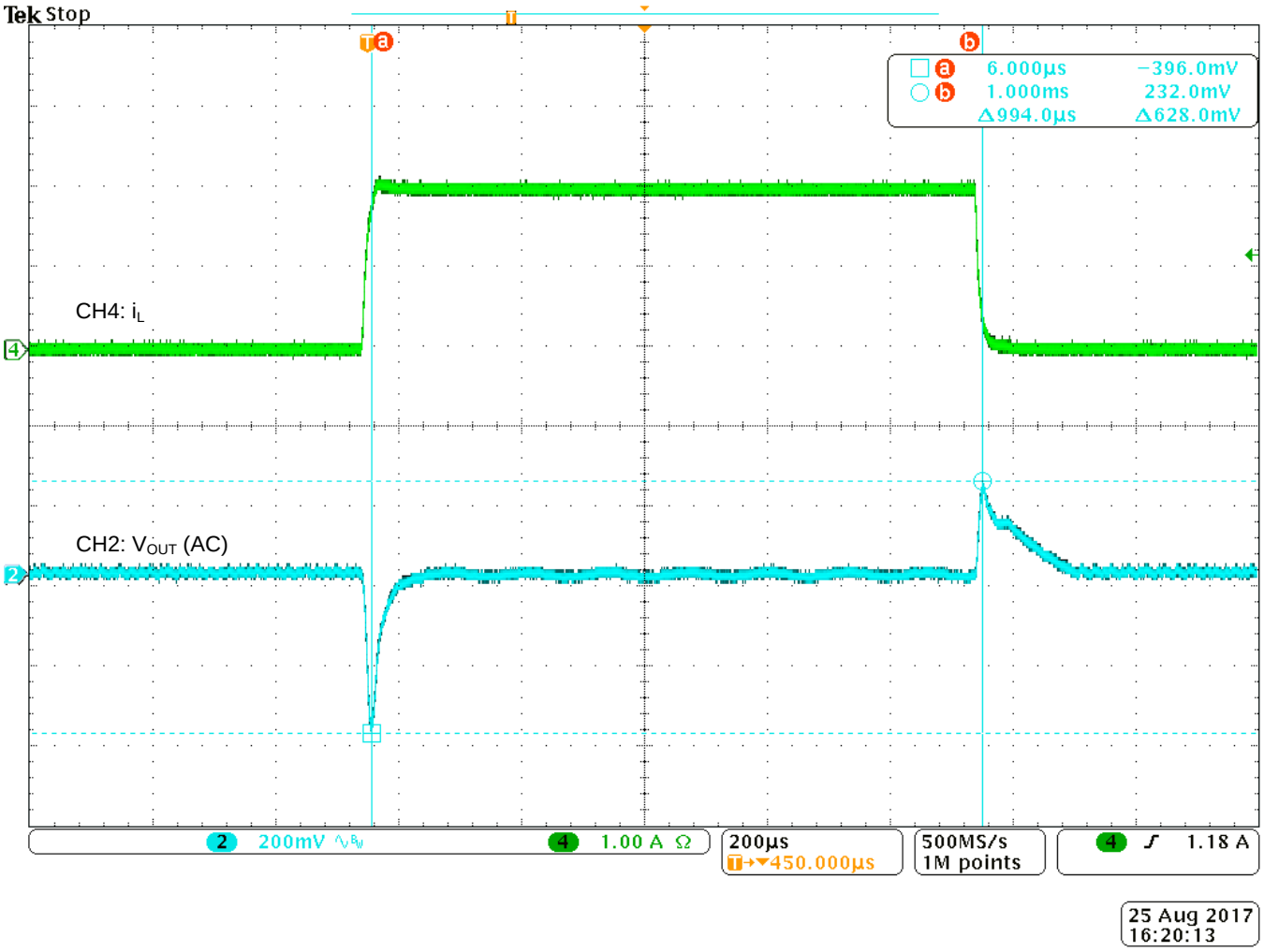

Figure 16. Transient Performance, L_f = 10 µH, V_{pp} = 628 mV

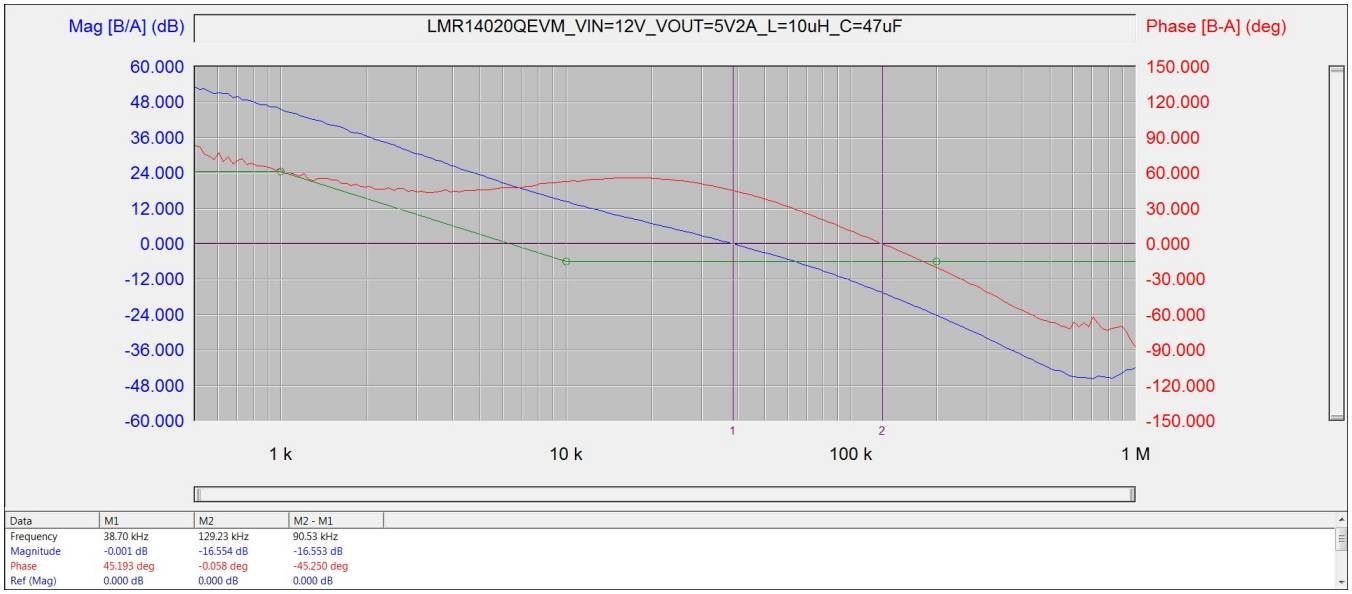

Figure 17. Loop Response, L_f = 10 µH, f_c = 38.7 kHz, PM = 45.2°

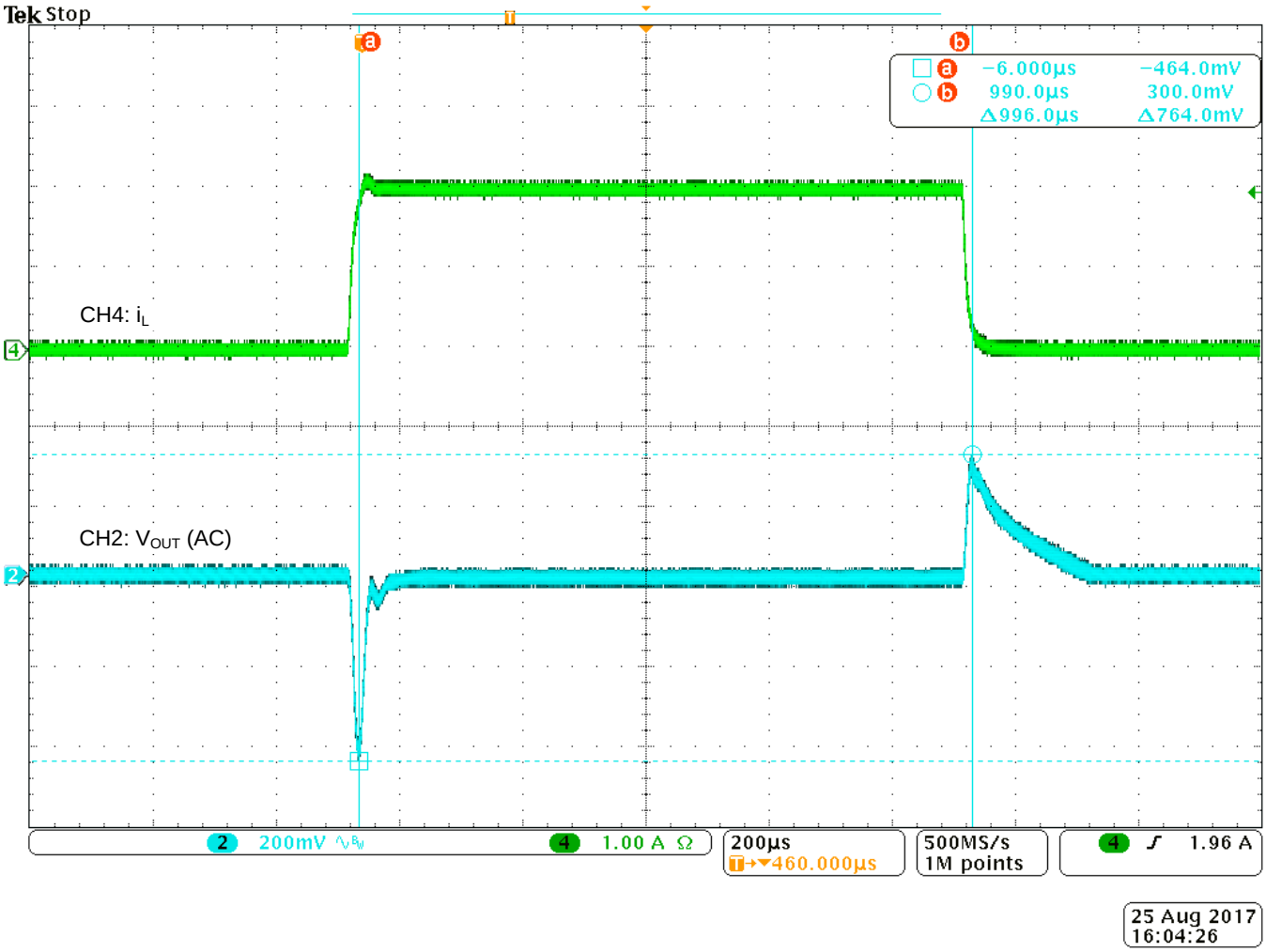

Figure 18. Transient Performance, L_f = 22 µH, V_{pp} = 764 mV

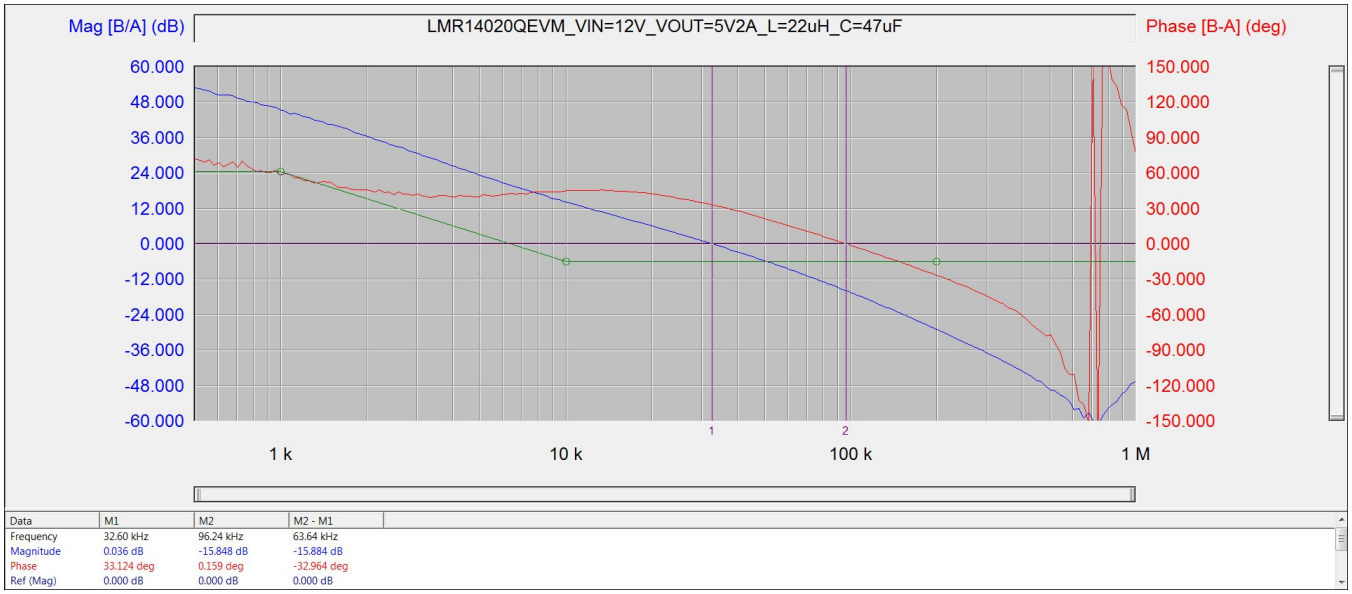

Figure 19. Loop Response, L_f = 22 µH, f_c = 32.6 kHz, PM = 33.1°

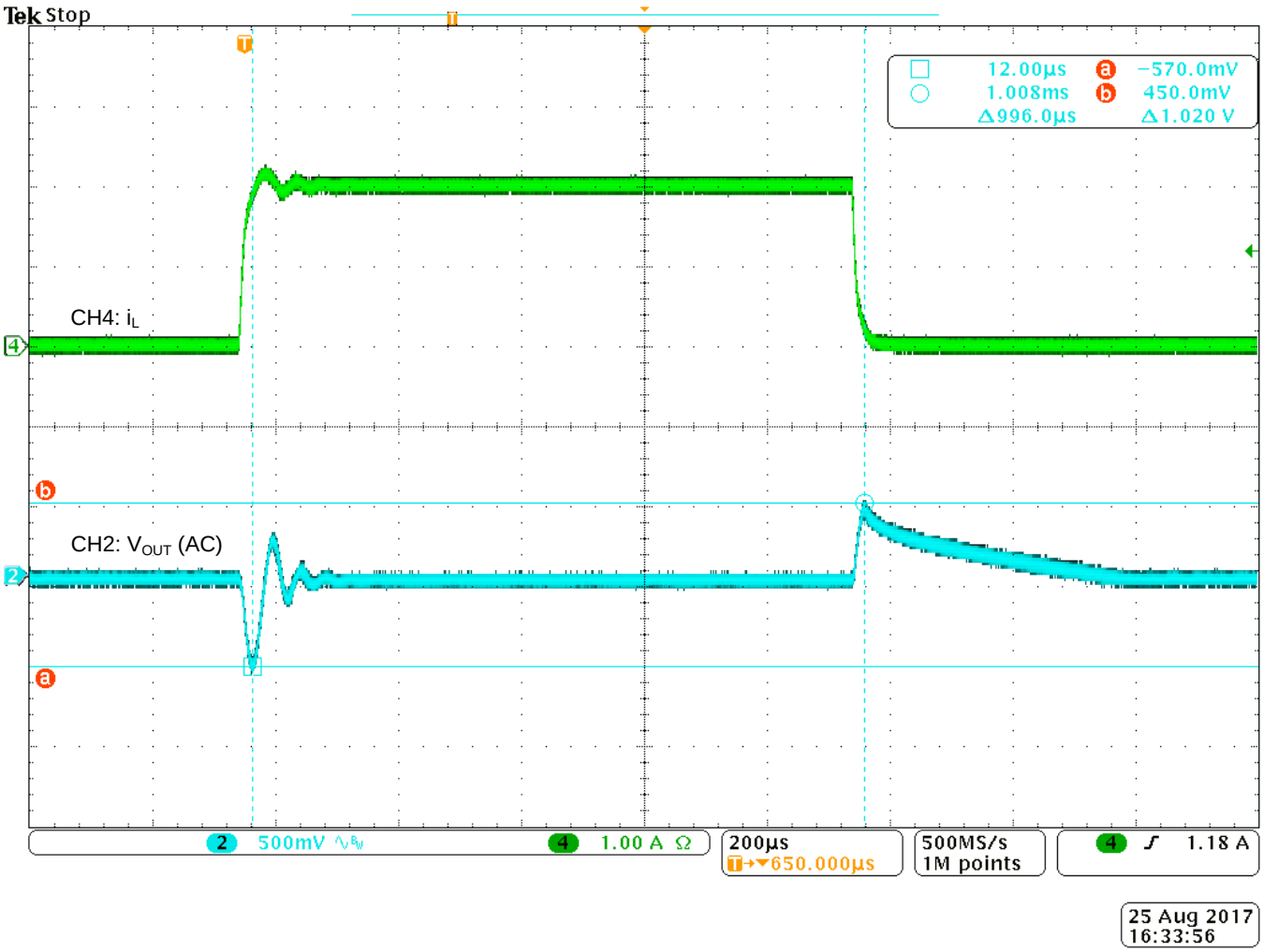

Figure 20. Transient Performance, L_f = 47 µH, V_{pp} = 1020 mV

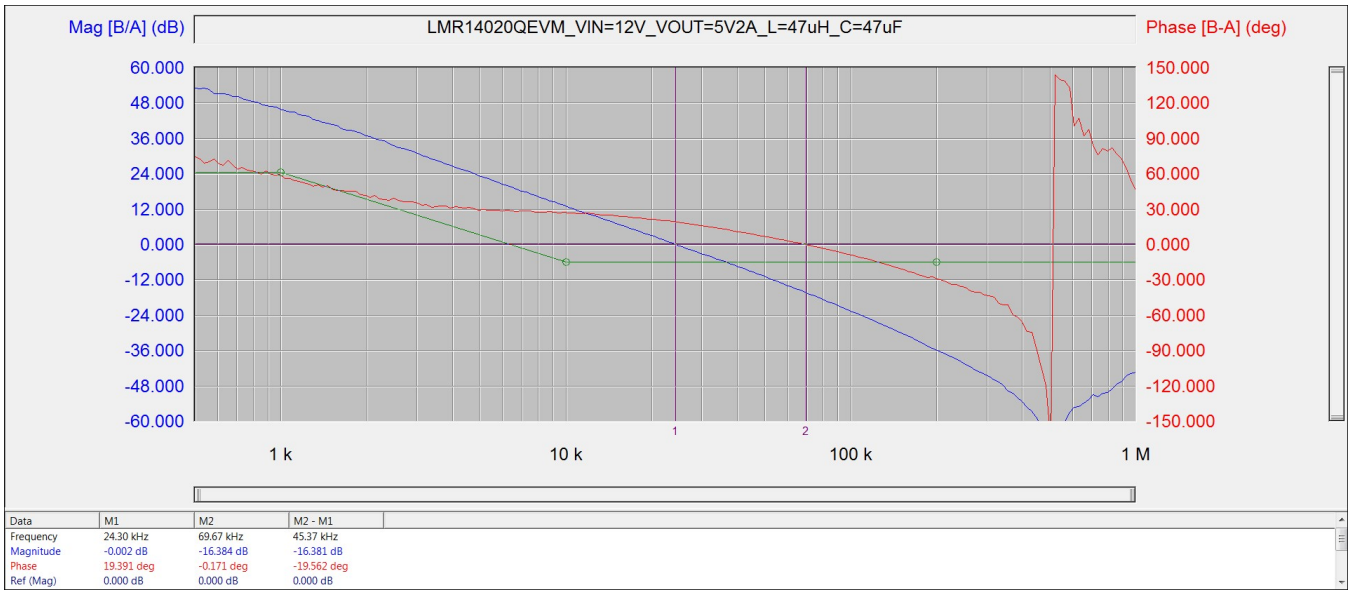

Figure 21. Loop Response, L_f = 47 µH, f_c = 24.3 kHz, PM = 19.4°

5 Conclusion

In an internal compensation PCM buck converter, crossover frequency is fixed with an output capacitor, in a simplified PCM model. In actuality, the inductor also brings in a pole and may reduce the system phase margin too much. The inductor pole must be larger than f_c derived in the simplified model. Mathcad calculated results, Simplis simulation, and bench test verify the theory.

6 References

1. Texas Instruments, *LMR14020-Q1 SIMPLE SWITCHER® 40 V, 2 A Step-Down Converter with 40 μA I_Q*
2. Texas Instruments, *LMR14020QDPR-EVM User's Guide*
3. Texas Instruments, *How to Configure LMZ30604 Power Module with Ceramic Capacitors*
4. Texas Instruments, *TPS65270 Loop Compensation Design Consideration*
5. Texas Instruments, *Current-Mode Modeling for Peak, Valley and Emulated Control Methods*

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265