Application Report

Benefits Using a Buck Converter's External Vcc Bias Pin

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ABSTRACT

Several step-down converters operating above a 5-V input have an internal linear low-drop-out (LDO) power supply providing power to the converter's internal logic control and MOSFET gate-drive circuitry. Unfortunately, the voltage drop of the internal LDO circuit increases the total power loss and slightly reduces the converter's efficiency. Some step-down converters on the market provide a separate pin that accepts an external bias voltage to override the internal LDO circuit and eliminate the power loss. Applying an external bias voltage allows designers to improve system efficiency and reduce power dissipation. This report compares the power losses of 16-V, 15-A TPS548A28 and TPS548A29 synchronous step-down converters when using internal and external bias voltages in a multi-rail point-of-load system. Both devices have the same integrated power stage but have a different internal LDO voltage.

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Trademarks

1 DC/DC Converters with Internal LDO

The input voltage of a DC/DC step-down converter is internally routed to analog circuitry, gate-drive circuitry, and the drain of the high-side MOSFET for power conversion. Since it is impractical and unnecessary to use a higher voltage semiconductor process for analog and gate-drive circuits, a separate internal LDO regulator is integrated into the DC/DC converter to provide power to these circuits. Figure 1-1 illustrates a typical DC/DC converter accepting a 4-V to 16-V input onto the VIN pins and Figure 1-2 shows an internal LDO providing power to the analog and gate-drive circuitry. The internal LDO powers all the analog circuitry and logic inside the IC, and its voltage may optimized for different voltage levels needed by the circuitry. The internal LDO steps-down the VIN voltage to the VCC voltage and the voltage-drop across the LDO causes power to be dissipated in the LDO. Since the load of the internal LDO is I_{VCC}, the power dissipated by the internal LDO is (VIN – VLDO)*I_{VCC}. A larger bias current and higher voltage-drop causes the DC/DC converter's efficiency to decrease.

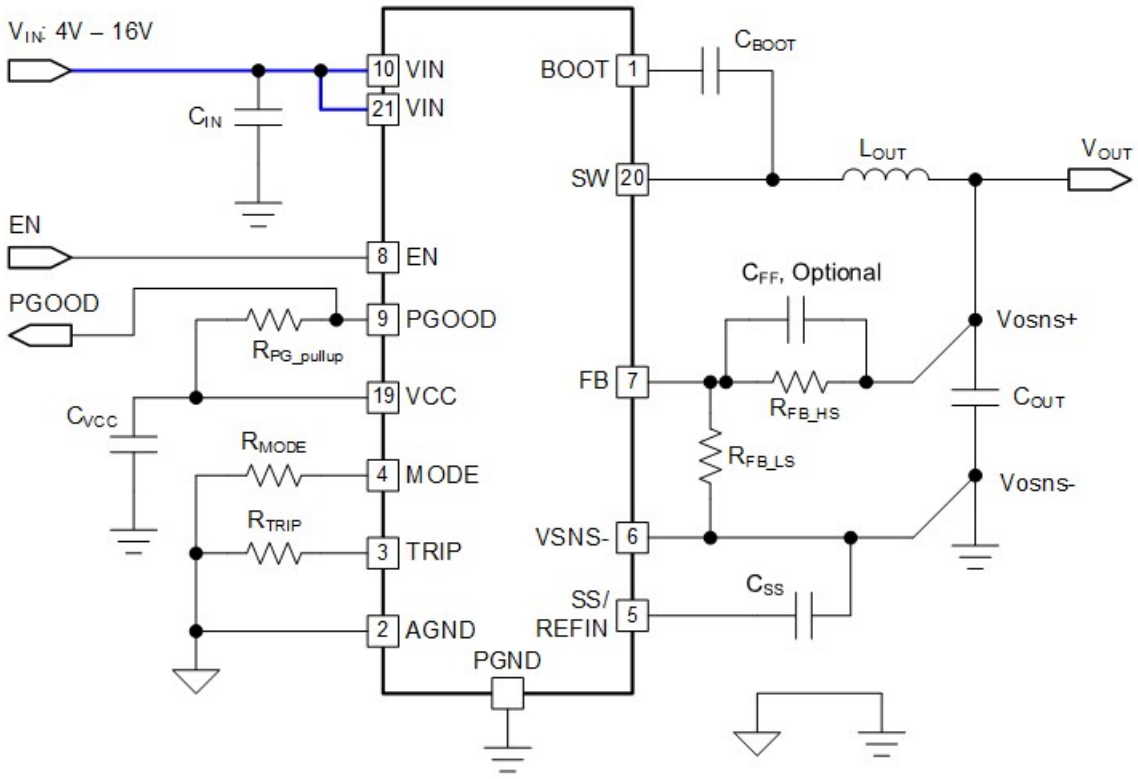

Figure 1-1. Typical DC/DC Converter with Single Input Voltage

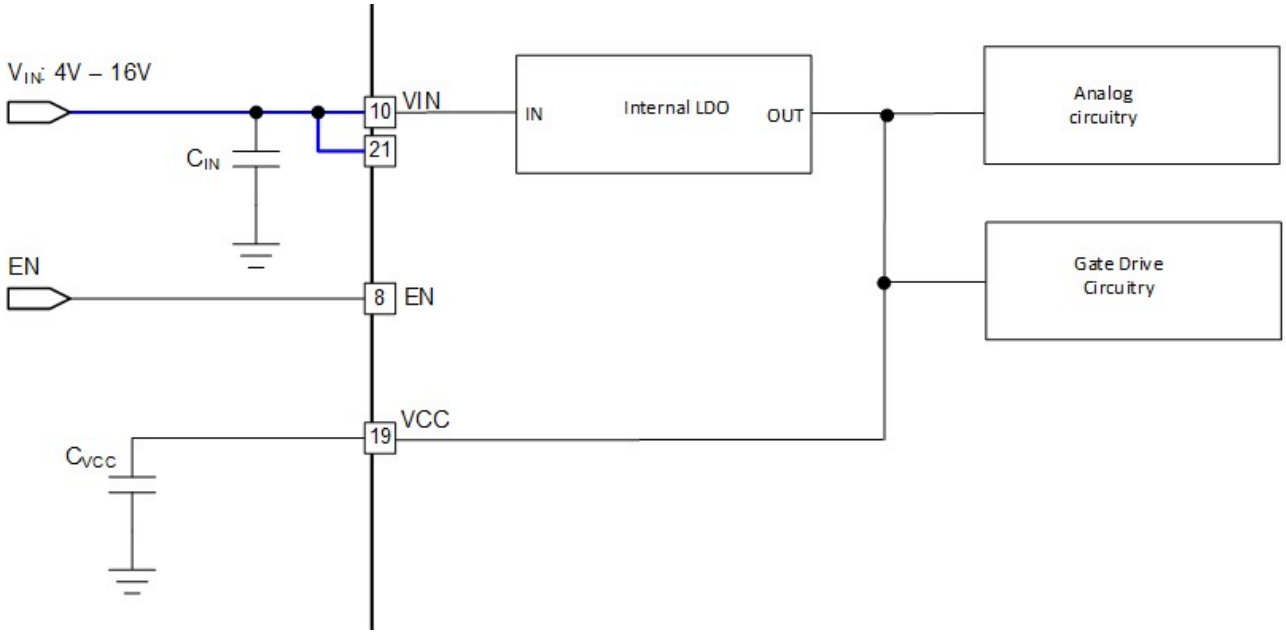

Figure 1-2. DC/DC Converter with Integrated Internal LDO

2 DC/DC Converters with External Bias

Several DC/DC converters on the market have an additional pin that accepts an externally applied voltage, such as the TPS548A28 and TPS548A29 shown in Table 2-1. An external bias voltage, also called a split-bias rail voltage, above the internal LDO's output voltage will override the internal LDO and enhance the efficiency of the converter by eliminating its power loss. The VCC current will be supplied from the external bias instead of the internal LDO. Figure 2-1 shows an external bias voltage applied to the VCC pin allowing a lower input voltage into the VIN pins. The VCC pin needs to be bypassed with a 2.2 µF ceramic capacitor, C_{VCC} with a 6.3-V or higher rating as shown in Figure 1-1 and Figure 2-1. The external VCC voltage is supplied by a separate DC/DC converter or connected directly from an existing 3.3-V or 5-V voltage source already available on the circuit board.

Table 2-1. Featured DC/DC Converters with Internal LDO and Split-Bias Rail

Device	Output Current	Internal LDO Voltage	External Bias Voltage Range	Power Stage Voltage Range with External Bias Voltage	Power Stage Voltage Range with Internal LDO Voltage
TPS548A28	15-A	3-V	3.13-V to 5.3-V	2.7-V to 16-V	4-V to 16-V
TPS548A29	15-A	4.5-V	4.75-V to 5.3-V	2.7-V to 16V	4-V to 16-V

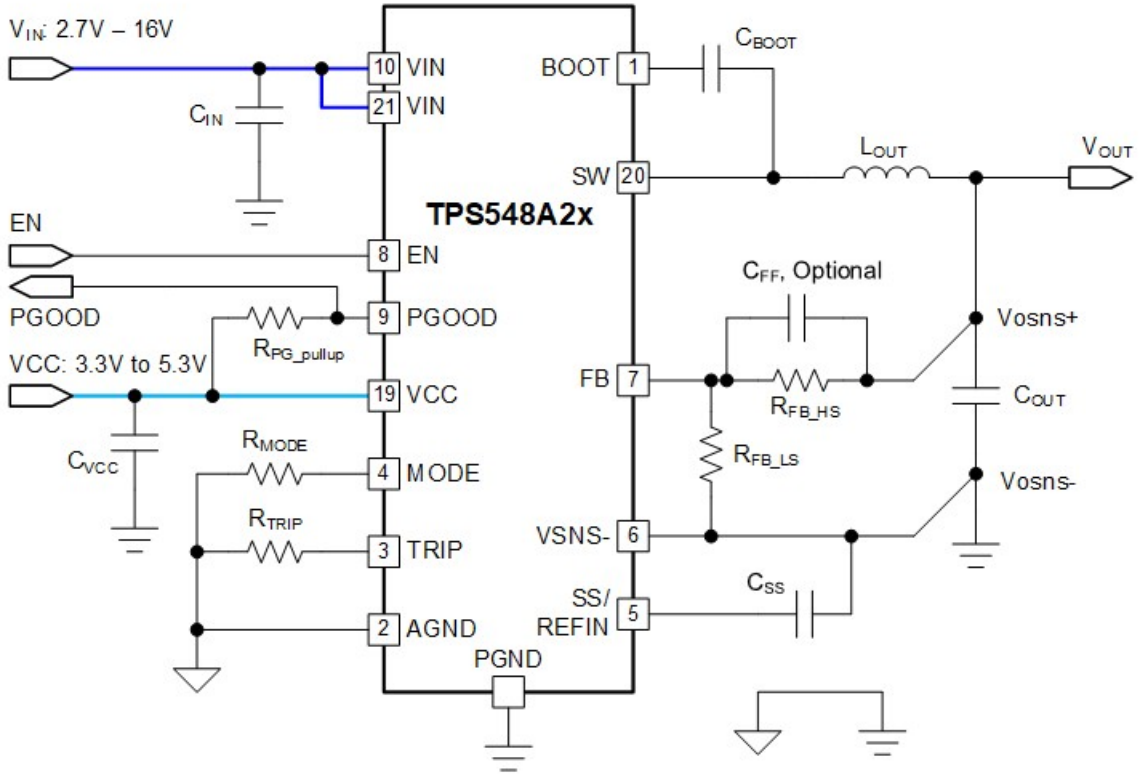

Figure 2-1. Typical DC/DC Converter with Split-Bias Rail Input Voltages

3 Efficiency and Power Loss Calculations

The power efficiency formula is shown in Equation 1 and the power loss formula is shown in Equation 2. Power loss results in Watts are easier to compare than efficiency numbers, especially in multi-rail systems because a watt is more specific than an efficiency percentage when considering power dissipation.

$$\text{Efficiency} = V_{OUT} \times I_{OUT} / V_{IN} \times I_{VIN} \quad (1)$$

$$\text{Power Loss} = V_{IN} \times I_{VIN} - V_{OUT} \times I_{OUT} \quad (2)$$

Equation 3 and Equation 4 show the power losses of the internal LDO and demonstrate that additional losses are present depending on the efficiency of the internal LDO, using 25% efficiency as an example.

$$\text{Efficiency}=(V_{OUT} \times I_{OUT})/(V_{IN} \times I_{VIN}+(VCC \times I_{VCC})/(0.25)) \quad (3)$$

$$\text{Power Loss}=V_{IN} \times I_{VIN}+(VCC \times I_{VCC})/0.25-V_{OUT} \times I_{OUT} \quad (4)$$

When the VCC pin is connected to an external source that is greater than the internal LDO output voltage, the internal LDO is turned off, power is drawn from the external source, and the internal LDO power loss $(VIN-V_{LDO})*I_{VCC}$ is zero resulting in increased efficiency of the converter. However, if the I_{BIAS} current is provided by an additional DC/DC converter, its own power losses need to be considered into the total system efficiency. If the additional DC/DC converter is a synchronous buck converter, the power losses will be lower than the internal LDO power losses. The internal LDO also provides the voltage for boot capacitor C_{BOOT} to provide the gate-drive voltage to drive the power MOSFETs. When the external VCC is higher than the internal LDO voltage, the gate-drive voltage increases, lowering the $R_{DS(on)}$ of the MOSFETs and increasing the efficiency, especially at higher output current.

4 Power Loss of Multi-Rail Point-of-Load System

Many applications use multiple DC/DC converters in a point-of-load architecture. Figure 4-1 shows 7 rails using the TPS548A28 accepting external 3.3-V or 5-V V_{BIAS} voltages from either a seperate step-down converter or a separate power supply rail already on the circuit board. The TPS548A29 with a 4.5-V internal LDO may also be used in its place to compare the TPS548A28 power loss across different output current levels.

Using the TPS548A28 with an external 5-V bias voltage, compared to the TPS548A29 4.5-V internal LDO saves 1.03-W at 12-A. Efficiency gains are realized from the reduced power losses of the overridden internal LDOs . The power loss of each internal LDO is approximately the bias current I_{VCC} (20-mA) multiplied by the voltage-drop (7-V) from the 7 DC/DC converters in the multi-rail system, and the calculated value of approximately 0.98-W correlates with the measurement at 12-A. Alternatively, the TPS548A28 with an external 3.3-V bias voltage compared to the TPS548A29 4.5-V internal LDO saves only 100-mW of power. In this example, the higher gate-drive voltage of the TPS548A29 improves the MOSFET $R_{DS(on)}$ conduction losses of Equation 5, compared to the TPS548A28 and external 3.3-V bias, but the internal LDO losses realized are still higher than the conduction loss savings. Table 4-1 summarizes the power loss measurements at various loads and configurations under the specified conditions. Table 4-2 shows the difference in MOSFET resistance depending on the applied gate-drive voltage. Both devices have the same integrated power stage. A higher gate-drive voltage provides lower $R_{DS(ON)}$ for higher efficiency and lower power losses.

$$\text{Conduction loss} = I_{OUT} \times R_{DS(ON)}{}^{2} \tag{5}$$

Table 4-3 compares the TPS548A28 with an internal 3-V bias volatge and an externally applied 5-V bias. At 10-A, there is a significant 1.56 W power loss savings between the TPS548A28 with a 3-V internal LDO to an externally applied 5-V bias voltage. MOSFET conduction loss savings are more prominent than the internal LDO power loss savings considering all 7 DC/DC converters together. At lower currents, the power loss improvements are less significant because conduction losses are less significant. At 1-A load, the savings from the external 5-V bias configuration saves only 30mW and at 5-A is 530mW. MOSFET gate-drive voltage and output current need to be considered when realizing power loss savings.

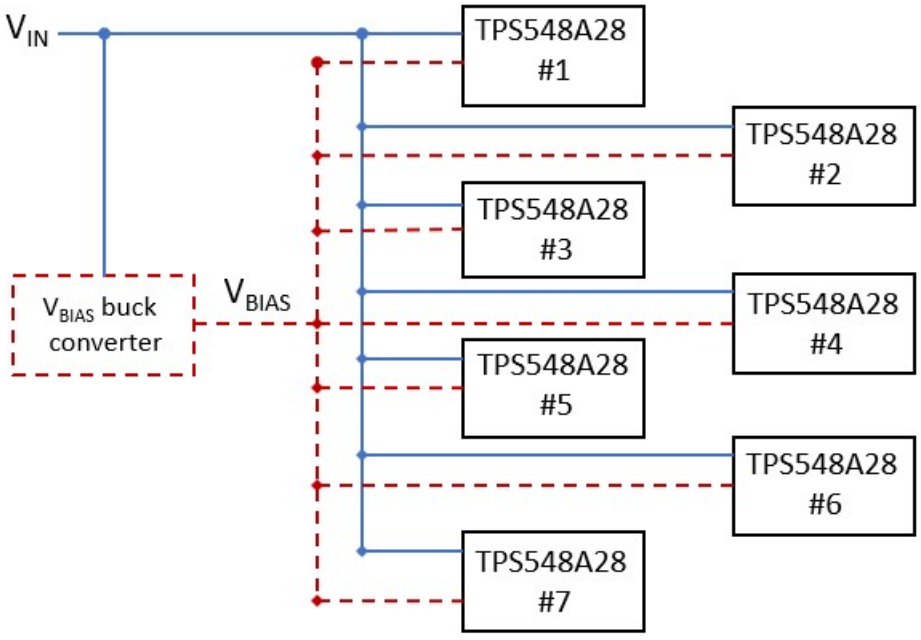

Figure 4-1. Multiple Rail System Using the TPS548A28 with External V_{BIAS} Voltage

Table 4-1. Measured Power Losses of 7-Rail System in Watts

12-V input, 1-V output, f_{sw} = 600 kHz, L=1 uH / 2.55 mΩ

Device	Bias Voltage	1-A	5-A	10-A
TPS548A28	Internal 3-V	1.98	4.13	11.2
TPS548A28	External 5-V	1.95	3.6	9.64

Table 4-2. MOSFET Resistance with Different Gate Drive Voltages

Device	Parameter	Description	Conditions	Typ.	Units
TPS548A28	$R_{DS(ON)HS}$	High-side MOSFET on-resistance	BOOT–SW = 3 V	10.2	mΩ
	$R_{DS(ON)LS}$	Low-side MOSFET on-resistance	VCC = 3 V	3.1	mΩ
TPS548A29	$R_{DS(ON)HS}$	Low-side MOSFET on-resistance	BOOT–SW = 4.5 V	8.4	mΩ
	$R_{DS(ON)LS}$	Low-side MOSFET on-resistance	VCC = 4.5 V	2.6	mΩ

Table 4-3. Measured Power Losses of 7-rail System in Watts

12-V input, 1-V output, f_{sw} = 600 kHz, L=1 uH / 2.55 mΩ

Device	Bias Voltage	1-A	5-A	10-A
TPS548A28	Internal 3-V	1.98	4.13	11.2
TPS548A28	External 5-V	1.95	3.6	9.64

5 Summary

DC/DC converters with split-bias rail capability considerably reduce power losses when an external 5-V supply is readily available on the circuit board. Efficiency is increased by eliminating internal LDO losses and reducing $R_{DS(on)}$ conduction losses with a higher gate-drive voltage, especially at higher output current levels. The improvements are multiplied by the number of DC/DC converters on the circuit board.

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