



Ridge Lahti

ABSTRACT

The LM5168 is a synchronous buck converter with a wide input voltage range from 6 V to 115 V and maximum output current of 300 mA. The LM5168 can be configured as an inverting buck-boost (IBB) converter with a negative output voltage. This application note demonstrates how the LM5168 can be used as an inverting buck-boost converter, along with optional design considerations for inverting buck-boost converters such as a PGOOD or EN level-shifter. If higher output current is required, the LM5168 is pin-to-pin compatible with the 600-mA rated LM5169. Automotive grade versions, the LM5168-Q1 and LM5169-Q1, are also available.

Table of Contents

1 Inverting Buck-Boost Topology	3
1.1 Concept.....	3
1.2 Output Current Calculations.....	3
1.3 Voltage Range of Inverting Buck-Boost Configuration.....	4
2 Design Considerations	5
2.1 Bypass Capacitor and Optional Schottky Diode.....	5
3 External Components	6
3.1 Capacitor Selection.....	6
3.2 Inductor Selection.....	6
4 Digital Pin Configurations	7
4.1 Optional Enable (EN) Level Shifter.....	7
4.2 Power-Good (PG) Pin.....	8
5 Typical Performance	9
5.1 $V_{OUT} = -12\text{ V}$ Typical Performance	9
5.2 $V_{OUT} = -24\text{ V}$ Typical Performance	12
5.3 $V_{OUT} = -48\text{ V}$ Typical Performance	15
6 Conclusion	18
7 References	19

List of Figures

Figure 1-1. Converting From Buck to Inverting Buck-Boost Topology.....	3
Figure 1-2. Maximum Output Current Calculations for the LM5168 with Assumed 85% Efficiency.....	4
Figure 2-1. LM5168 Inverting Buck-Boost with Optional Schottky Diode.....	5
Figure 4-1. EN Pin Level Shifter.....	7
Figure 4-2. PG Pin Level Shifter.....	8
Figure 5-1. Schematic.....	9
Figure 5-2. Bill of Materials.....	9
Figure 5-3. Efficiency vs. Load Current.....	9
Figure 5-4. Load Regulation vs. Load Current.....	9
Figure 5-5. Startup at $V_{IN} = 12\text{ V}$	9
Figure 5-6. Shutdown at $V_{IN} = 12\text{ V}$	9
Figure 5-7. Startup at $V_{IN} = 24\text{ V}$	10
Figure 5-8. Shutdown at $V_{IN} = 24\text{ V}$	10
Figure 5-9. Full Load Transient at $V_{IN} = 12\text{ V}$	10
Figure 5-10. Load Transient at $V_{IN} = 12\text{ V}$	10
Figure 5-11. Full Load Transient at $V_{IN} = 24\text{ V}$	10
Figure 5-12. Load Transient at $V_{IN} = 24\text{ V}$	10
Figure 5-13. No Load Output Ripple at $V_{IN} = 12\text{ V}$	11
Figure 5-14. Full Load Output Ripple at $V_{IN} = 12\text{ V}$	11

Figure 5-15. No Load Output Ripple at $V_{IN} = 24\text{ V}$	11
Figure 5-16. Full Load Output Ripple at $V_{IN} = 24\text{ V}$	11
Figure 5-17. Schematic.....	12
Figure 5-18. Bill of Materials.....	12
Figure 5-19. Efficiency vs. Load Current.....	12
Figure 5-20. Load Regulation vs. Load Current.....	12
Figure 5-21. Startup at $V_{IN} = 24\text{ V}$	12
Figure 5-22. Shutdown at $V_{IN} = 24\text{ V}$	12
Figure 5-23. Startup at $V_{IN} = 48\text{ V}$	13
Figure 5-24. Shutdown at $V_{IN} = 48\text{ V}$	13
Figure 5-25. Full Load Transient at $V_{IN} = 24\text{ V}$	13
Figure 5-26. Load Transient at $V_{IN} = 24\text{ V}$	13
Figure 5-27. Full Load Transient at $V_{IN} = 48\text{ V}$	13
Figure 5-28. Load Transient at $V_{IN} = 48\text{ V}$	13
Figure 5-29. No Load Output Ripple at $V_{IN} = 24\text{ V}$	14
Figure 5-30. Full Load Output Ripple at $V_{IN} = 24\text{ V}$	14
Figure 5-31. No Load Output Ripple at $V_{IN} = 48\text{ V}$	14
Figure 5-32. Full Load Output Ripple at $V_{IN} = 48\text{ V}$	14
Figure 5-33. Schematic.....	15
Figure 5-34. Bill of Materials.....	15
Figure 5-35. Efficiency vs. Load Current.....	15
Figure 5-36. Load Regulation vs. Load Current.....	15
Figure 5-37. Startup at $V_{IN} = 48\text{ V}$	15
Figure 5-38. Shutdown at $V_{IN} = 48\text{ V}$	15
Figure 5-39. Startup at $V_{IN} = 60\text{ V}$	16
Figure 5-40. Shutdown at $V_{IN} = 60\text{ V}$	16
Figure 5-41. Full Load Transient at $V_{IN} = 48\text{ V}$	16
Figure 5-42. Load Transient at $V_{IN} = 48\text{ V}$	16
Figure 5-43. Full Load Transient at $V_{IN} = 60\text{ V}$	16
Figure 5-44. Load Transient at $V_{IN} = 60\text{ V}$	16
Figure 5-45. No Load Output Ripple at $V_{IN} = 48\text{ V}$	17
Figure 5-46. Full Load Output Ripple at $V_{IN} = 48\text{ V}$	17
Figure 5-47. No Load Output Ripple at $V_{IN} = 60\text{ V}$	17
Figure 5-48. Full Load Output Ripple at $V_{IN} = 60\text{ V}$	17

Trademarks

All trademarks are the property of their respective owners.

1 Inverting Buck-Boost Topology

1.1 Concept

For the standard buck converter, the inductor is connected to V_{OUT} and the switch pin (SW) of the LM5168. In order to change to an inverting buck-boost topology, the V_{OUT} and ground nodes of the circuit must be reversed. With the nodes reversed, the LM5168 can now invert the output voltage from the input voltage.

To change an LM5168 buck converter to an inverting buck-boost, reassign the buck converter V_{OUT} to system ground, and the old buck system ground to $-V_{OUT}$. The input capacitor will need to be reconnected to the new system ground, and a new bypass capacitor, C_{IO} , is needed between V_{IN} and $-V_{OUT}$. The positive input and the feedback resistors will remain the same as in the buck converter. To adjust the output of the inverting buck-boost, calculate the feedback resistor values as if it was a buck converter. For further reading on the inverting buck-boost topology, refer to the [Working with Inverting Buck-Boost Converters](#) application note. The schematics in Figure 1-1 show the changes that have to be made when configuring the LM5168 buck converter as an inverting buck-boost converter.

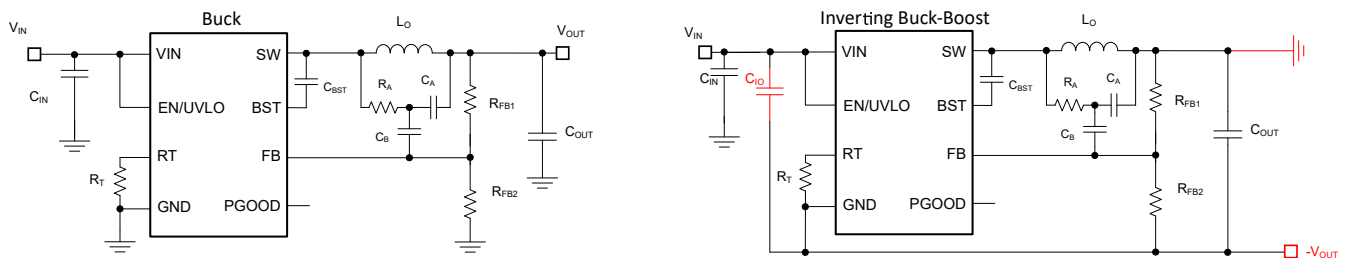


Figure 1-1. Converting From Buck to Inverting Buck-Boost Topology

1.2 Output Current Calculations

Changing to an inverting buck-boost topology will have an impact on the maximum possible output current. For an inverting buck-boost converter, the inductor current will always be larger than the output current. As a result, the maximum possible output current is calculated by:

$$I_{OUT}(IBB) = I_{OUT_Buck} \times (1 - D) \quad (1)$$

where:

- I_{OUT_Buck} is the maximum buck converter DC output current
- D is the duty cycle

The duty cycle can be calculated as:

$$D = \frac{V_{out}}{V_{out} - V_{in} \times \eta} \quad (2)$$

V_{OUT} is represented as the negative output voltage of the inverting buck-boost converter. The efficiency term in the duty cycle equation helps account for power losses to provide a more accurate calculation of the output current. For example, if the output voltage is -24 V, the input voltage is 12 V, and the efficiency is assumed to be 85%, then the duty cycle is:

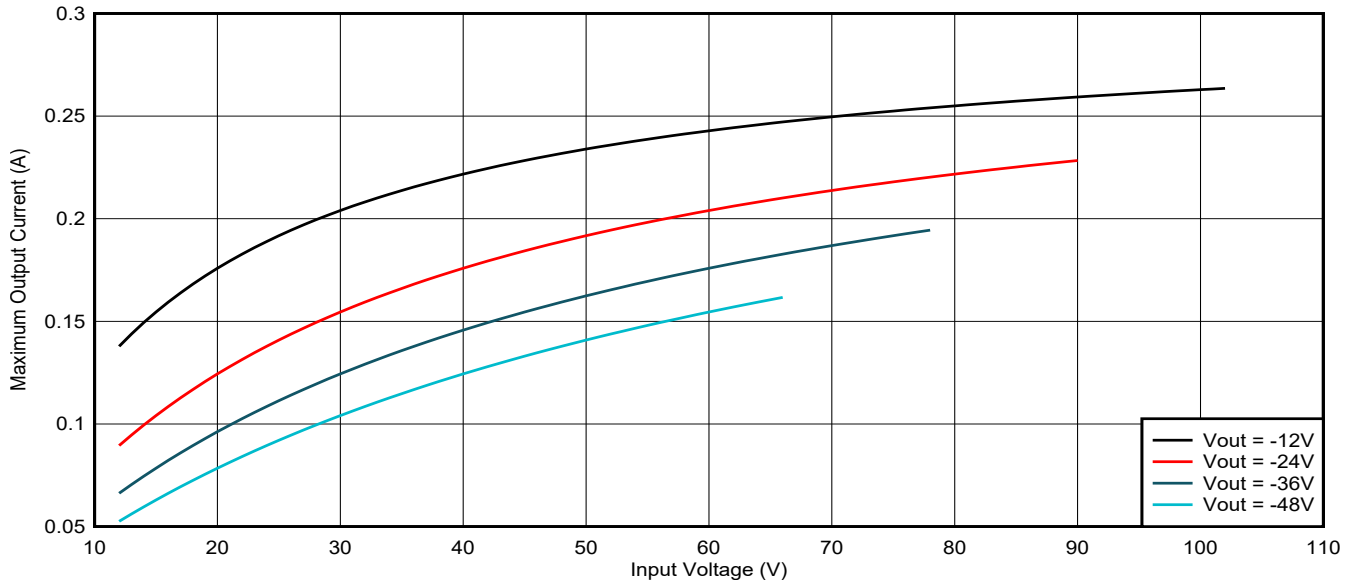
$$D = \frac{-24}{-24 - 12 \times 0.85} = 0.702 \quad (3)$$

In the case of the LM5168, which has a maximum current of 300 mA, the resulting maximum output current of the inverting buck-boost converter would be:

$$I_{OUT}(IBB) = 300 \text{ mA} \times (1 - 0.702) = 89 \text{ mA} \quad (4)$$

Table 1-1. Maximum Output Current Calculations for the LM5168

V _{OUT} (V)	V _{IN} (V)	I _{OUT_Buck} (A)	η	D	I _{OUT} (A)
-12	24	0.3	0.85	0.370	0.189
-24	24	0.3	0.85	0.541	0.138
-36	24	0.3	0.85	0.638	0.109
-48	24	0.3	0.85	0.702	0.089


Figure 1-2. Maximum Output Current Calculations for the LM5168 with Assumed 85% Efficiency

1.3 Voltage Range of Inverting Buck-Boost Configuration

When using a buck converter as an inverting buck-boost, the connection changes limit the voltage range from input to output that the part can safely operate at. The ground (GND) pin of the IC is no longer referenced to 0 V, and it is now the output of the converter. As a result, the maximum voltage over the IC can be calculated as V_{IN} minus $-V_{OUT}$. For example, if the input voltage is 60 V and the output is -80 V, then the voltage over the IC is 140 V. In the case of the LM5168, this configuration would exceed the maximum input voltage of 115 V across the part listed in the data sheet. It is important to keep the input and output voltage difference within the maximum voltage rating of the IC.

2 Design Considerations

2.1 Bypass Capacitor and Optional Schottky Diode

A new bypass capacitance, from V_{IN} to $-V_{OUT}$ is used to help with load transients. The value for the bypass capacitance, C_{IO} , can be chosen using input capacitance recommendations from the buck datasheet, but it is important to note that the voltage across the capacitors will be $V_{IN} + |-V_{OUT}|$. The capacitors used should be appropriately sized for the voltage difference between V_{IN} and $-V_{OUT}$. When the input supply is turned on, the bypass capacitance may cause the output to shortly swing positive before becoming negative. If the desired load is sensitive to a positive swing, then an optional Schottky diode can be placed across the output to clamp the voltage.

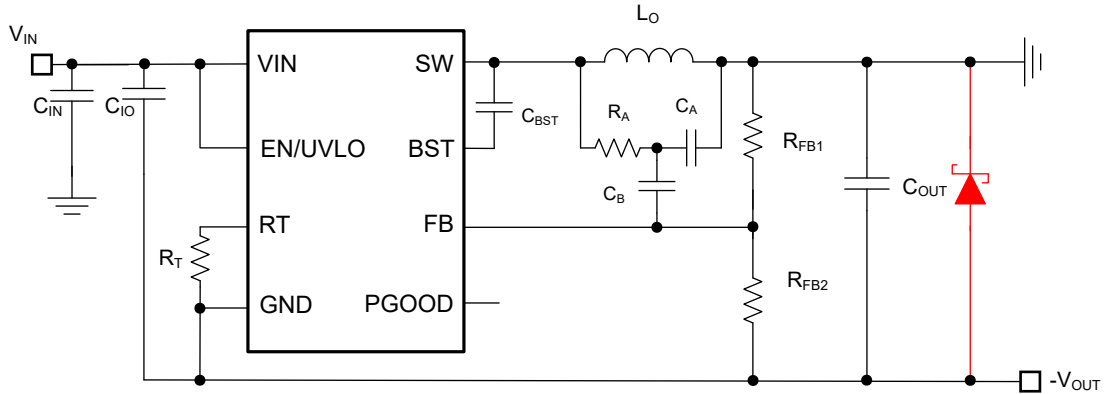


Figure 2-1. LM5168 Inverting Buck-Boost with Optional Schottky Diode

3 External Components

The LM5168 has integrated power MOSFETS and requires an inductor, input capacitance, output capacitance, and feedback resistors to be chosen by the designer. A ripple injection network is also needed for the feedback of the LM5168 because the device uses a constant on-time (COT) control architecture. Keeping in mind that the voltage across the inductor is now only V_{IN} , the feedback and ripple injection network can be designed following data sheet recommendations for the buck converter.

3.1 Capacitor Selection

The capacitance values for C_{IO} can follow the datasheet recommendations for input capacitance when using the LM5168 as a buck converter. An additional C_{IN} capacitance can be added to the inverting buck-boost as necessary. If needed, C_{IO} and C_{IN} can be increased. The output capacitance can also follow buck converter datasheet recommendations, but may need to be increased to improve performance.

3.2 Inductor Selection

The value of inductance is primarily chosen for a desired current ripple, which is usually selected to be between 20% and 40%. When selecting an inductor, be sure to choose an inductor that is rated for the maximum current which can be calculated using the equation in the output current section. Inductance is calculated as:

$$L = \frac{V_{in}}{F_s \times \Delta I_L} \times \frac{|V_{out}|}{V_{in} \times \eta + |V_{out}|} \quad (5)$$

where:

- F_s is the switching frequency

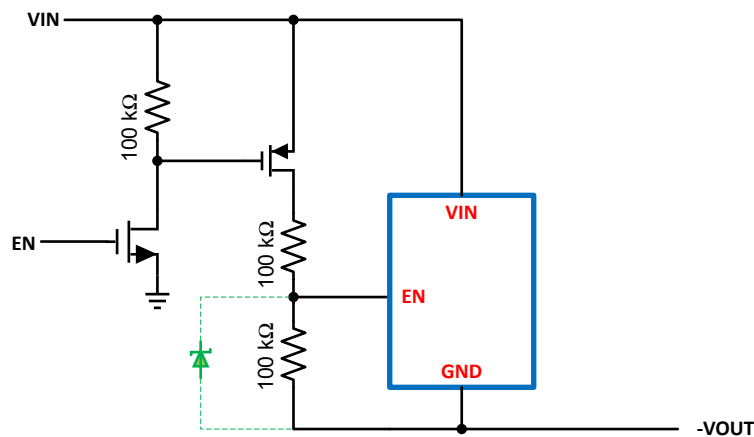
4 Digital Pin Configurations

4.1 Optional Enable (EN) Level Shifter

Since the ground of the buck converter IC is now referenced to the negative output voltage, a level shifter is required if a control signal is to be used on the enable pin. An example circuit is shown in Figure 4-1 that can be used to level shift an incoming enable signal. While the circuit requires two transistors, it has no hysteresis and requires no current from the control signal. If the enable pin is not rated for the full input voltage range, then a Zener diode must be used to clamp the enable pin below its maximum voltage. The enable pin needs to be configured properly even without a control signal, and the buck converter data sheet can be referenced for the proper connection of the EN pin.

When the enable signal is pulled low, then the NMOS switch is turned off, pulling the gate of the PMOS to V_{IN} . The PMOS then turns off, pulling the enable pin below the high-level threshold.

When the enable signal is pulled high, the NMOS switch is turned on, pulling the gate of the PMOS low. The PMOS then turns on, pulling the enable pin above the high level threshold from V_{IN} .



-VOUT is the negative output voltage of the inverting buck-boost converter

Figure 4-1. EN Pin Level Shifter

4.2 Power-Good (PG) Pin

Similar to EN, the power good flag needs to be level shifted if it is used for an inverting buck-boost application. The circuit shown in Figure 4-2 can be used to level shift the PGOOD logic as a signal that swings to zero volts. When using the circuit, the PGOOD pin needs to be rated for $|V_{OUT}|$.

When the internal PGOOD switch turns off, the gate of the first external MOSFET is pulled to ground, causing the MOSFET to turn on. With the first MOSFET on, the gate of the second MOSFET is pulled to $-V_{OUT}$, turning the second MOSFET off. With the second switch off, the PGOOD node is pulled to the logic voltage.

When the internal PGOOD switch turns on, the gate of the first external MOSFET is pulled to $-V_{OUT}$, turning off the MOSFET. With the first external MOSFET off, the gate of the second external MOSFET is pulled to the logic voltage of the controller. This causes the second external MOSFET to turn on and pull the PGOOD node to ground. When selecting the external MOSFETs, they must have a V_{GS} rating of at least $|V_{OUT}|$.

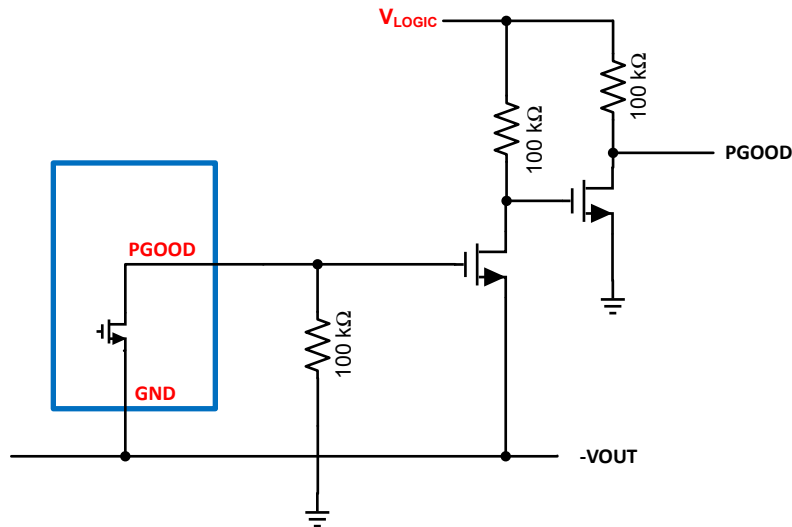


Figure 4-2. PG Pin Level Shifter

5 Typical Performance

5.1 $V_{OUT} = -12\text{ V}$ Typical Performance

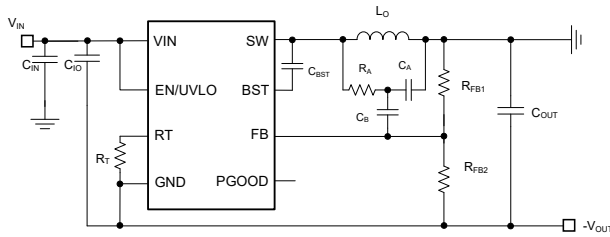


Figure 5-1. Schematic

COMPONENT VALUES FOR $V_{OUT} = -12\text{ V}$			
C_{IN}	4µF	250V	X7R or X5R
C_{OUT}	60µF	100V	X7R or X5R
C_{IO}	4µF	250V	X7R or X5R
L_O	220µH		
R_{FBT}	453kΩ	1%	
R_{FB2}	49.9kΩ	1%	
R_A	182kΩ	1%	
C_A	3300pF	100V	X7R or X5R
C_B	56pF	50V	X7R or X5R
C_{BST}	2200pF	50V	X7R or X5R
R_T	60.4kΩ	1%	

Figure 5-2. Bill of Materials

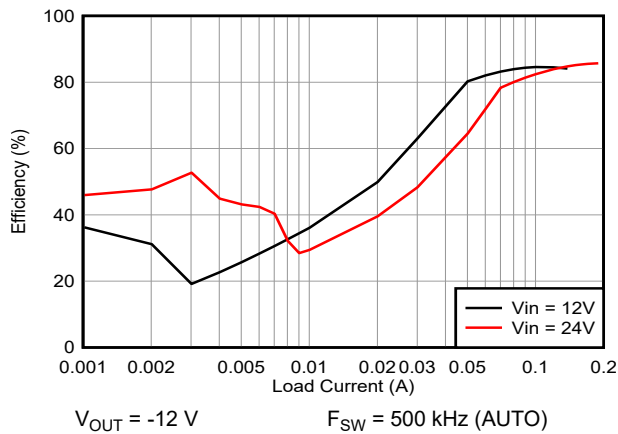


Figure 5-3. Efficiency vs. Load Current

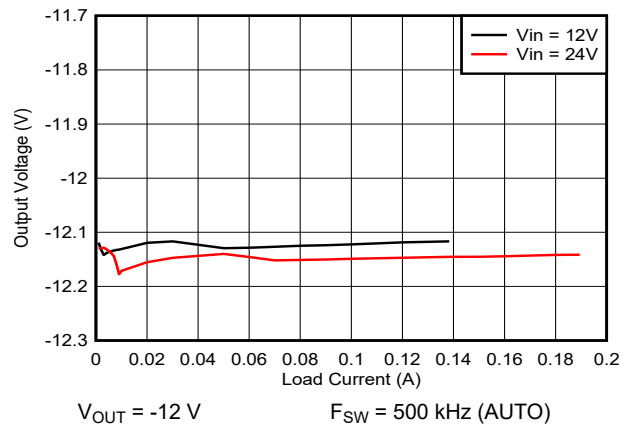
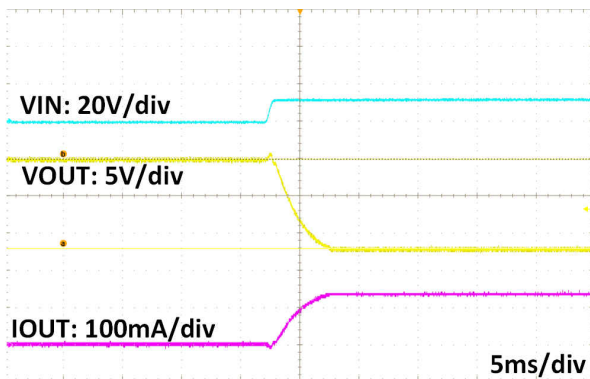
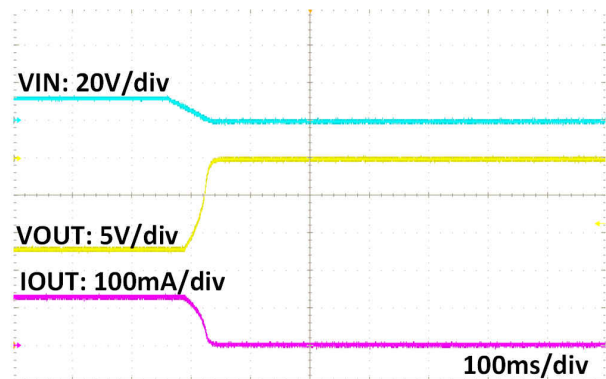


Figure 5-4. Load Regulation vs. Load Current



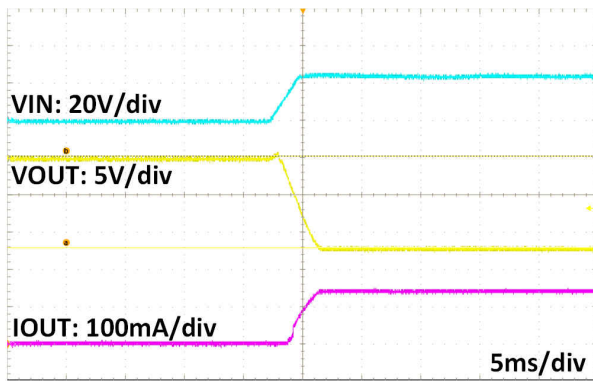
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-5. Startup at $V_{IN} = 12\text{ V}$



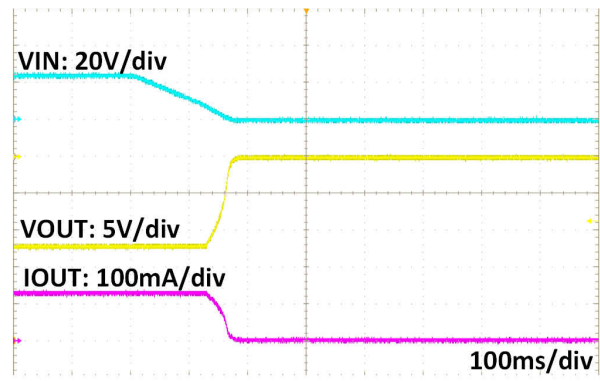
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-6. Shutdown at $V_{IN} = 12\text{ V}$



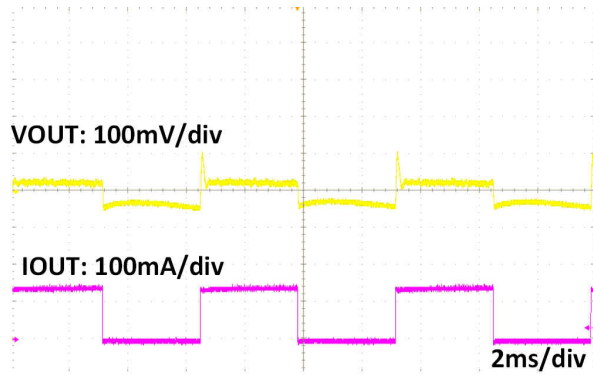
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-7. Startup at $V_{IN} = 24\text{ V}$



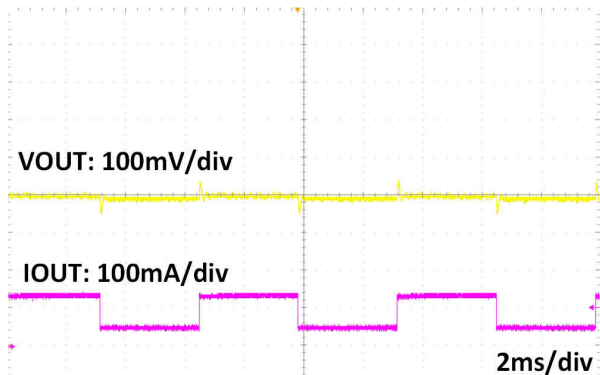
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-8. Shutdown at $V_{IN} = 24\text{ V}$



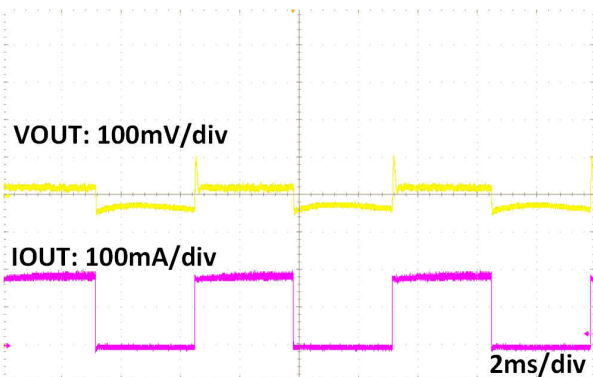
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 0\text{ mA to }138\text{ mA}$

Figure 5-9. Full Load Transient at $V_{IN} = 12\text{ V}$



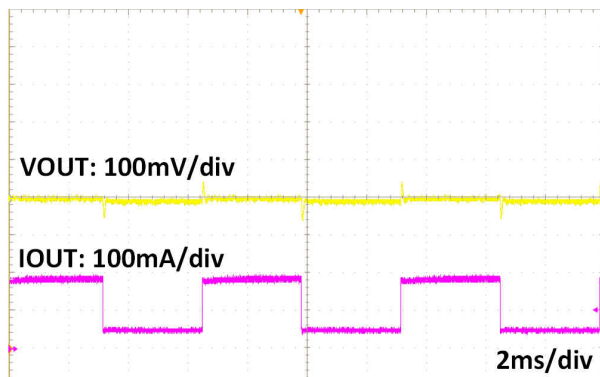
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 50\text{ mA to }138\text{ mA}$

Figure 5-10. Load Transient at $V_{IN} = 12\text{ V}$



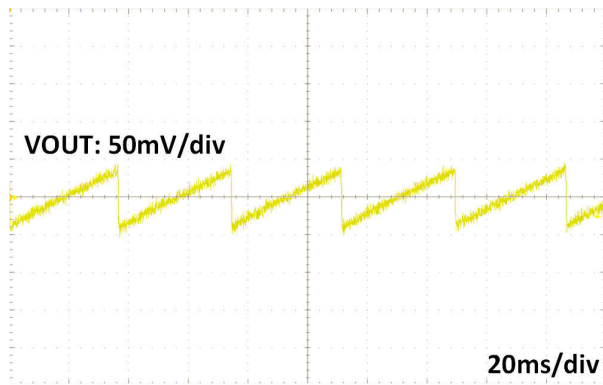
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 0\text{ mA to }189\text{ mA}$

Figure 5-11. Full Load Transient at $V_{IN} = 24\text{ V}$



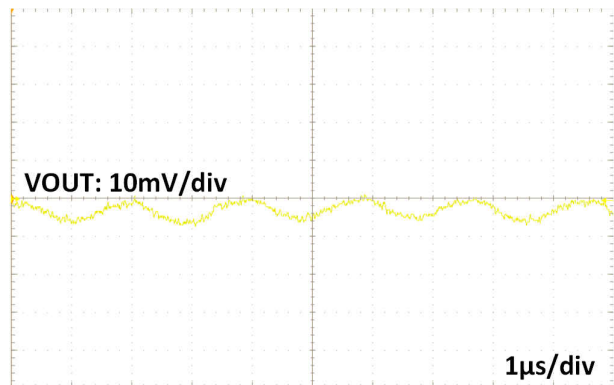
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 50\text{ mA to }189\text{ mA}$

Figure 5-12. Load Transient at $V_{IN} = 24\text{ V}$



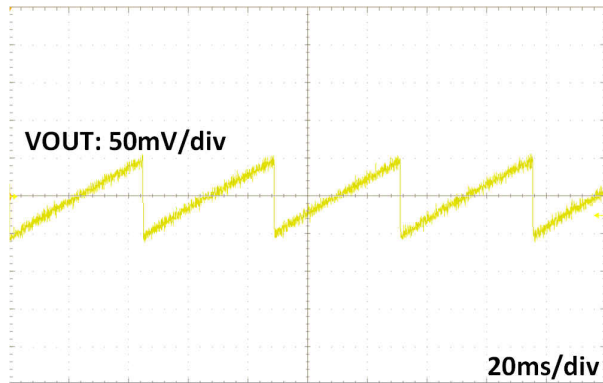
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 0\text{ A}$

Figure 5-13. No Load Output Ripple at $V_{IN} = 12\text{ V}$



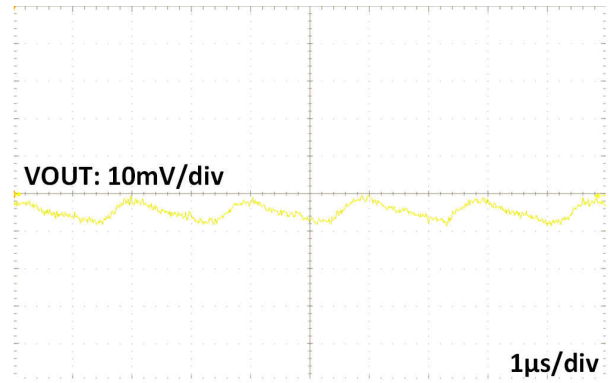
$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-14. Full Load Output Ripple at $V_{IN} = 12\text{ V}$



$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 0\text{ A}$

Figure 5-15. No Load Output Ripple at $V_{IN} = 24\text{ V}$



$V_{OUT} = -12\text{ V}$ $I_{LOAD} = 189\text{ mA}$

Figure 5-16. Full Load Output Ripple at $V_{IN} = 24\text{ V}$

5.2 V_{OUT} = -24 V Typical Performance

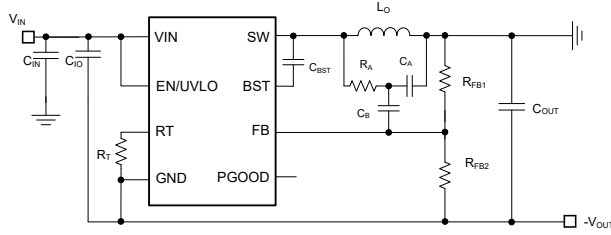


Figure 5-17. Schematic

COMPONENT VALUES FOR V _{OUT} = -24 V			
C _{IN}	4μF	250V	X7R or X5R
C _{OUT}	60μF	100V	X7R or X5R
C _{IO}	4μF	250V	X7R or X5R
L _O	220μH		
R _{FBT}	953kΩ	1%	
R _{FBB}	49.9kΩ	1%	
R _A	182kΩ	1%	
C _A	3300pF	100V	X7R or X5R
C _B	56pF	50V	X7R or X5R
C _{BST}	2200pF	50V	X7R or X5R
R _T	121kΩ	1%	

Figure 5-18. Bill of Materials

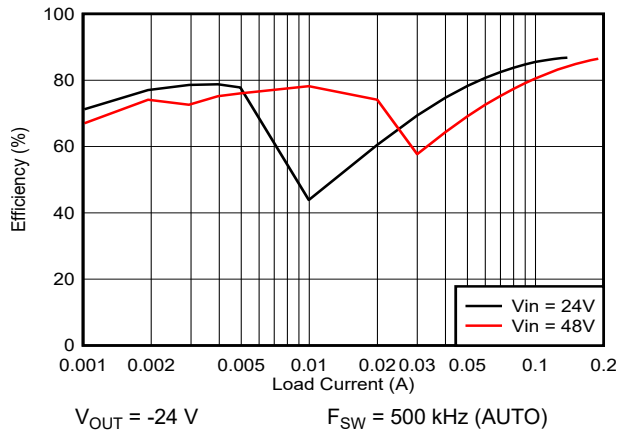


Figure 5-19. Efficiency vs. Load Current

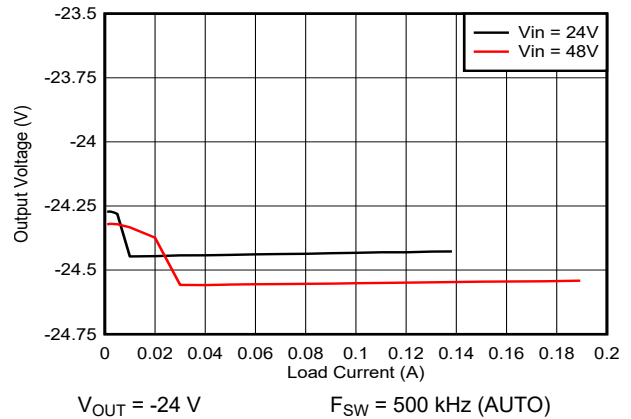


Figure 5-20. Load Regulation vs. Load Current

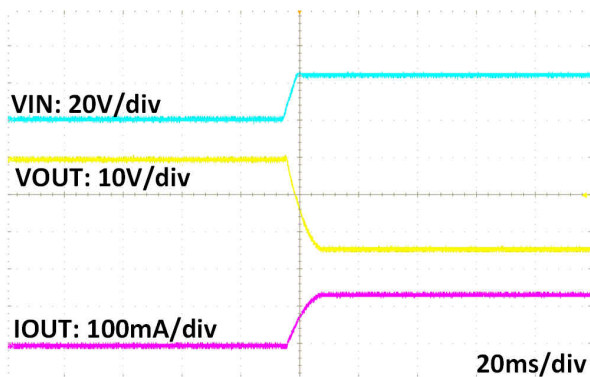


Figure 5-21. Startup at V_{IN} = 24 V

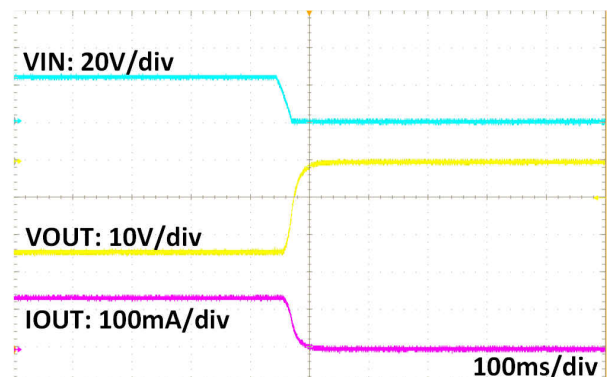
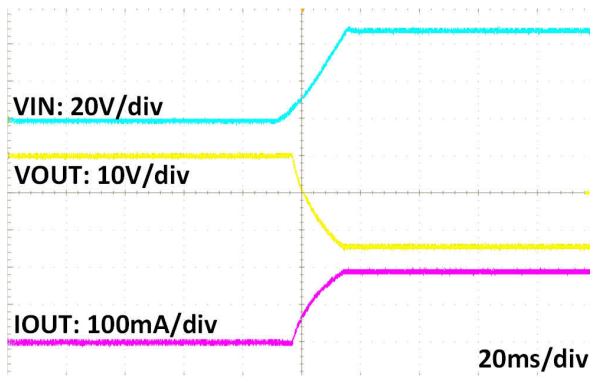
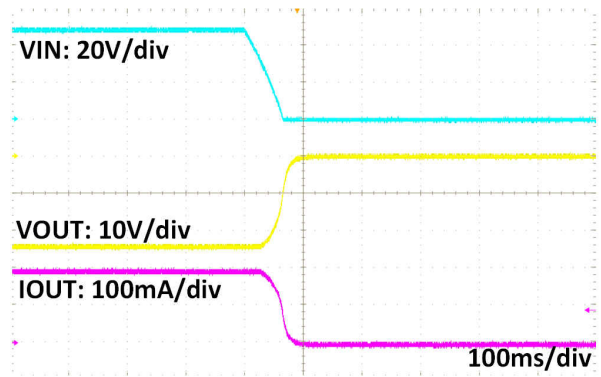


Figure 5-22. Shutdown at V_{IN} = 24 V



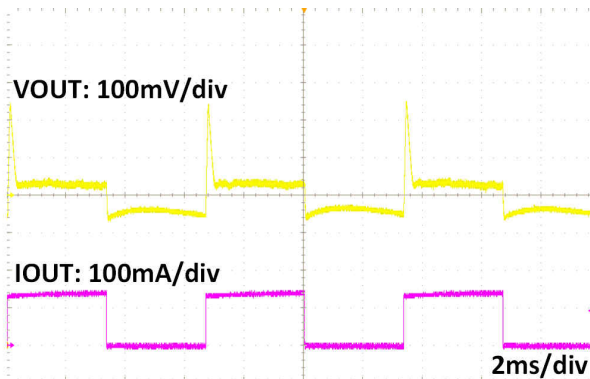
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 189\text{ mA}$

Figure 5-23. Startup at $V_{IN} = 48\text{ V}$



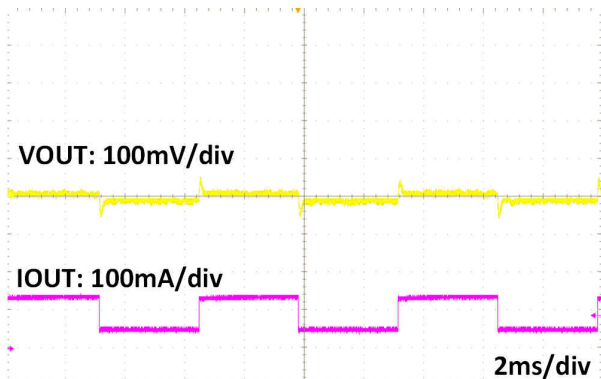
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 189\text{ mA}$

Figure 5-24. Shutdown at $V_{IN} = 48\text{ V}$



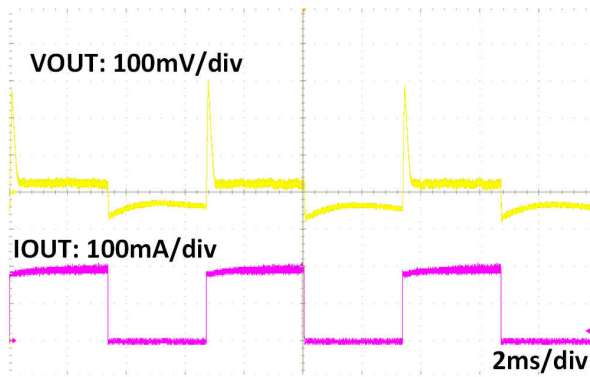
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 0\text{ mA to }138\text{ mA}$

Figure 5-25. Full Load Transient at $V_{IN} = 24\text{ V}$



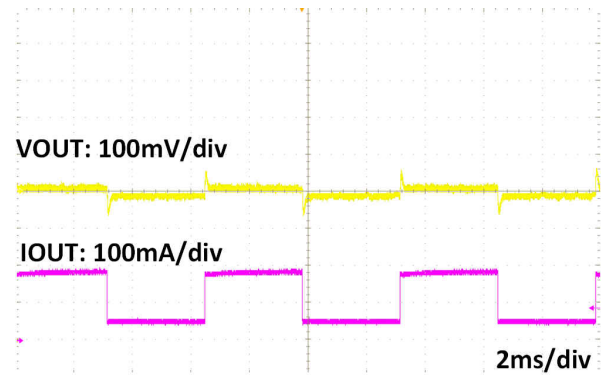
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 50\text{ mA to }138\text{ mA}$

Figure 5-26. Load Transient at $V_{IN} = 24\text{ V}$



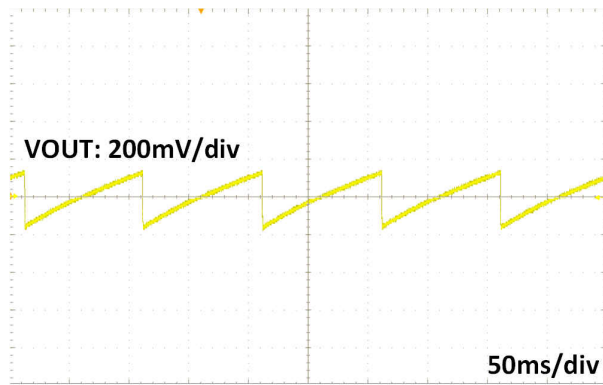
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 0\text{ mA to }189\text{ mA}$

Figure 5-27. Full Load Transient at $V_{IN} = 48\text{ V}$



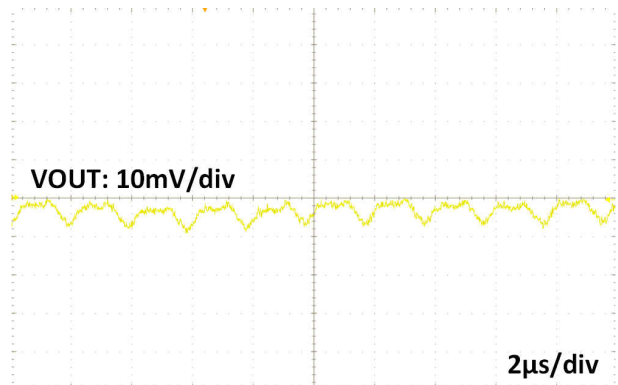
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 50\text{ mA to }189\text{ mA}$

Figure 5-28. Load Transient at $V_{IN} = 48\text{ V}$



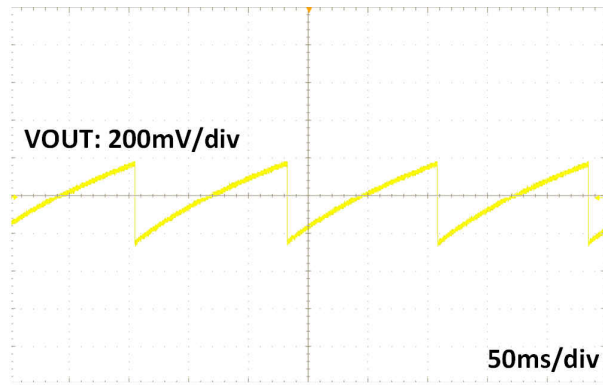
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 0\text{ A}$

Figure 5-29. No Load Output Ripple at $V_{IN} = 24\text{ V}$



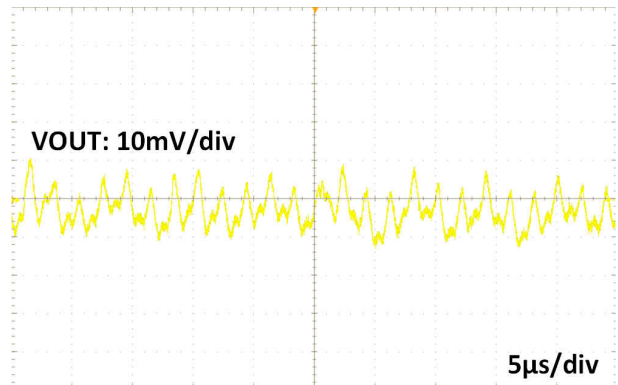
$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-30. Full Load Output Ripple at $V_{IN} = 24\text{ V}$



$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 0\text{ A}$

Figure 5-31. No Load Output Ripple at $V_{IN} = 48\text{ V}$



$V_{OUT} = -24\text{ V}$ $I_{LOAD} = 189\text{ mA}$

Figure 5-32. Full Load Output Ripple at $V_{IN} = 48\text{ V}$

5.3 $V_{OUT} = -48\text{ V}$ Typical Performance

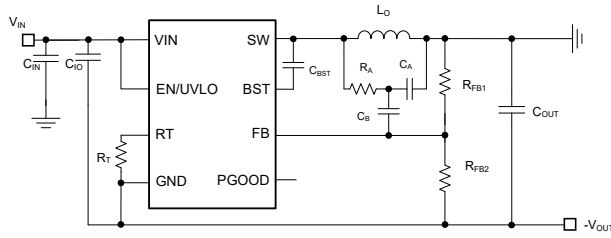


Figure 5-33. Schematic

COMPONENT VALUES FOR $V_{OUT} = -48\text{ V}$			
C_{IN}	4µF	250V	X7R or X5R
C_{OUT}	60µF	100V	X7R or X5R
C_{IO}	4µF	250V	X7R or X5R
L_O	220µH		
R_{FB1}	1.96MΩ	1%	
R_{FB2}	49.9kΩ	1%	
R_A	182kΩ	1%	
C_A	3300pF	100V	X7R or X5R
C_B	56pF	50V	X7R or X5R
C_{BST}	2200pF	50V	X7R or X5R
R_T	243kΩ	1%	

Figure 5-34. Bill of Materials

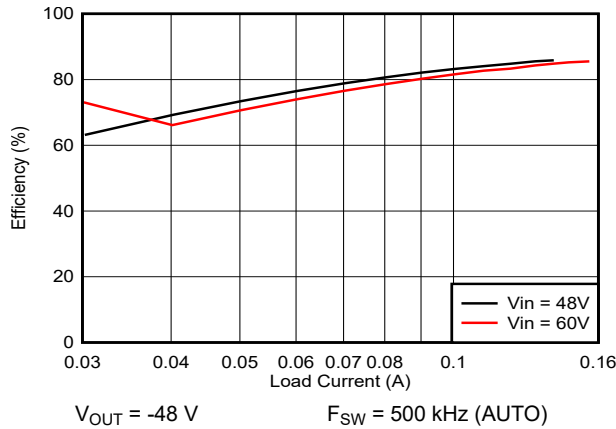


Figure 5-35. Efficiency vs. Load Current

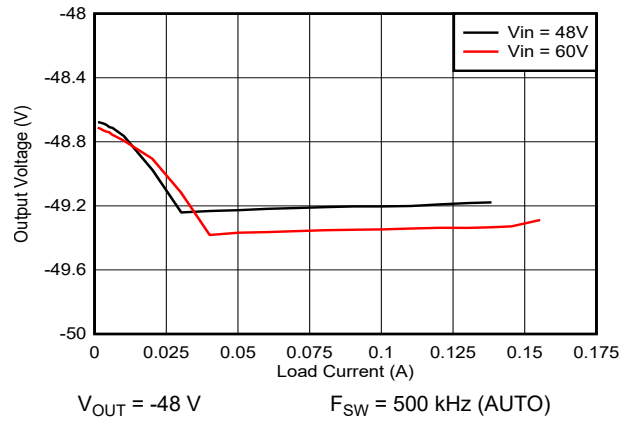
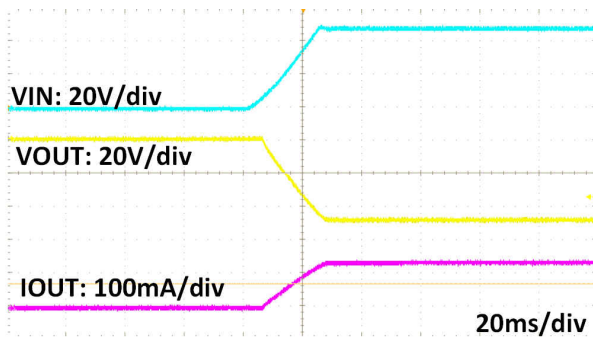
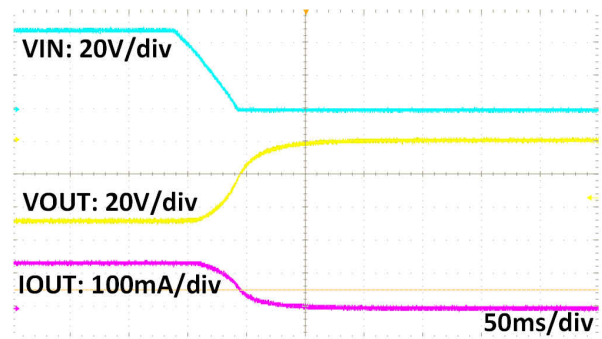


Figure 5-36. Load Regulation vs. Load Current



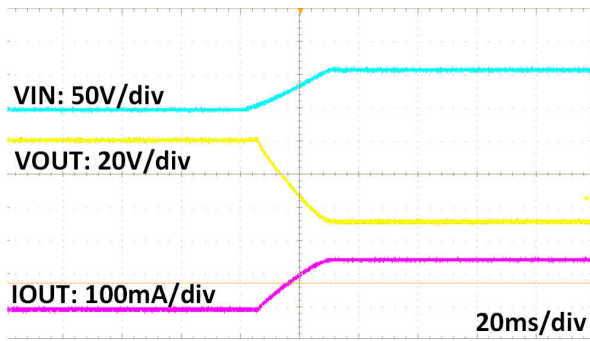
$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-37. Startup at $V_{IN} = 48\text{ V}$



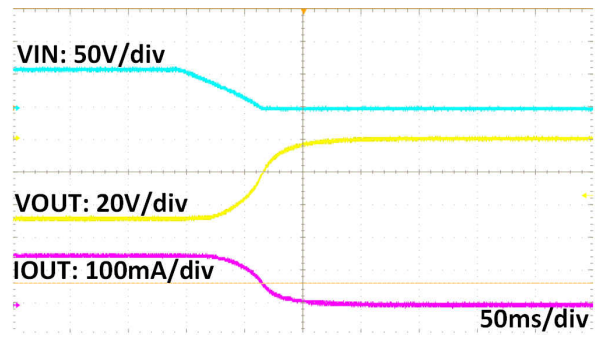
$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 138\text{ mA}$

Figure 5-38. Shutdown at $V_{IN} = 48\text{ V}$



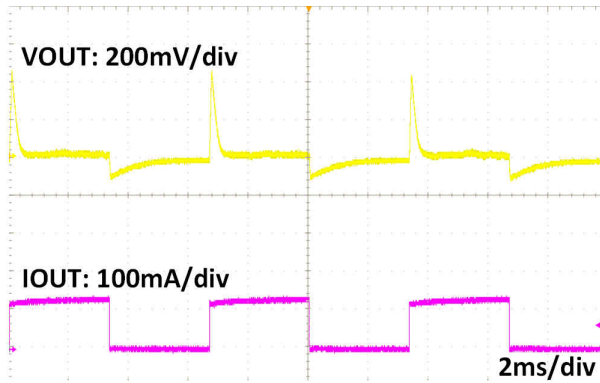
$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 155\text{ mA}$

Figure 5-39. Startup at $V_{IN} = 60\text{ V}$



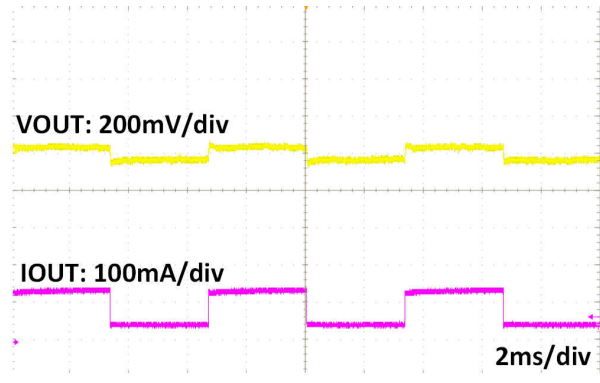
$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 155\text{ mA}$

Figure 5-40. Shutdown at $V_{IN} = 60\text{ V}$



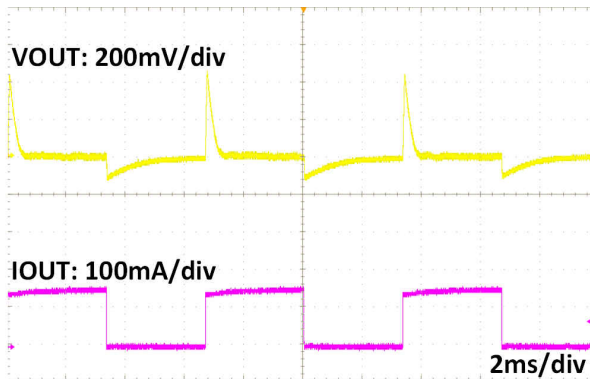
$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 0\text{ mA to }138\text{ mA}$

Figure 5-41. Full Load Transient at $V_{IN} = 48\text{ V}$



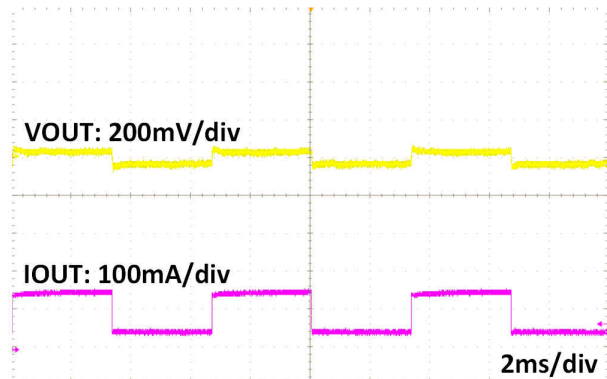
$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 50\text{ mA to }138\text{ mA}$

Figure 5-42. Load Transient at $V_{IN} = 48\text{ V}$



$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 0\text{ mA to }155\text{ mA}$

Figure 5-43. Full Load Transient at $V_{IN} = 60\text{ V}$



$V_{OUT} = -48\text{ V}$ $I_{LOAD} = 50\text{ mA to }155\text{ mA}$

Figure 5-44. Load Transient at $V_{IN} = 60\text{ V}$

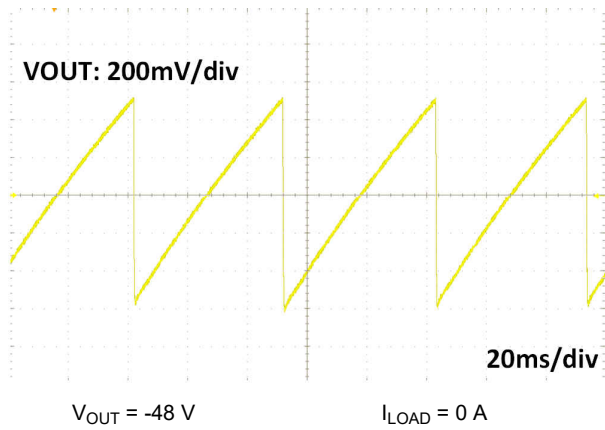


Figure 5-45. No Load Output Ripple at $V_{IN} = 48\text{ V}$

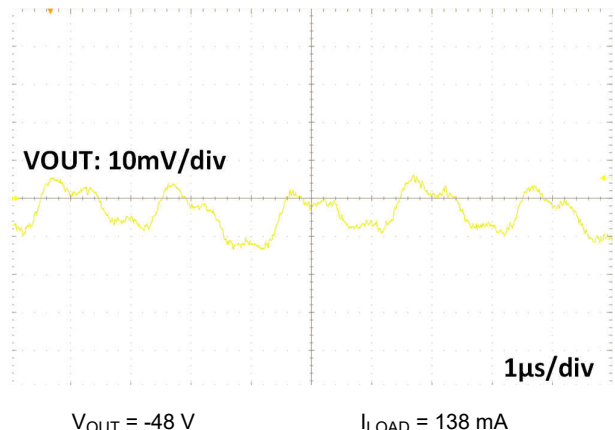


Figure 5-46. Full Load Output Ripple at $V_{IN} = 48\text{ V}$

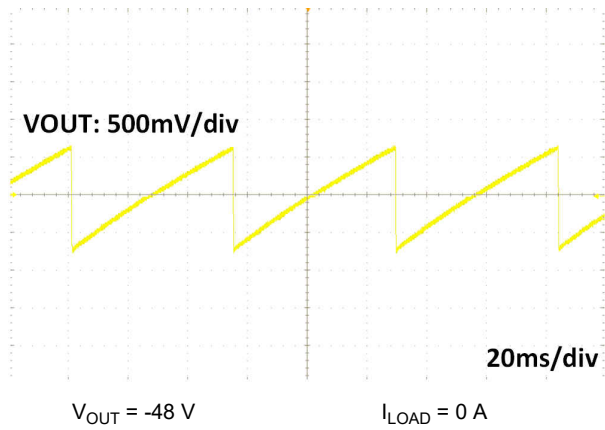


Figure 5-47. No Load Output Ripple at $V_{IN} = 60\text{ V}$

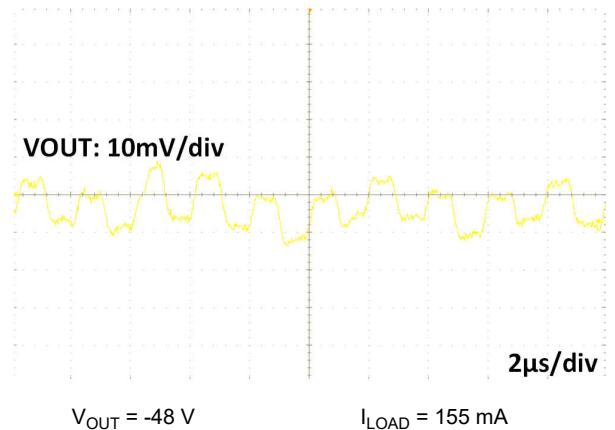


Figure 5-48. Full Load Output Ripple at $V_{IN} = 60\text{ V}$

6 Conclusion

The LM5168 is a buck converter that can be configured as an inverting buck-boost (IBB) topology by changing the output voltage and ground connections. Since the IBB is referenced to $-V_{OUT}$ rather than ground, the input voltage range of the LM5168 is limited depending on the magnitude of $-V_{OUT}$. The maximum possible output current is also limited since the maximum inductor current is always larger than the maximum output current. This report explains the IBB topology and how to select the external components for a design. Data is provided from a test circuit. For further reading on the inverting buck-boost topology, refer to the [Working with Inverting Buck-Boost Converters](#) application note.

7 References

1. Texas Instruments, [Working with Inverting Buck-Boost Converters](#) application note.
2. Texas Instruments, [LM5169, LM5168 0.65-A/0.3-A, 120-V, Step-Down Converter with Fly-Buck™ Converter Capability](#) data sheet.
3. Texas Instruments, [Inverting Application for the LMZM23601 and LMZM23600](#) application note.
4. Texas Instruments, [Using the TPSM5601R5H-IBB-EVM](#) users guide.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated