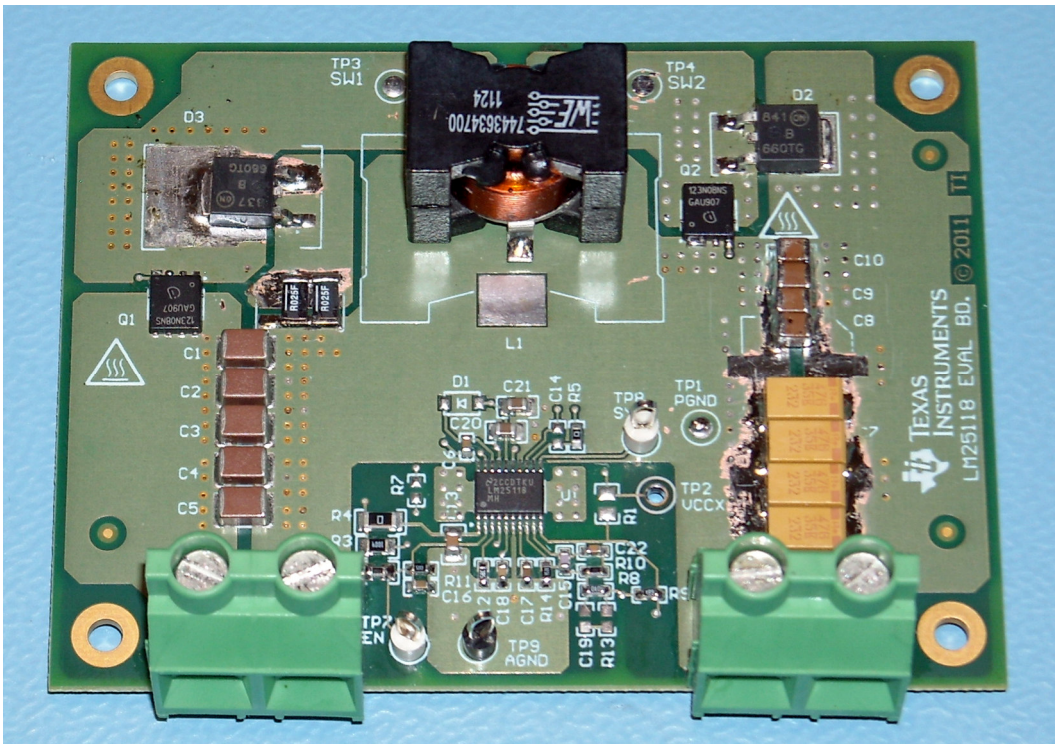
## Buck-Boost with 28.0V @ 2.5A

- Input 10..32V DC
- Output 28.0V @ 2.5A
- Controller LM25118
- Free-Running switching frequency of 150 kHz, synchronized to 175 kHz
- Modified “LM25118 Evaluation Board”



# 1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 21V, with no load on the 28.0V output.

Channel C1: **Input voltage**
5V/div, 5ms/div

Channel C2: **Output voltage**
5V/div, 5ms/div

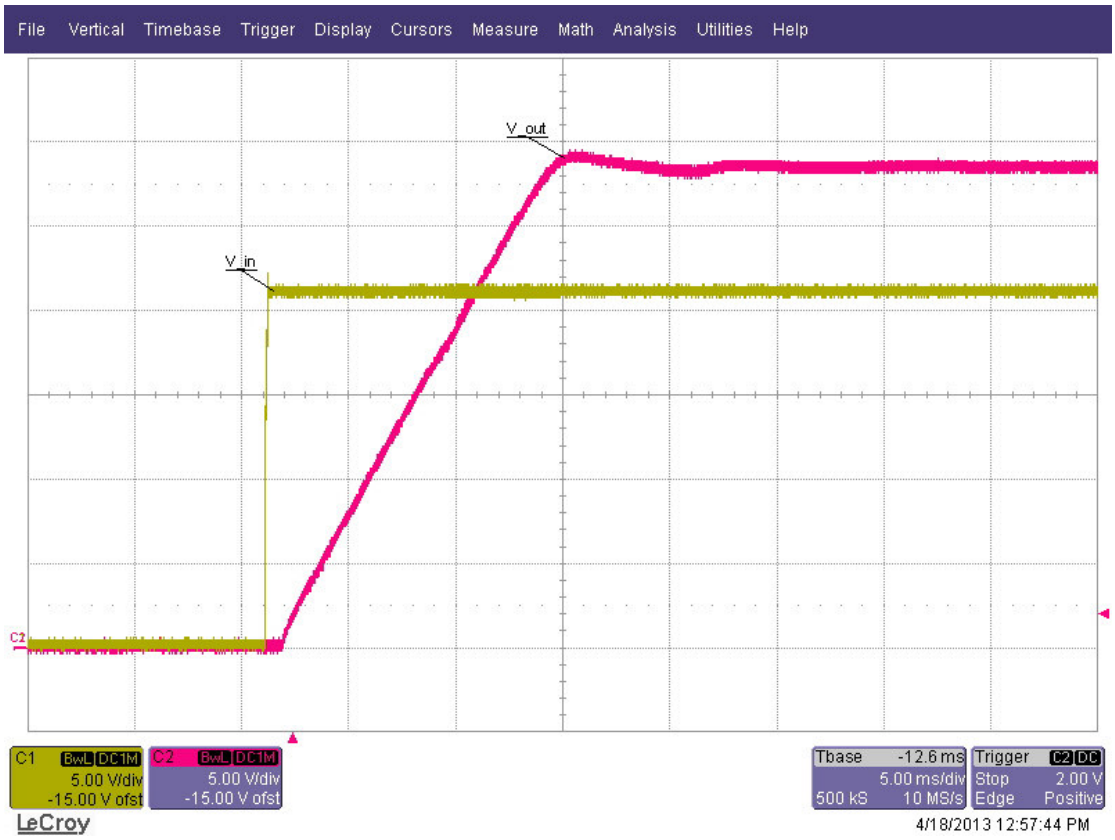



**Figure 1**

## 2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 21V with a 2.5A load on the 28.0V output.

Channel C1: **Input voltage**
5V/div, 1ms/div

Channel C2: **Output voltage**
5V/div, 1ms/div

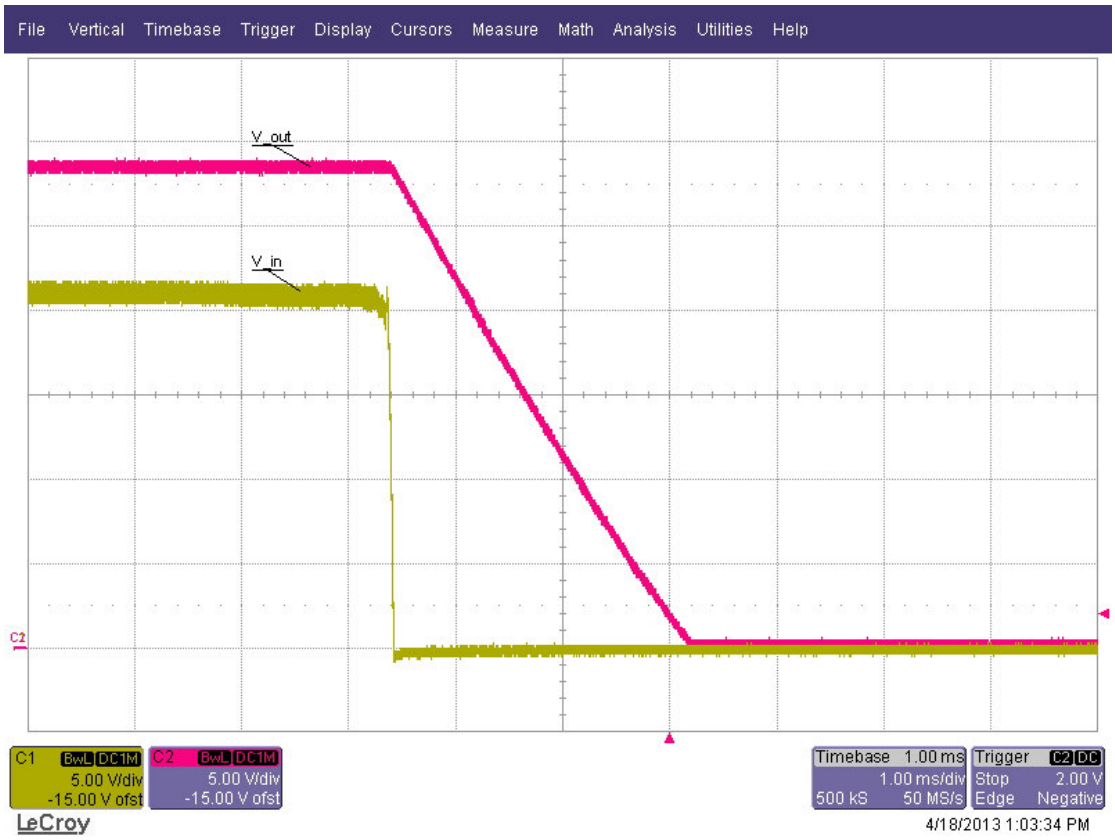



**Figure 2**

# 3 Efficiency

The efficiency and load regulation at 10.0V, 21.0V and 32.0V input voltage are shown in Figure 3 and Figure 4.

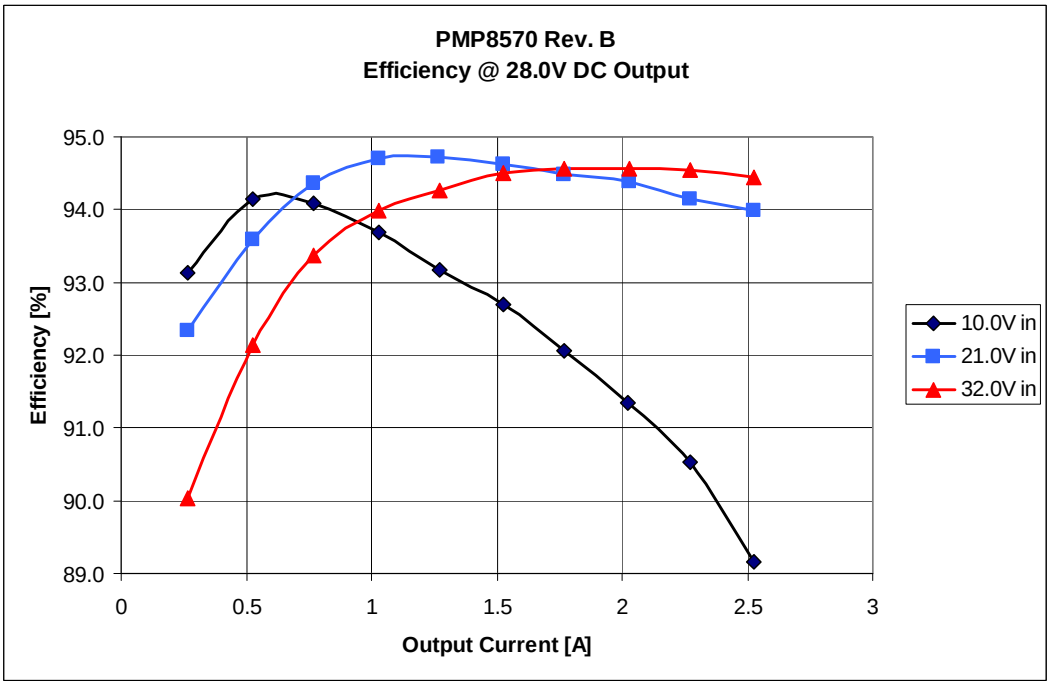



**Figure 3**

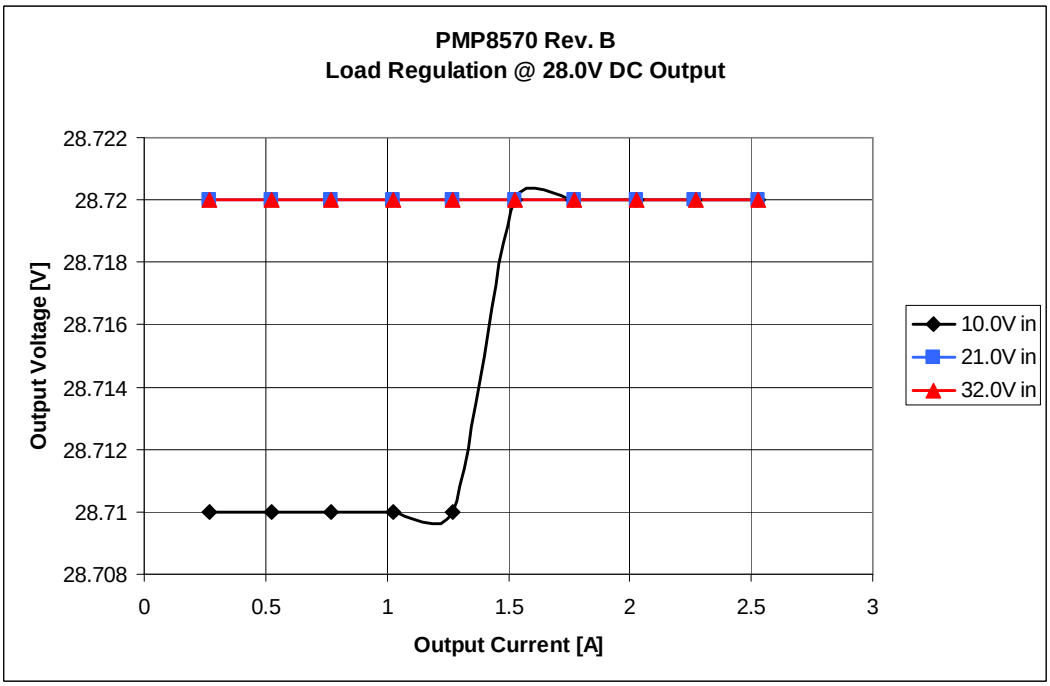



**Figure 4**

# 4 Output ripple voltage

The output ripple voltage at 10.0V, 21.0V and 32.0V input voltage are shown in Figure 5.

Channel M1: **Output voltage**, AC coupled, 380mV peak-peak @ 10.0V input voltage 200mV/div, 5us/div

Channel M2: **Output voltage**, AC coupled, 200mV peak-peak @ 21.0V input voltage 200mV/div, 5us/div

Channel M3: **Output voltage**, AC coupled, 180mV peak-peak @ 32.0V input voltage 200mV/div, 5us/div

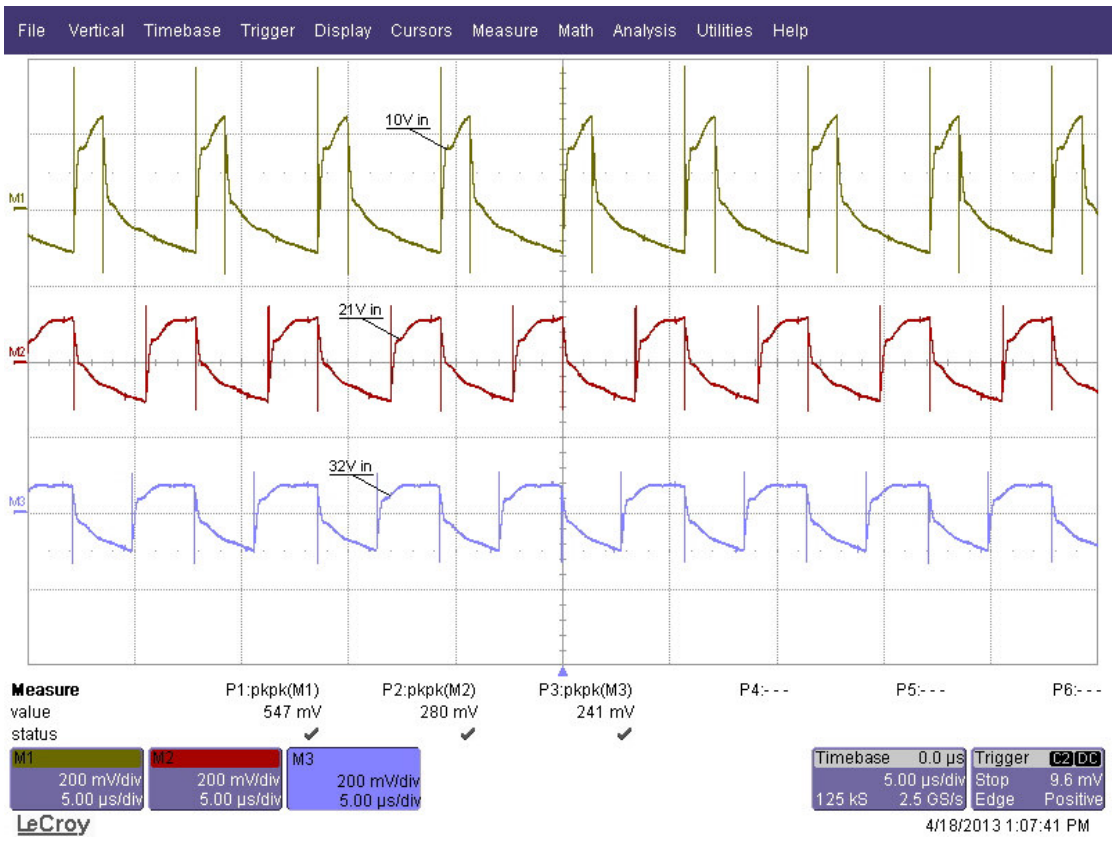



**Figure 5**

# 5 Load step

The response to a load step and a load dump at an input voltage of 10.0V is shown in Figure 6.

Channel C2: **Output voltage**, -1.57V undershoot, 1.43V overshoot
1V/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.35A to 2.2A
1.0A/div, 1ms/div

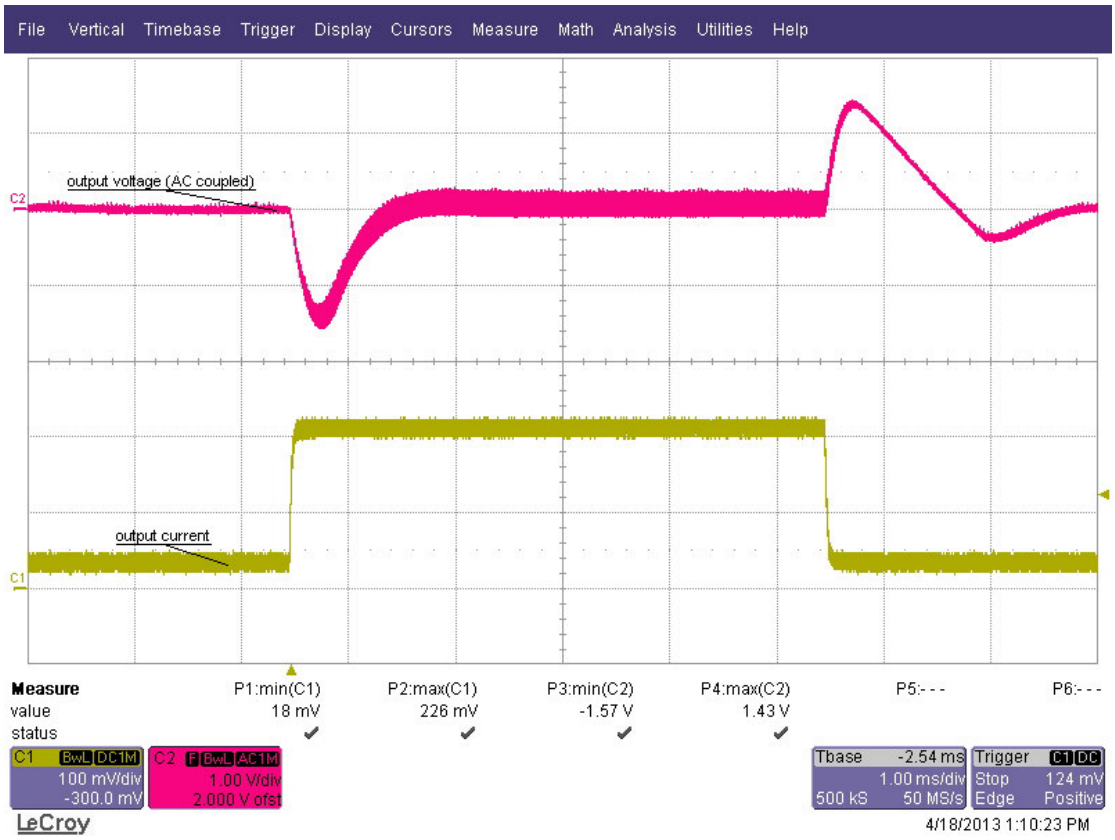



**Figure 6**

The response to a load step and a load dump at an input voltage of 21.0V is shown in Figure 7.

Channel C2: **Output voltage**, -1.03V undershoot, 0.94V overshoot
1V/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.35A to 2.2A
1.0A/div, 1ms/div

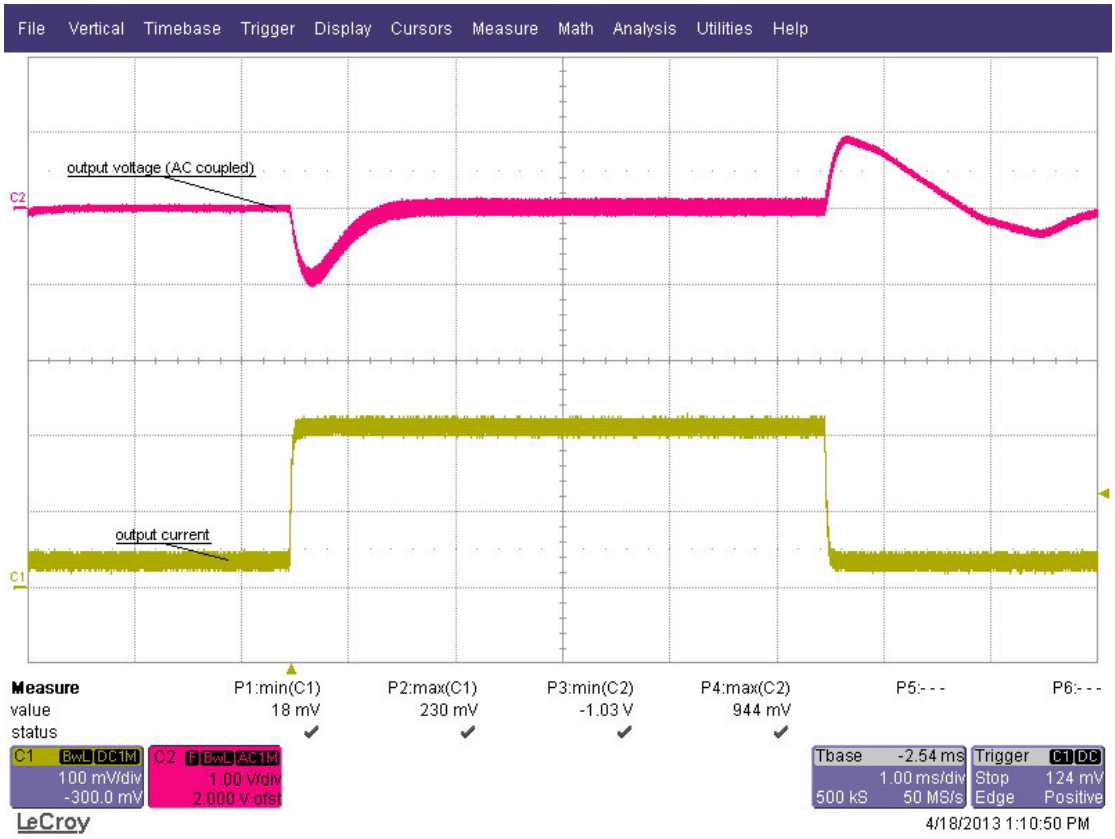



**Figure 7**

The response to a load step and a load dump at an input voltage of 32.0V is shown in Figure 8.

Channel C2: **Output voltage**, -1.25V undershoot, 0.88V overshoot
1V/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.35A to 2.2A
1.0A/div, 1ms/div

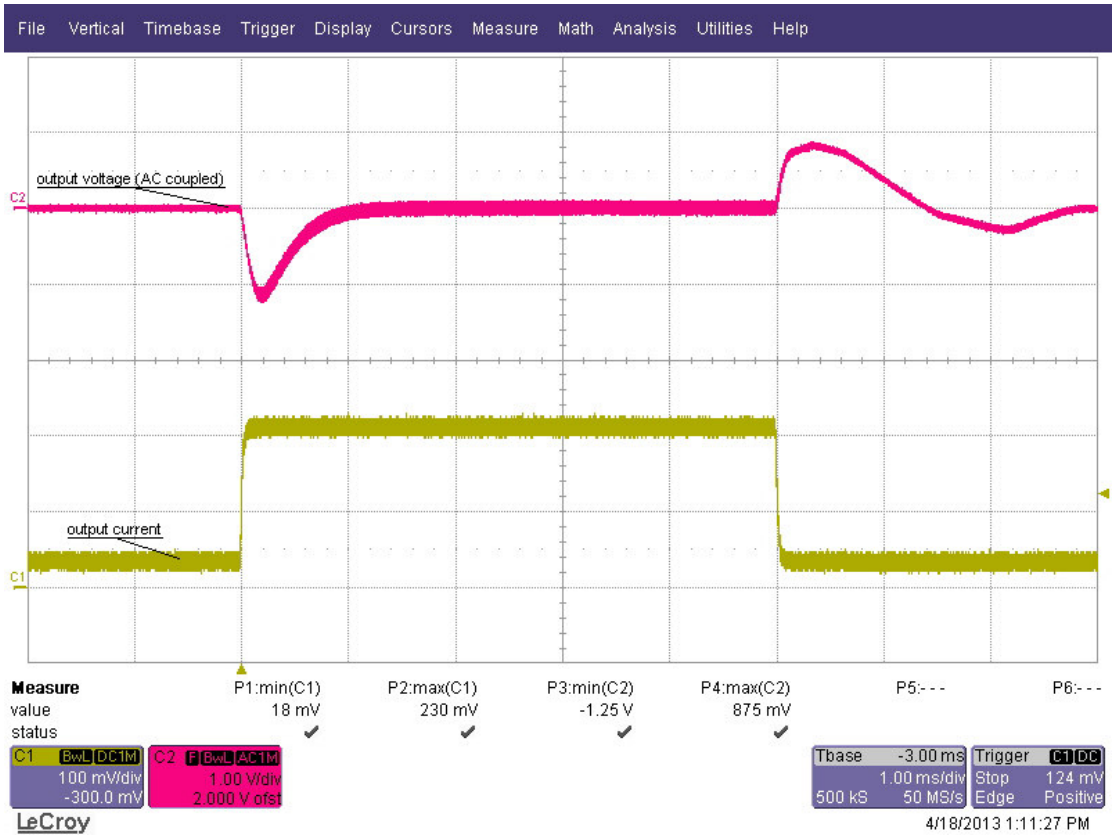



**Figure 8**

## 6 Frequency response

Figure 9 shows the loop response of the 28.0V output at 10.0V, 21.0V and 32.0V V input voltage and a 2.5A load.

**10.0V input**

- 66 deg phase margin @ crossover frequency 2.1 kHz
- -15 db gain margin

**21.0V input**

- 65 deg phase margin @ crossover frequency 1.6 kHz
- -22 db gain margin

**32.0V input**

- 62 deg phase margin @ crossover frequency 1.3 kHz
- -19 db gain margin

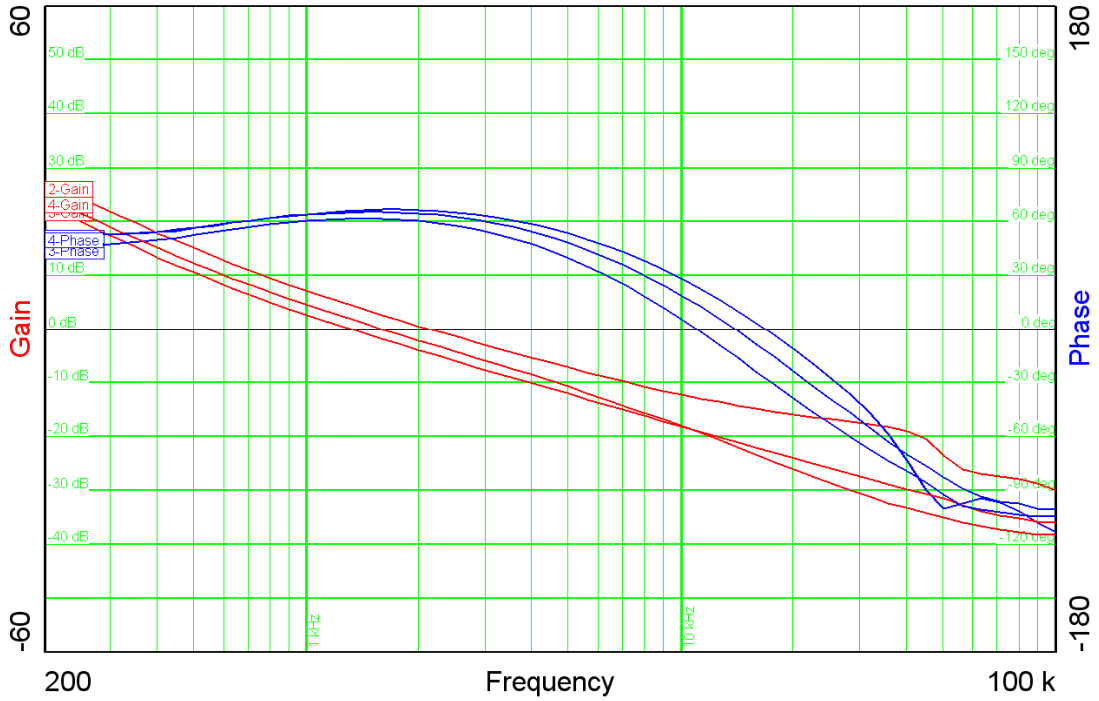



**Figure 9**

# 7 Switching Node

The drain-source voltage on the switching node (low side FET Q2) is shown in Figure 10. The image was captured with 10.0V input and a 2.5A load.

Channel C2: **Drain-source voltage**, -7.1V minimum voltage, 41.2V maximum voltage 10V/div, 5us/div

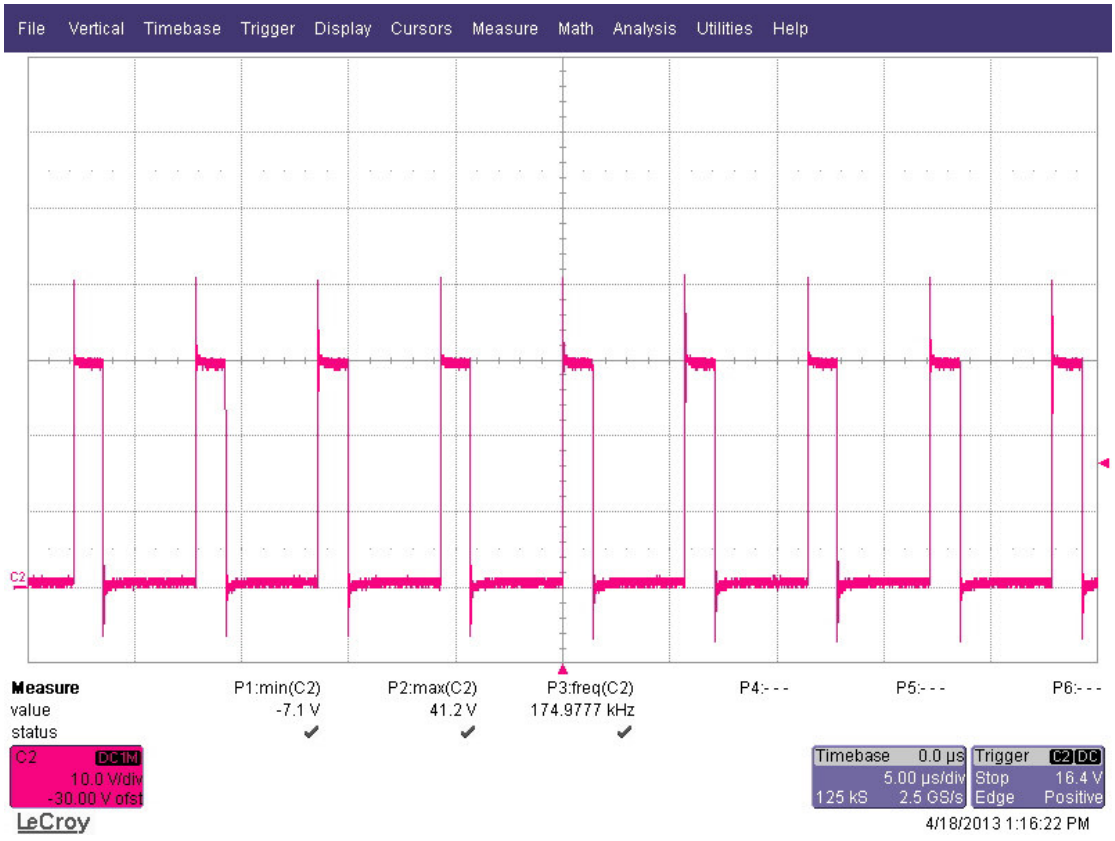



**Figure 10**

## 8 Thermal measurement

The thermal image (Figure 11) shows the circuit at an ambient temperature of 21 °C with an input voltage of 21.0V and a load of 2.5A.

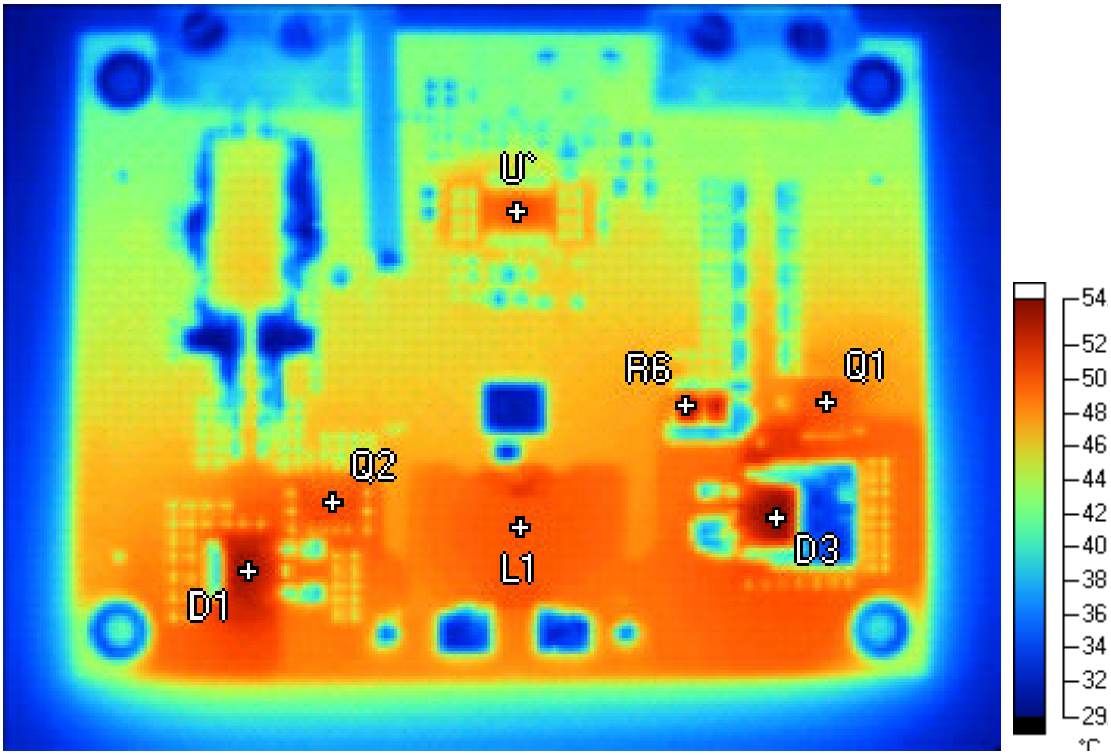



**Figure 11**

**Markers**

| Label | Temperature | Emissivity | Background |
|---|---|---|---|
| D1 | 54.1 °C | 0.95 | 21.0 °C |
| L1 | 50.1 °C | 0.95 | 21.0 °C |
| D3 | 54.6 °C | 0.95 | 21.0 °C |
| Q1 | 50.0 °C | 0.95 | 21.0 °C |
| Q2 | 50.3 °C | 0.95 | 21.0 °C |
| R6 | 54.3 °C | 0.95 | 21.0 °C |
| U` | 50.4 °C | 0.95 | 21.0 °C |

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