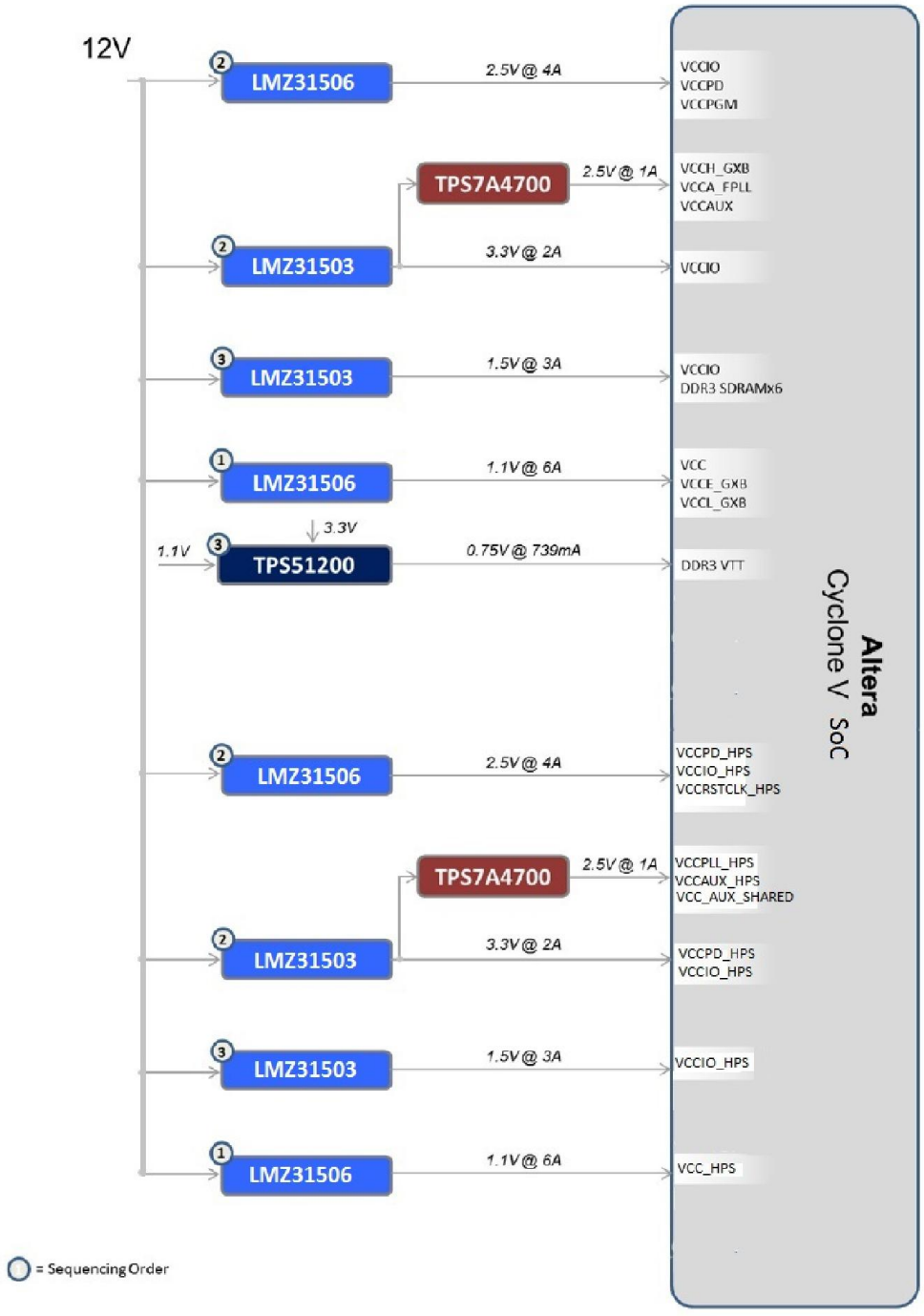
# PMP9353_RevA Test Results

# 1. Block Diagram



## 2. Startup/Sequencing

The startup waveform is shown in Figure 1. The input voltage is 12V, with no load at the output.

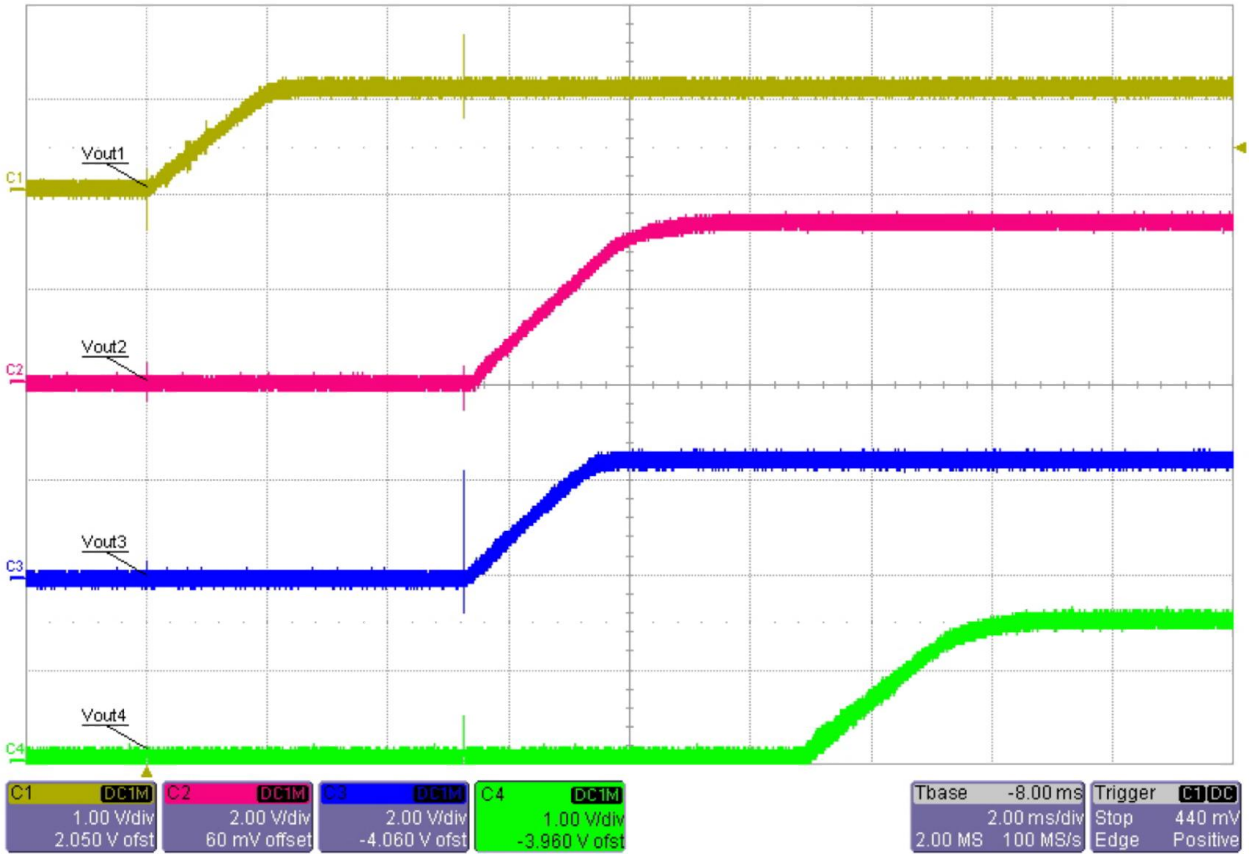



Figure 1

*Ch1 => Output voltage 1.1V order #1*
*Ch2 => Output voltage 3.3V order #2*
*Ch3 => Output voltage 2.5V order #2*
*Ch4 => Output voltage 1.5V order #3*
*2ms/div*
*Full Bandwidth*

A selection of startup waveforms is shown in Figure 1.1 to demonstrate LDO startup. The input voltage is 12V, with no load at the output.

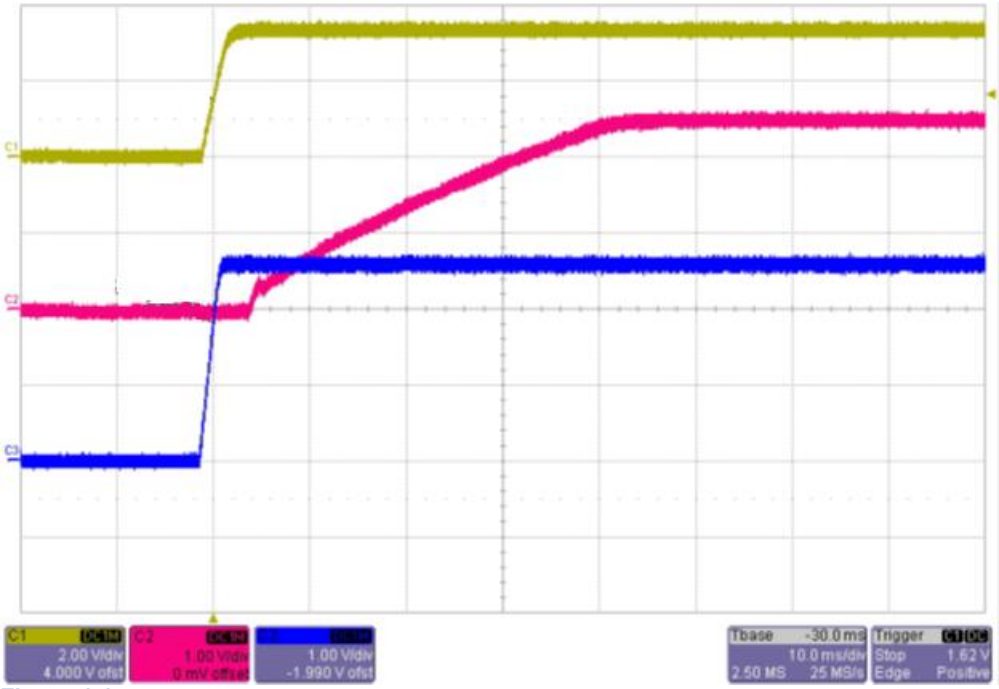



**Figure 1.1**

*Ch1 => Output voltage 3.3V order #2*
*Ch3 => Output voltage 2.5V order #2*
*Ch2 => LDO Output voltage 2.5V order #2 + LDO delay*
*2ms/div*
*Full Bandwidth*

## 3. Synchronization

The switching nodes of the buck stages are shown in Figure 2. The input voltage is 12V, with no load at the output.

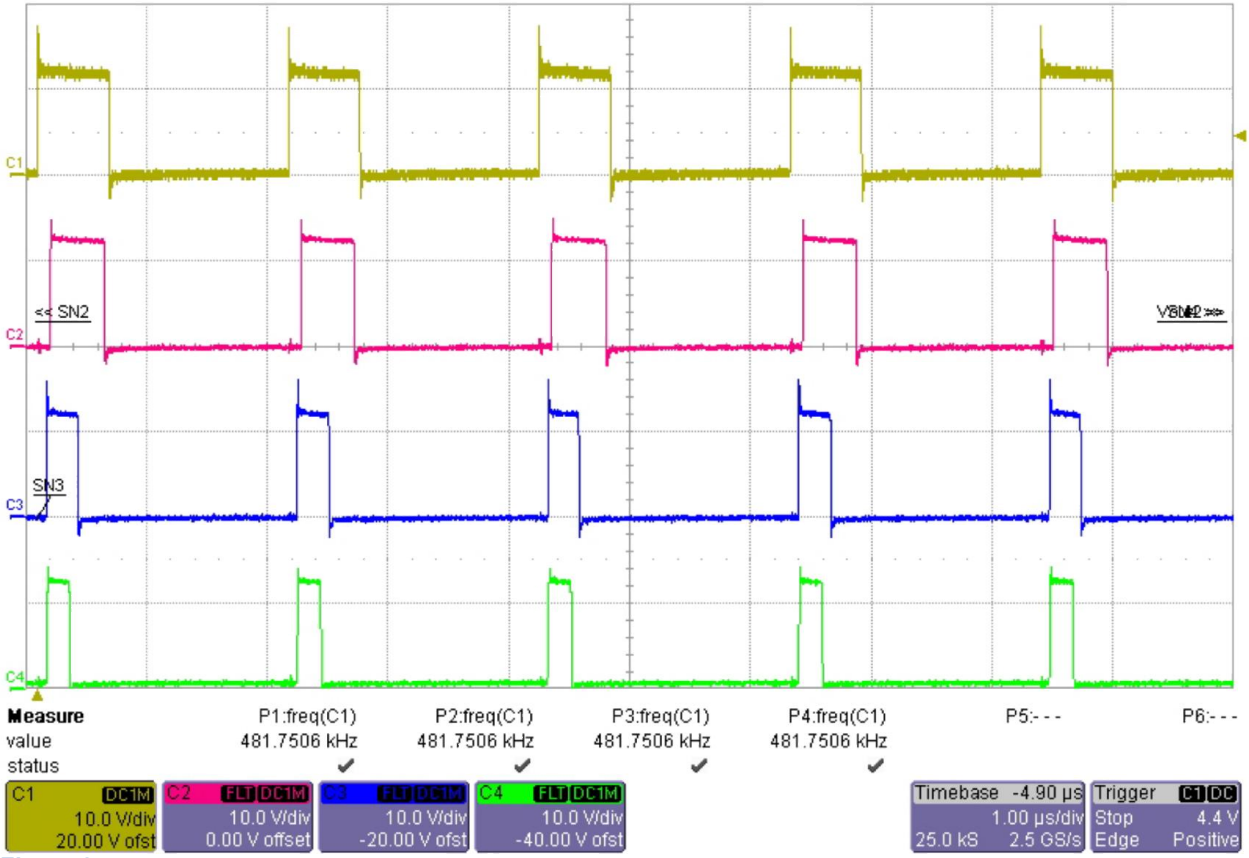



Figure 2

*Ch1 => Switching node for 3.3 Vout*
*Ch2 => Switching node for 2.5 Vout*
*Ch3 => Switching node for 1.5 Vout*
*Ch4 => Switching node for 1.1 Vout*
*Common frequency: 481.75 kHz*
*1µs/div*
*Full Bandwidth*

# 4. DDR Tracking

DDR tracking is shown in the Figures 3 and 4.

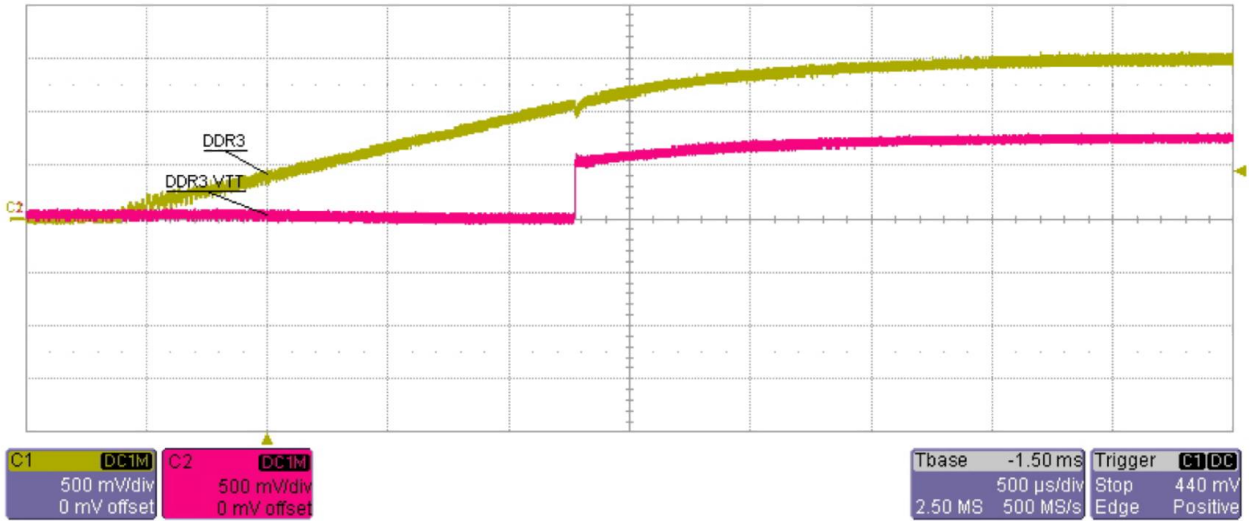



Figure 3

*Ch1 => DDR3 1.5V output voltage from buck stage*
*Ch2 => DDR3 0.75V termination voltage from TPS51200*
*500µs/div*
*Full Bandwidth*

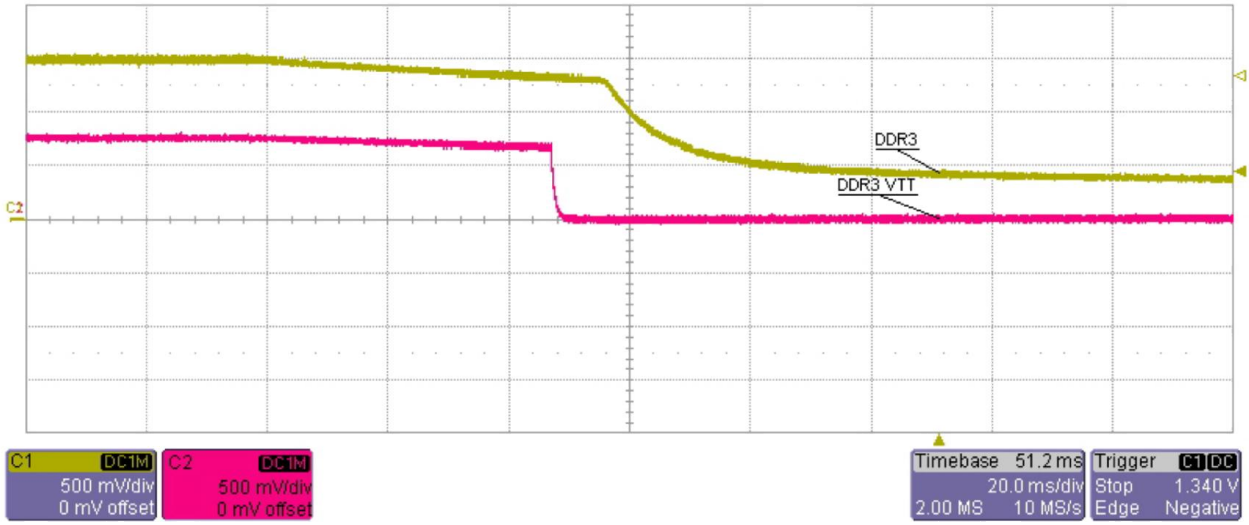



Figure 4

*Ch1 => DDR3 1.5V output voltage from buck stage*
*Ch2 => DDR3 0.75V termination voltage from TPS51200*
*20ms/div*
*Full Bandwidth*

## 5. Efficiency

The respective efficiencies of the buck stages providing 1.1V, 1.5V, 3.3V, and 2.5V are shown in Figures 5, 6, 7, and 8 below. The input voltage is 12V.

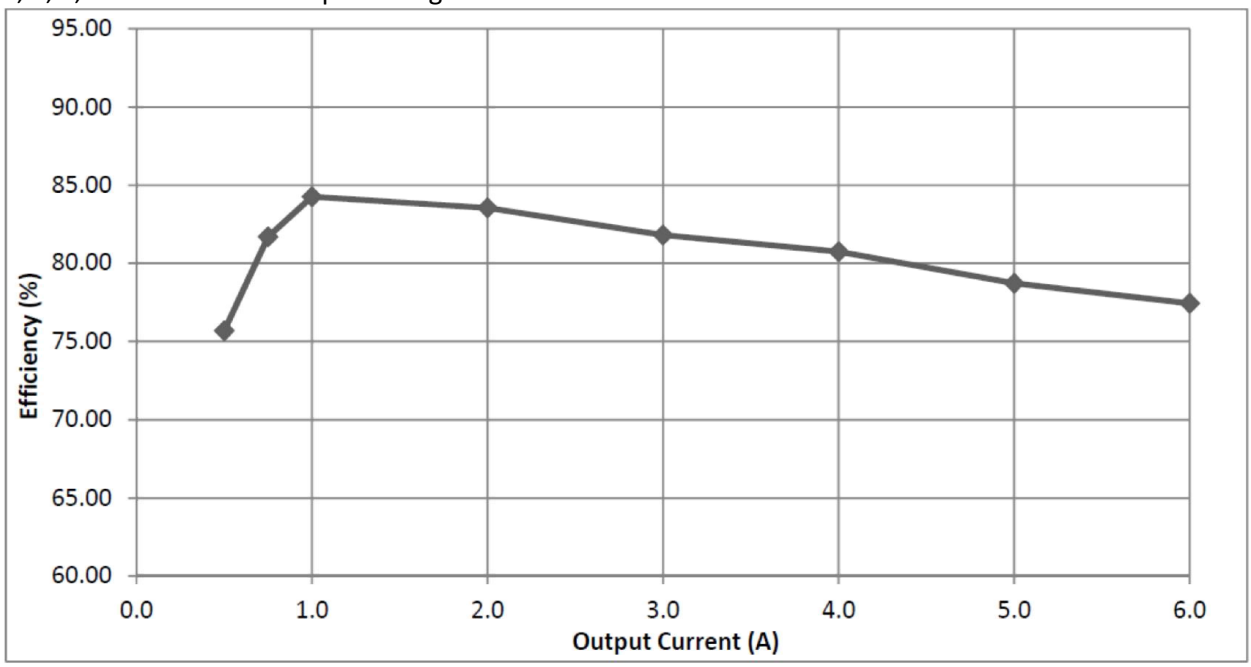



Figure 5: 1.1V Output

| VIN (V) | IIN (A) | VOUT (V) | IOUT (A) | PIN (W) | POUT (W) | Eff (%) |
|---|---|---|---|---|---|---|
| 12.01 | 0.06 | 1.11 | 0.5 | 0.734 | 0.556 | 75.68 |
| 12.00 | 0.09 | 1.11 | 0.8 | 1.020 | 0.833 | 81.69 |
| 11.99 | 0.11 | 1.11 | 1.0 | 1.319 | 1.111 | 84.27 |
| 11.98 | 0.22 | 1.11 | 2.0 | 2.660 | 2.222 | 83.55 |
| 11.98 | 0.34 | 1.11 | 3.0 | 4.073 | 3.332 | 81.80 |
| 11.96 | 0.46 | 1.11 | 4.0 | 5.502 | 4.441 | 80.73 |
| 11.95 | 0.59 | 1.11 | 5.0 | 7.051 | 5.550 | 78.71 |
| 11.94 | 0.72 | 1.11 | 6.0 | 8.597 | 6.656 | 77.43 |

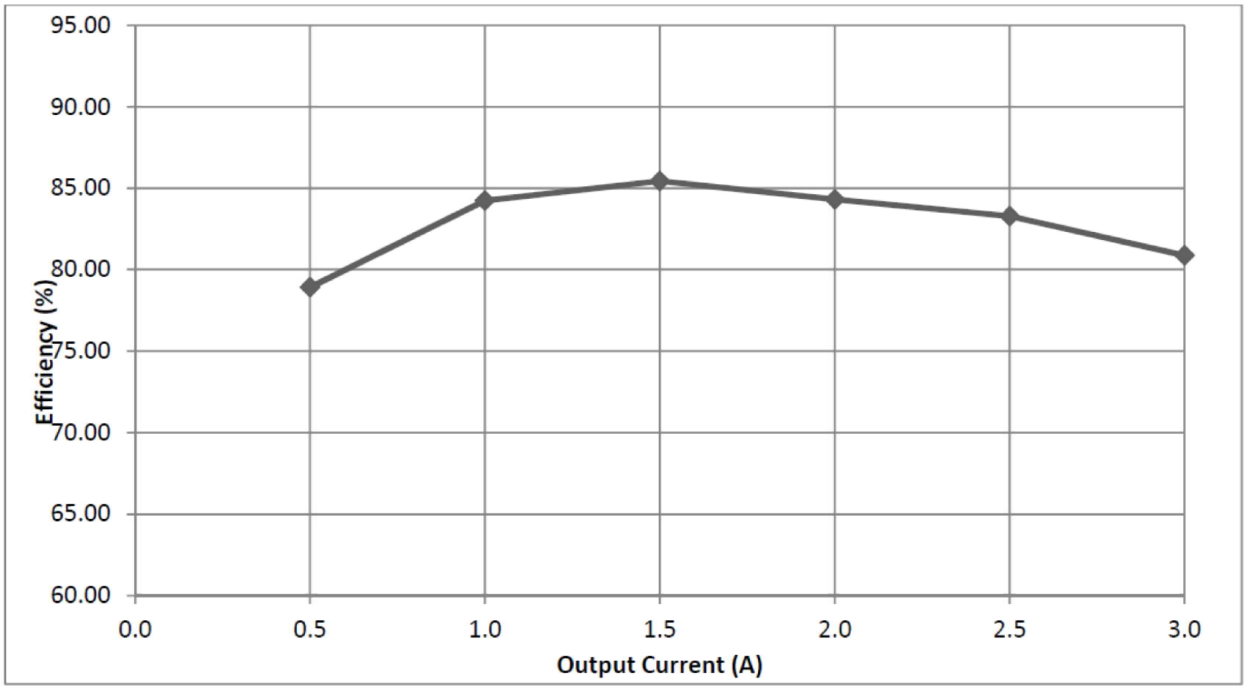



Figure 6: 1.5V Output

| VIN (V) | IIN (A) | VOUT (V) | IOUT (A) | PIN (W) | POUT (W) | Eff (%) |
|---|---|---|---|---|---|---|
| 12.00 | 0.08 | 1.52 | 0.5 | 0.960 | 0.758 | 78.91 |
| 11.99 | 0.15 | 1.52 | 1.0 | 1.799 | 1.515 | 84.24 |
| 11.98 | 0.22 | 1.52 | 1.5 | 2.660 | 2.273 | 85.45 |
| 11.98 | 0.30 | 1.52 | 2.0 | 3.594 | 3.030 | 84.31 |
| 11.97 | 0.38 | 1.52 | 2.5 | 4.549 | 3.788 | 83.27 |
| 11.96 | 0.47 | 1.52 | 3.0 | 5.621 | 4.545 | 80.85 |

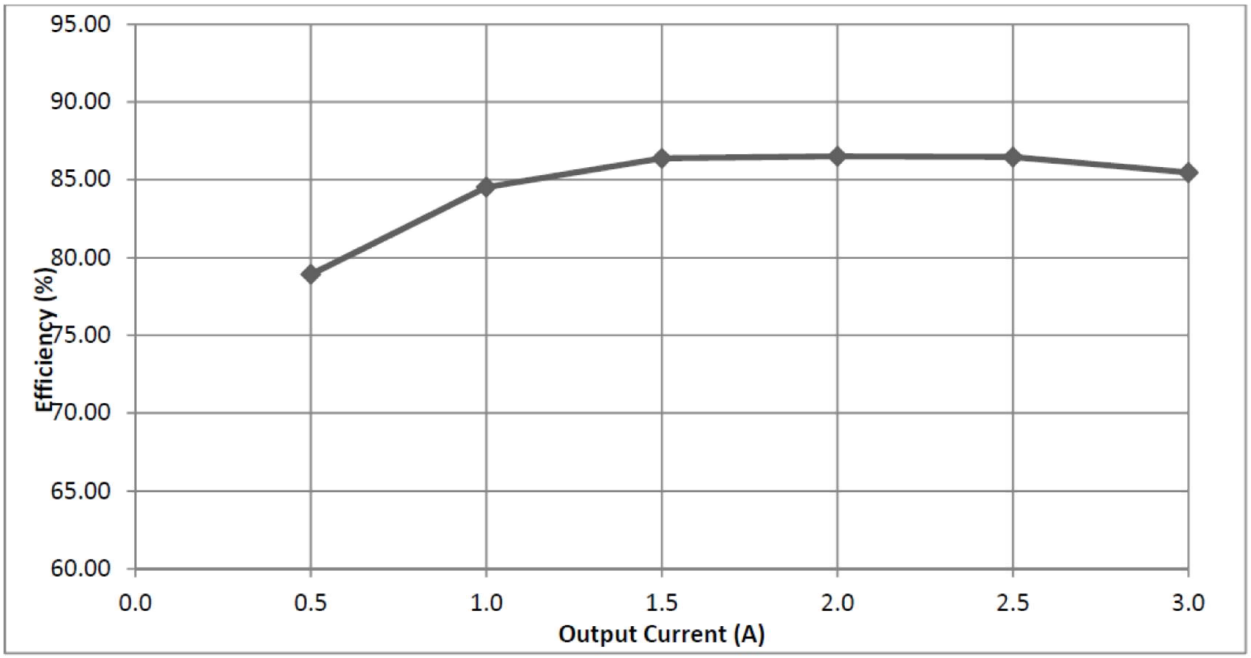



Figure 7: 3.3V Output

| VIN (V) | IIN (A) | VOUT (V) | IOUT (A) | PIN (W) | POUT (W) | Eff (%) |
|---|---|---|---|---|---|---|
| 11.99 | 0.18 | 3.41 | 0.5 | 2.158 | 1.704 | 78.93 |
| 11.98 | 0.34 | 3.39 | 1.0 | 4.013 | 3.392 | 84.52 |
| 11.97 | 0.49 | 3.38 | 1.5 | 5.865 | 5.066 | 86.36 |
| 11.96 | 0.65 | 3.36 | 2.0 | 7.774 | 6.724 | 86.49 |
| 11.95 | 0.81 | 3.35 | 2.5 | 9.680 | 8.368 | 86.45 |
| 11.94 | 0.98 | 3.33 | 3.0 | 11.701 | 9.999 | 85.45 |

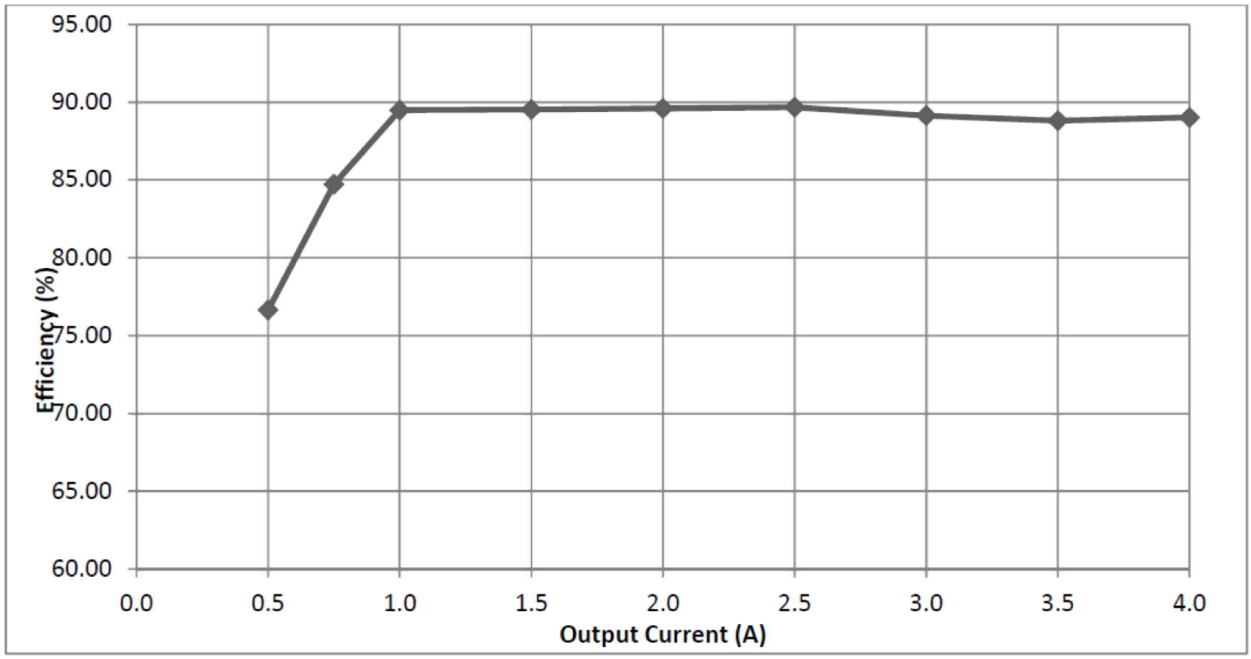



Figure 8: 2.5V Output

| VIN (V) | IIN (A) | VOUT (V) | IOUT (A) | PIN (W) | POUT (W) | Eff (%) |
|---|---|---|---|---|---|---|
| 11.99 | 0.14 | 2.57 | 0.5 | 1.679 | 1.287 | 76.64 |
| 11.99 | 0.19 | 2.57 | 0.8 | 2.278 | 1.930 | 84.71 |
| 11.98 | 0.24 | 2.57 | 1.0 | 2.875 | 2.573 | 89.49 |
| 11.97 | 0.36 | 2.57 | 1.5 | 4.309 | 3.858 | 89.53 |
| 11.96 | 0.48 | 2.57 | 2.0 | 5.741 | 5.144 | 89.60 |
| 11.95 | 0.60 | 2.57 | 2.5 | 7.170 | 6.430 | 89.68 |
| 11.94 | 0.73 | 2.57 | 3.0 | 8.657 | 7.716 | 89.14 |
| 11.92 | 0.85 | 2.57 | 3.5 | 10.132 | 8.999 | 88.81 |
| 11.91 | 0.97 | 2.57 | 4.0 | 11.553 | 10.284 | 89.02 |

# 6. Load Step

The load regulation of the 1.1V output is shown in Figures 9 and 10 below. The input voltage is 12V. The load step increases from 3A to 6A.

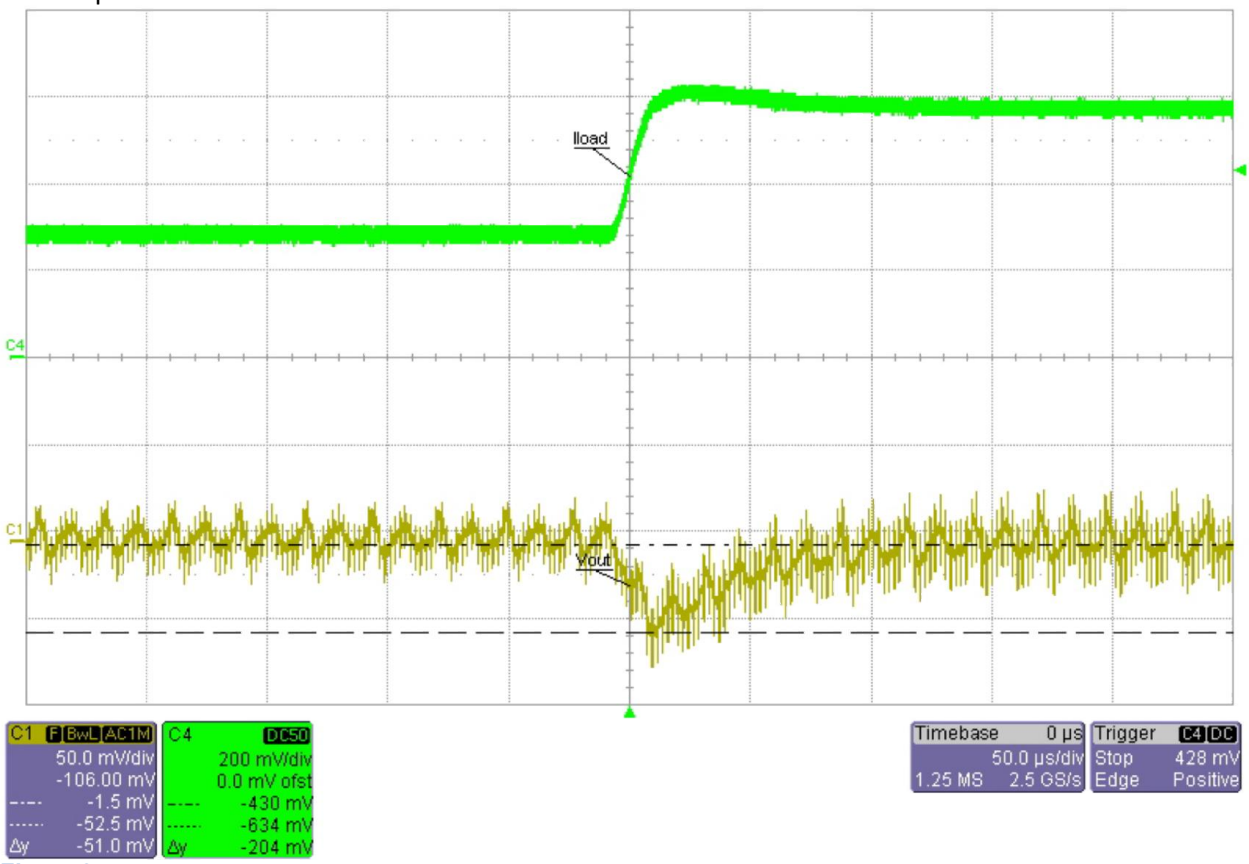



**Figure 9**

*Ch1 => AC coupled output voltage*
*Ch2 => Output current 1V = 10A*
*Slope of step: 3A/16.6µs*

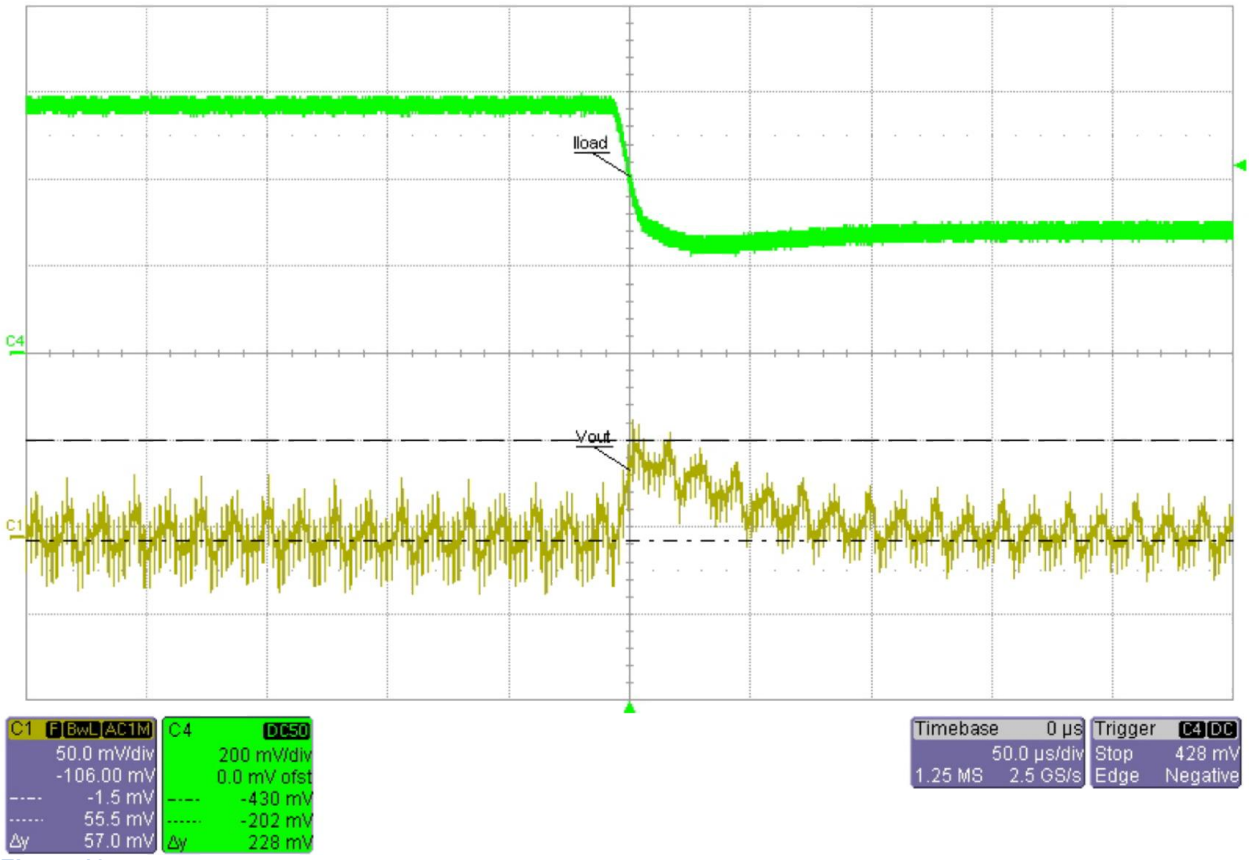



**Figure 10**

*Ch1 => AC coupled output voltage*
*Ch2 => Output current 1V = 10A*
*Slope of step: 3A/11µs*

The load regulation of the 1.5V output is shown in Figures 11 and 12 below. The input voltage is 12V. The load step increases from 1.5A to 3A.

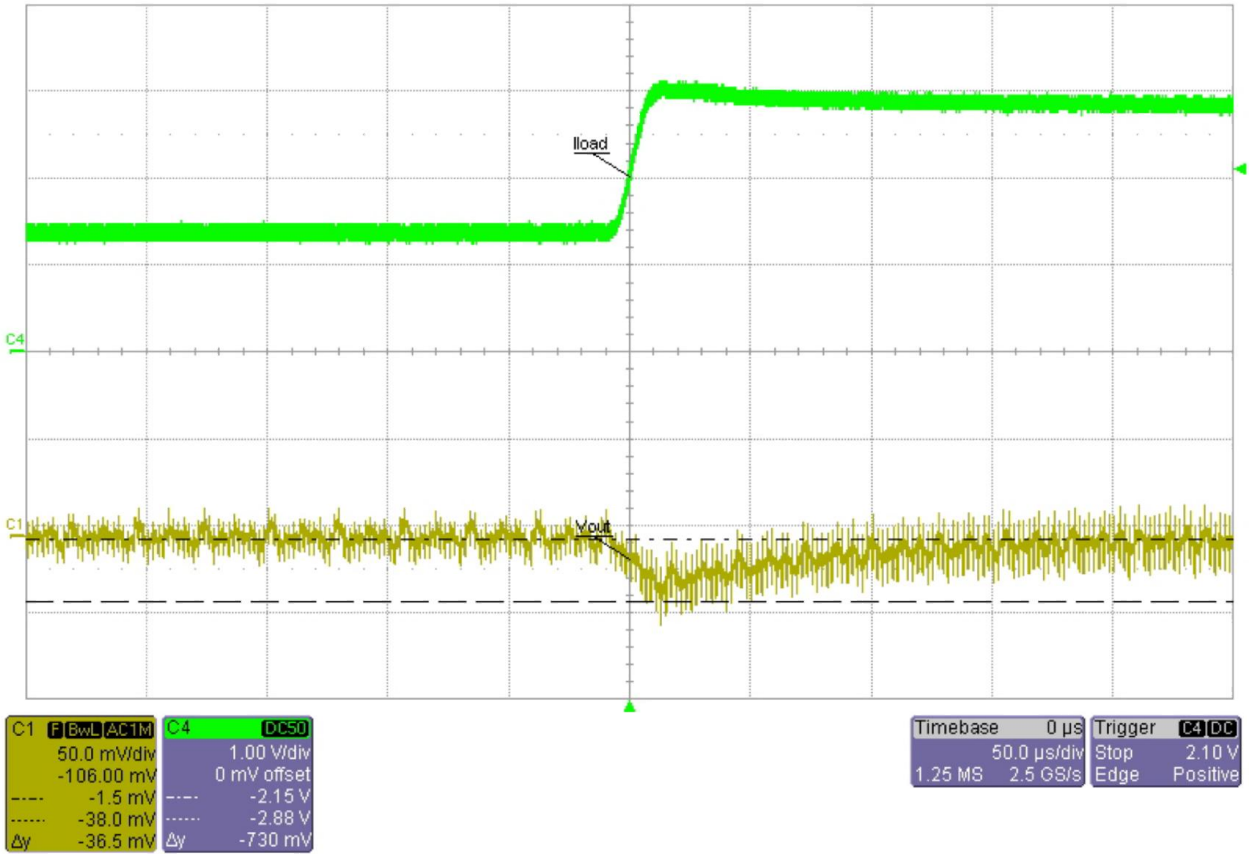



**Figure 11**

*Ch1 => AC coupled output voltage*
*Ch2 => Output current 1V = 10A*
*Slope of step: 1.5A/16.3µs*

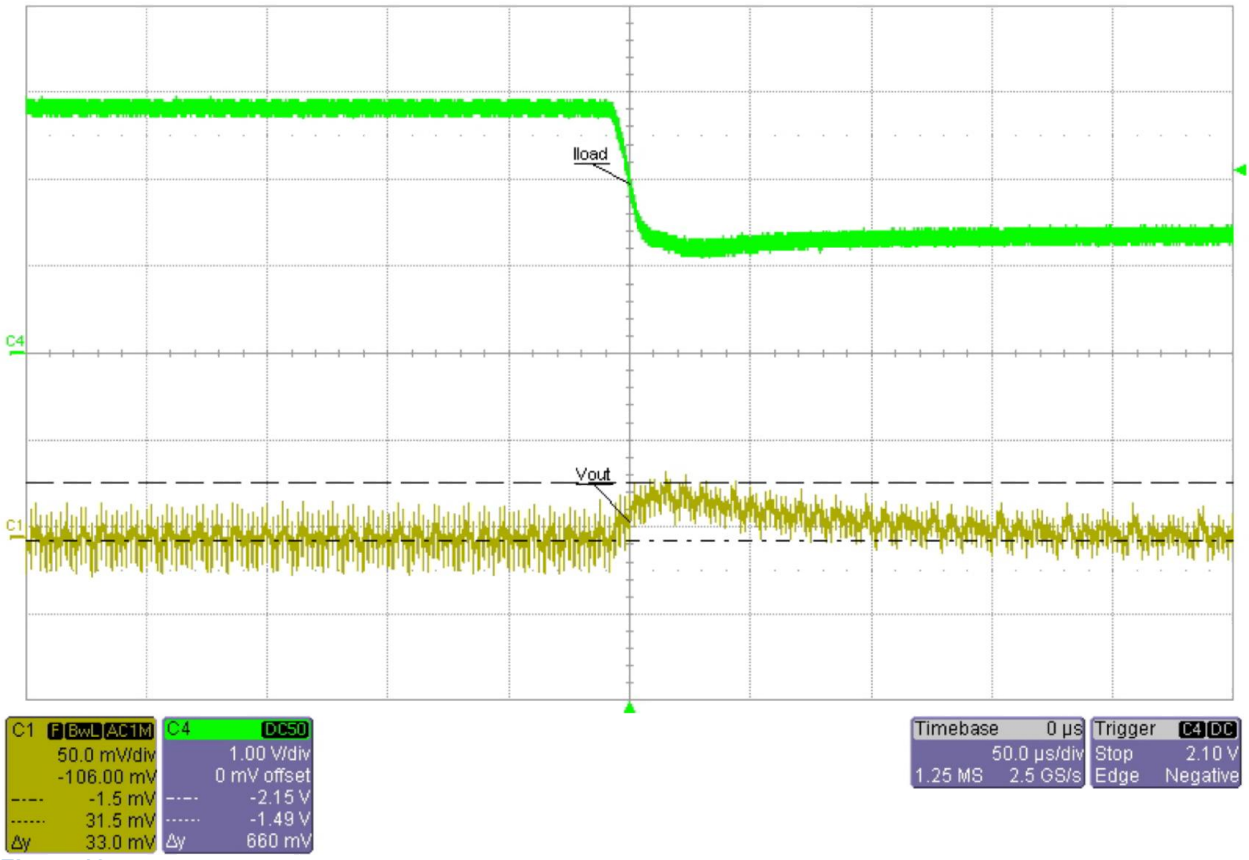



**Figure 12**

*Ch1 => AC coupled output voltage*
*Ch2 => Output current 1V = 10A*
*Slope of step: 1.5A/13.7µs*

The load regulation of the 3.3V output is shown in Figures 13 and 14 below. The input voltage is 12V. The load step increases from 1.25A to 2.5A.

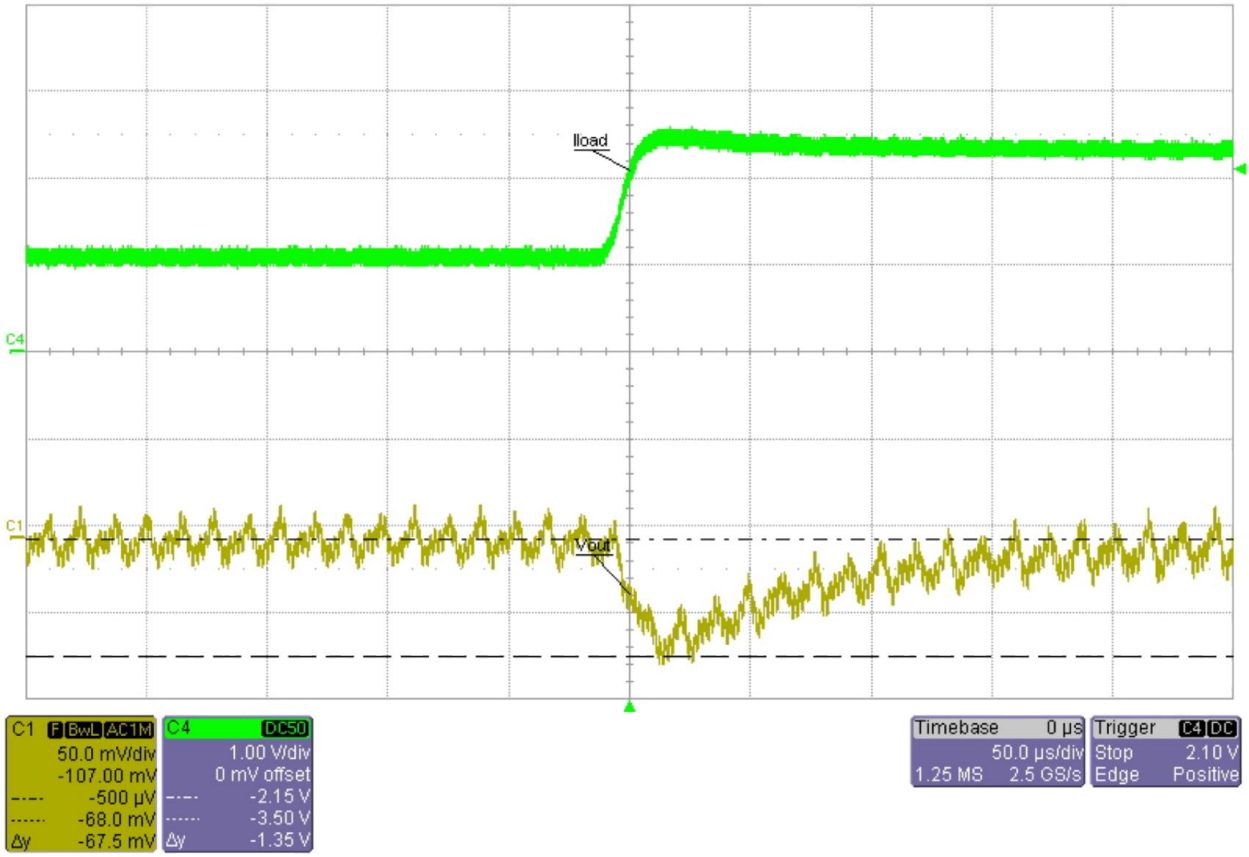



**Figure 13**

Ch1 => AC coupled output voltage
Ch2 => Output current 1V = 10A
Slope of step: 1.25A/17.1µs

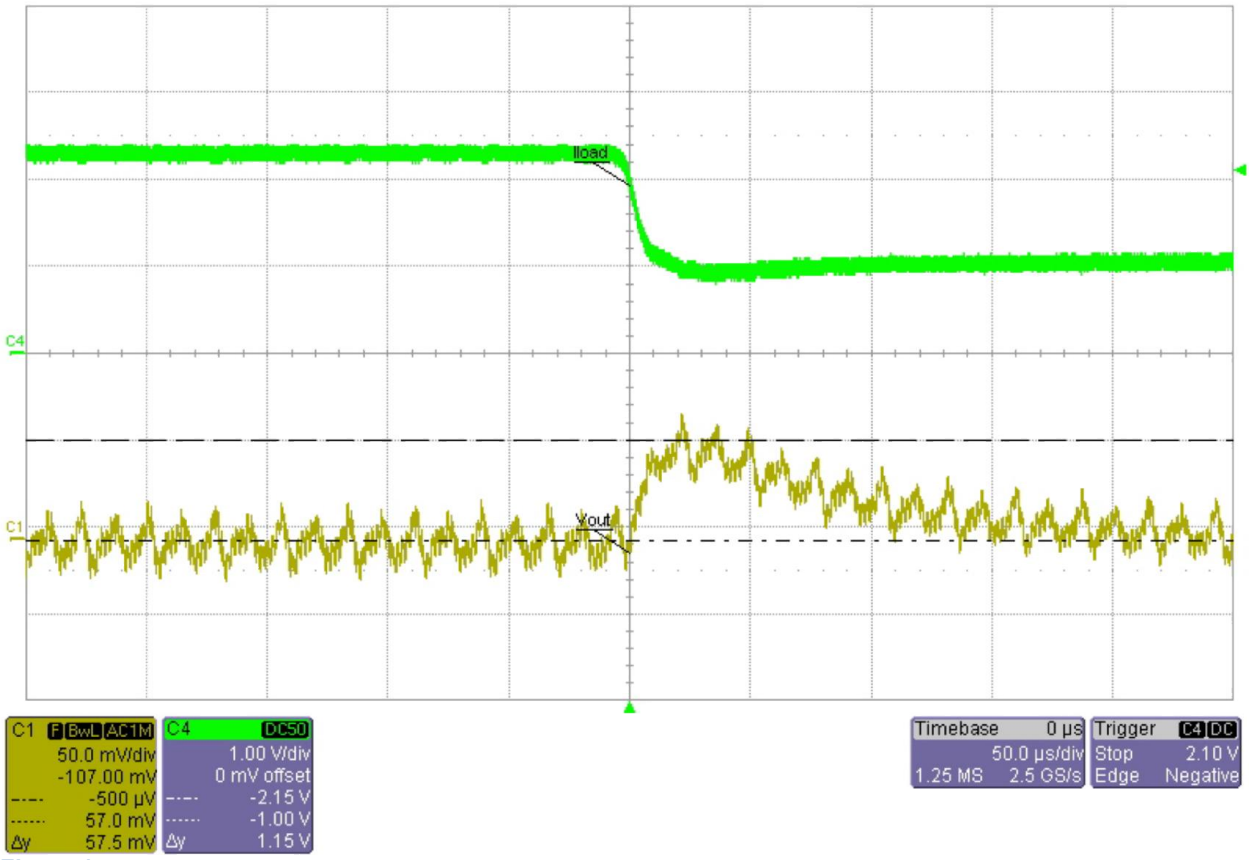



**Figure 14**

Ch1 => AC coupled output voltage

Ch2 => Output current 1V = 10A

Slope of step: 1.25A/13.3µs

The load regulation of the 2.5V output is shown in the Figures 15 and 16 below. The input voltage is 12V. The load step increases from 1.75A to 3.5A.

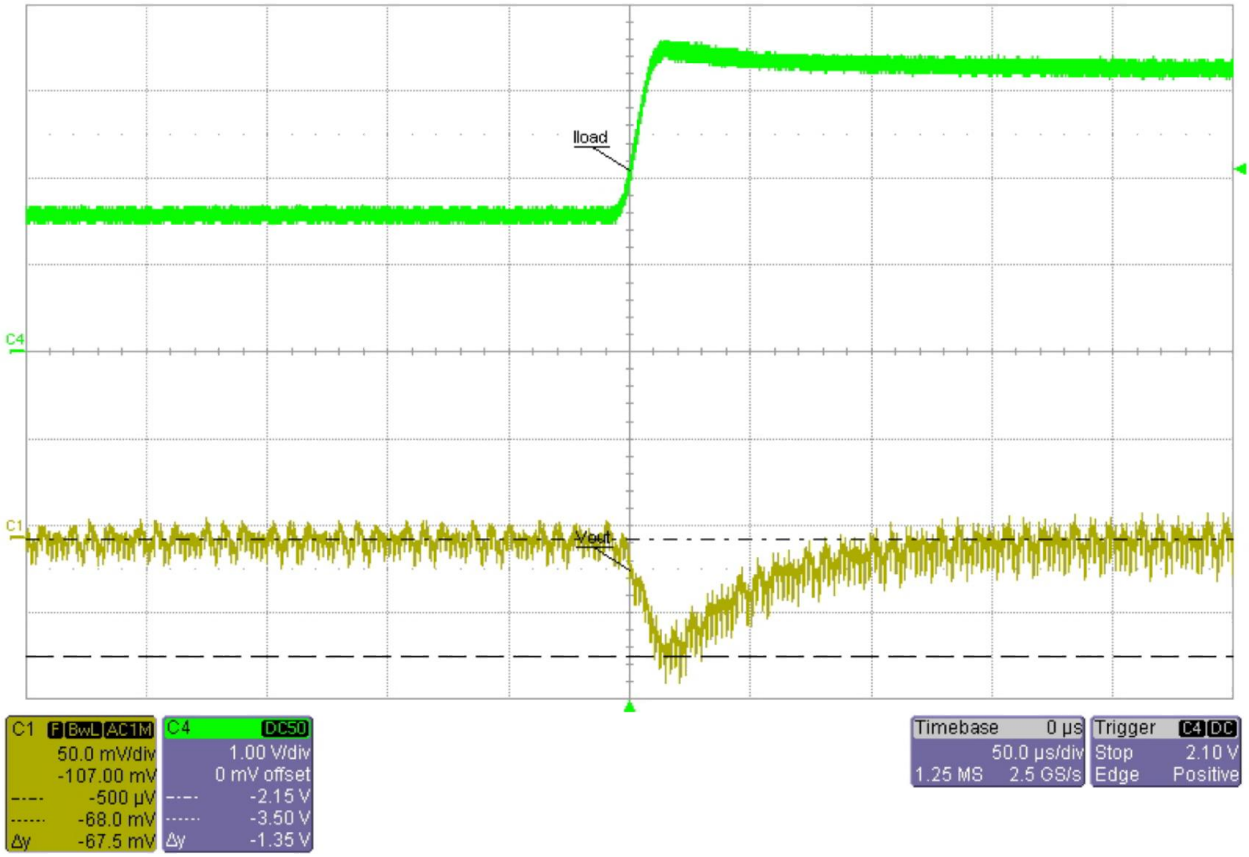



**Figure 15**

Ch1 => AC coupled output voltage
Ch2 => Output current 1V= 10A
Slope of step: 1.75A/15.8µs

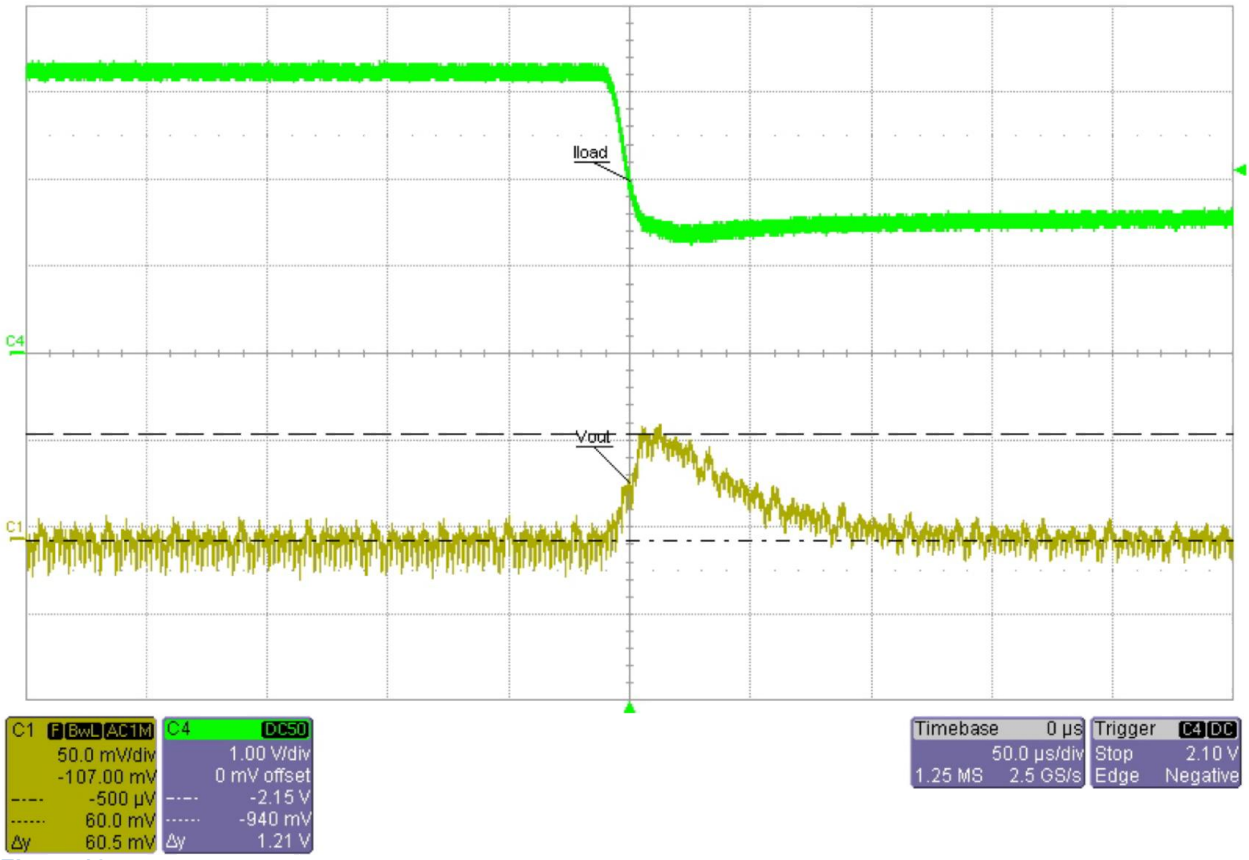



**Figure 16**

Ch1 => AC coupled output voltage

Ch2 => Output current 1V = 10A

Slope of step: 1.75A/14.2µs

The load regulation of the 2.5V LDO output is shown in the Figures 17 and 18 below. The input voltage is 12V. The load step increases from 0A to 1A.

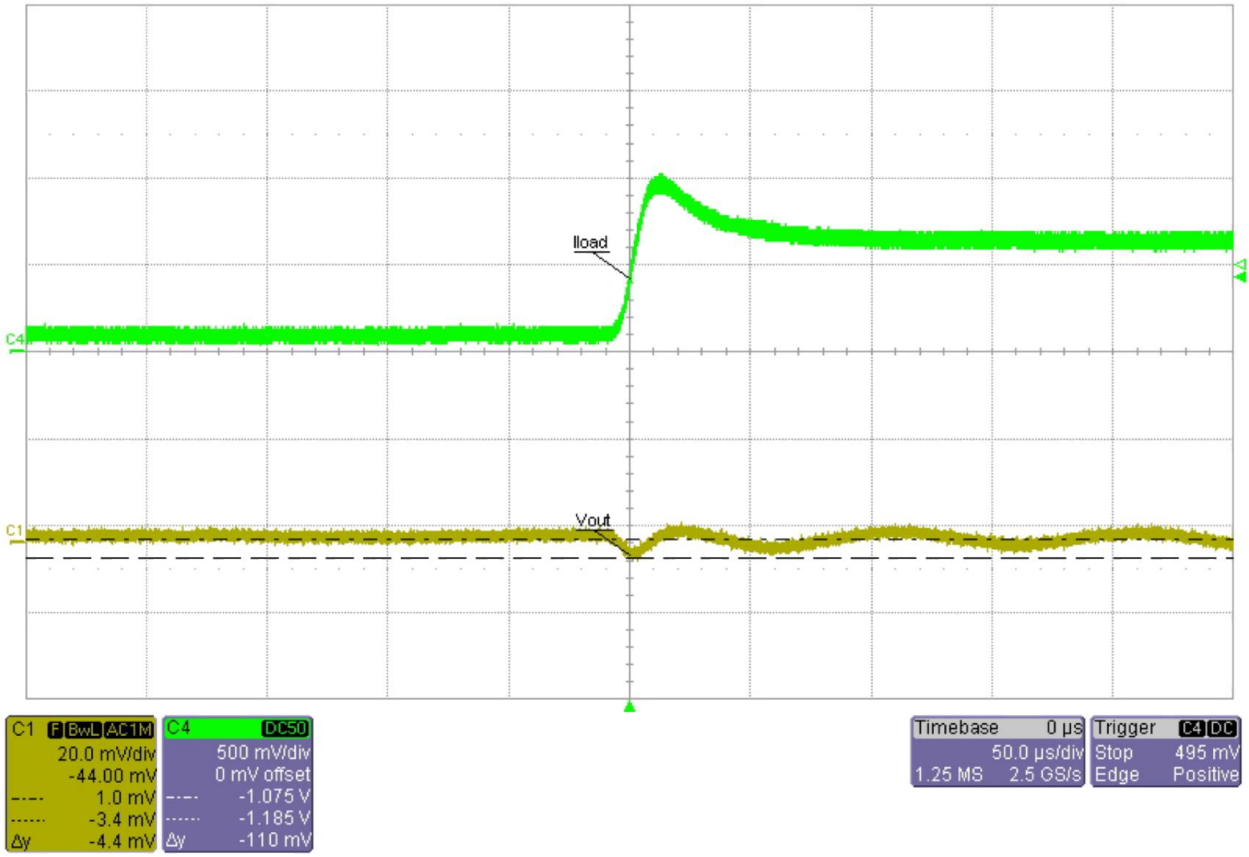



**Figure 17**

Ch1 => AC coupled output voltage
Ch2 => Output current 1V= 10A
Slope of step: 1A/17µs

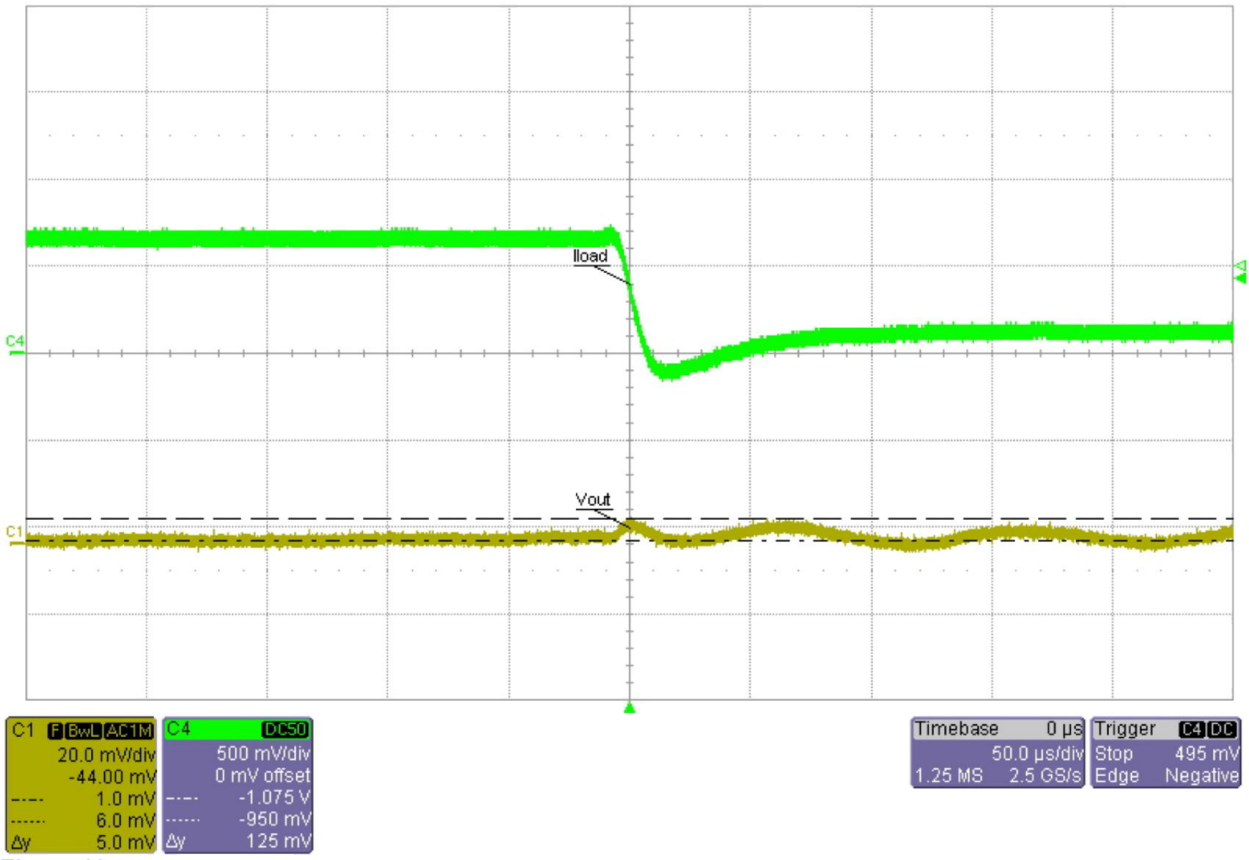



**Figure 18**

Ch1 => AC coupled output voltage

Ch2 => Output current 1V = 10A

Slope of step: 1A/17µs

# 7. Frequency Response

Figure 19 shows the loop response of the 1.1V output with 2A load and 12V input.

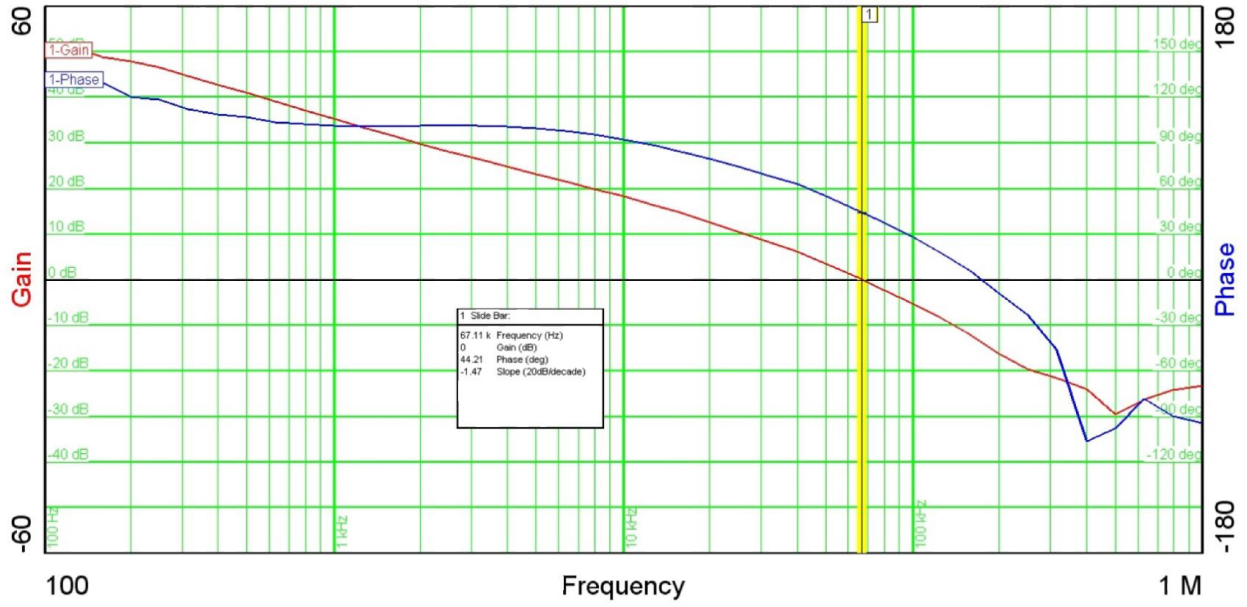



Figure 19

Table 1 summarizes the results from Figure 19.

| | |
|---|---|
| **Bandwidth (kHz)** | 67.11 |
| **Phase Margin** | 44.21° |
| **Slope (20dB/Decade)** | -1.47 |

Table 1

Figure 20 shows the loop response of the 1.5V output with 2A load and 12V input.

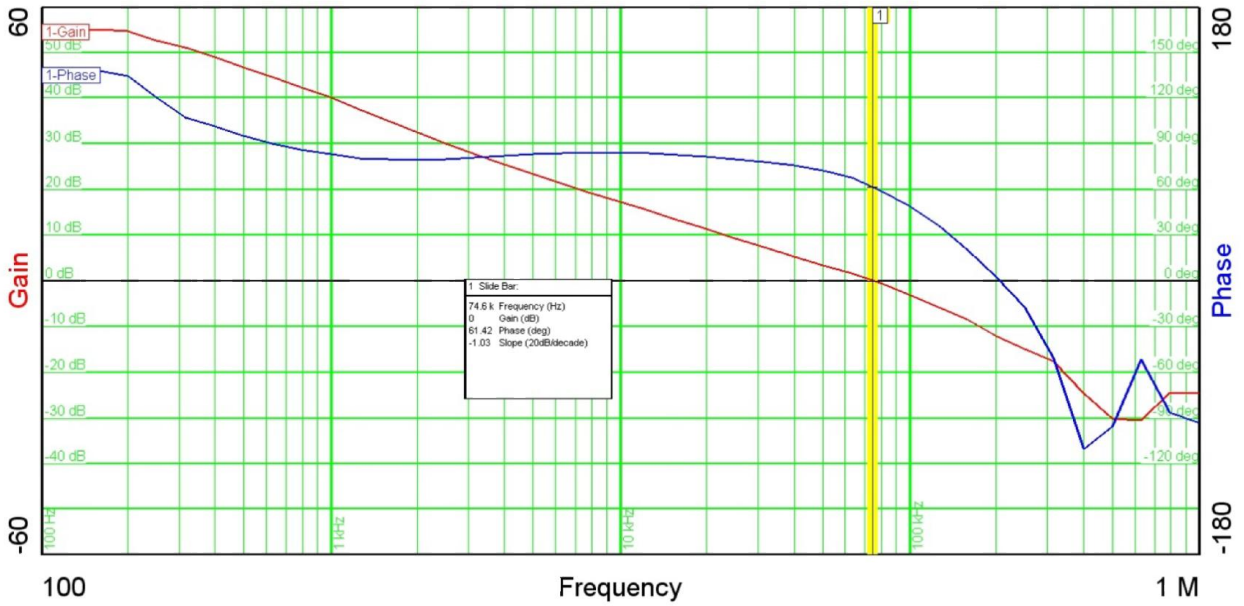



Figure 20

Table 2 summarizes the results from Figure 20.

| | |
|---|---|
| **Bandwidth (kHz)** | 75.6 |
| **Phase Margin** | 61.42° |
| **Slope (20dB/Decade)** | -1.03 |

Table 2

Figure 21 shows the loop response of the 3.3V output with 2A load and 12V input.

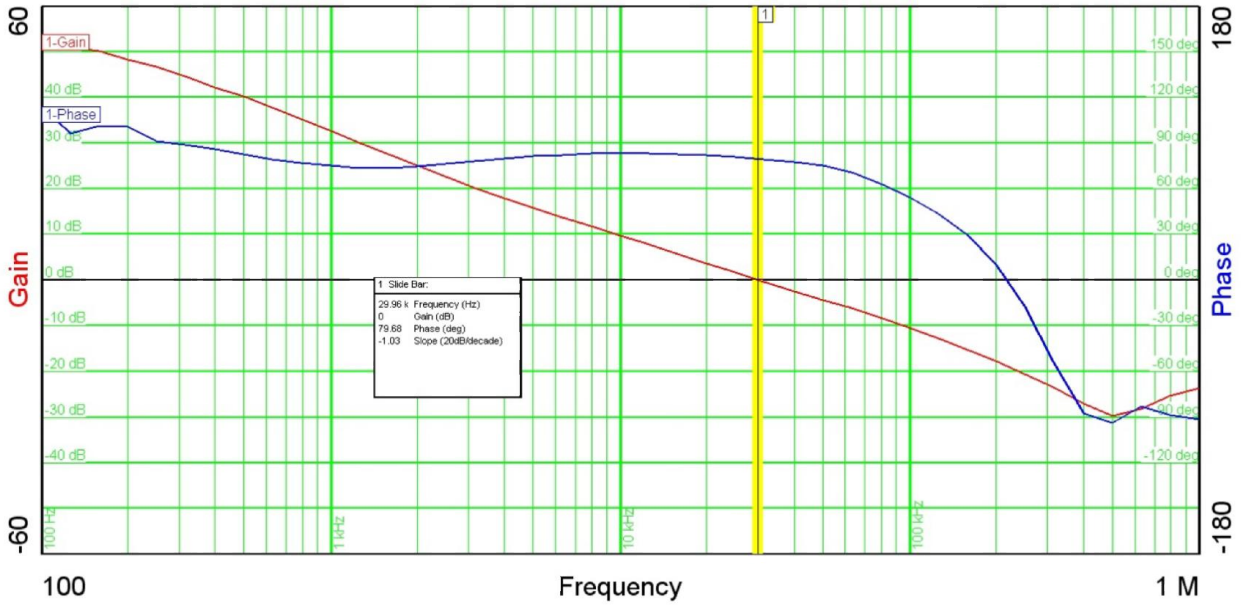



Figure 21

Table 3 summarizes the results from Figure 21.

| | |
|---|---|
| **Bandwidth (kHz)** | 29.96 |
| **Phase Margin** | 79.68° |
| **Slope (20dB/Decade)** | -1.03 |

Table 3

Figure 22 shows the loop response of the 2.5V output with 2A load and 12V input.

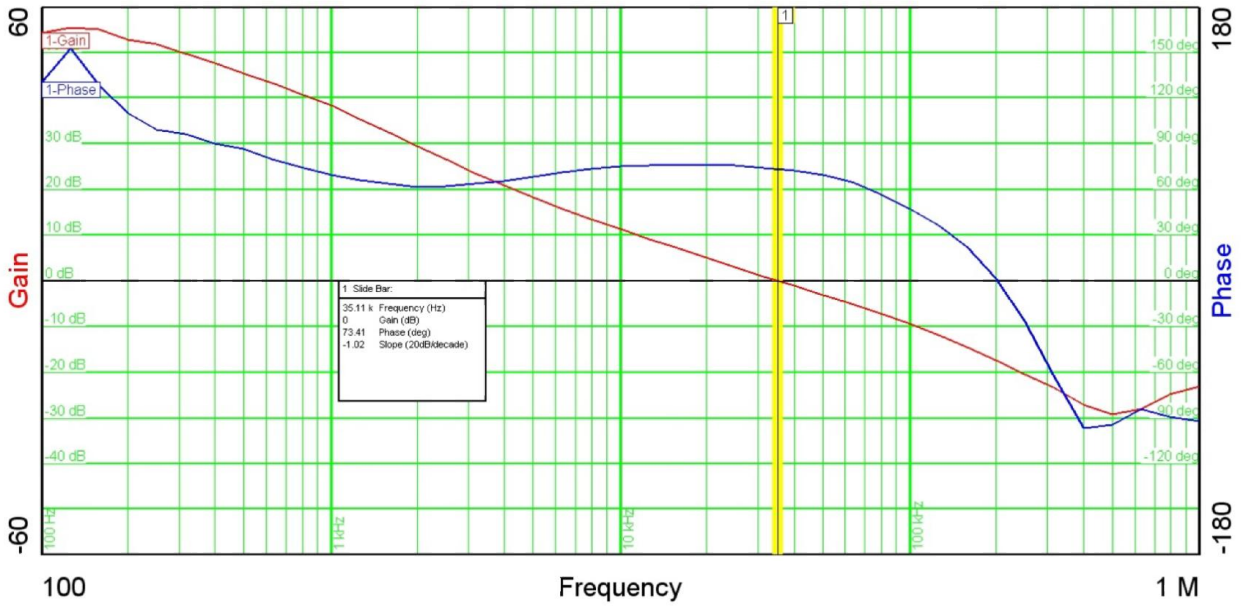



Figure 22

Table 4 summarizes the results from Figure 22.

| | |
|---|---|
| **Bandwidth (kHz)** | 35.11 |
| **Phase Margin** | 73.41° |
| **Slope (20dB/Decade)** | -1.02 |

Table 4

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