User's Guide

TPS54J06x Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the BSR067 evaluation module (EVM) as well as for the TPS54J060 and TPS54J061 DC/DC converters. Also included are the performance specifications, the schematic, and the list of materials for the TPS54J060EVM-067 and TPS54J061EVM-067.

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1 Introduction

The TPS54J060 and TPS54J061 are D-CAP3™ synchronous buck converters designed for 6-A output current. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the device. The high-side and low-side switching MOSFETs are integrated in the device package along with their gate drive circuitry. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

1.1 Background

The EVM is setup to allow the user to see the performance of the TPS54J060 and TPS54J061 devices and easily make changes to multiple settings. The low drain-to-source on resistance of the MOSFETs allows the device to achieve high efficiencies and helps keep the junction temperature low at high output currents. There is no need for external compensation components since this device is designed with D-CAP3™ control topology. On the EVM the switching frequency and the operation mode are externally selectable using a jumper to set the resistor from the MODE pin to AGND. An external resistor divider allows for an adjustable output voltage. Additionally, the device provides adjustable soft start, adjustable OC limit threshold, external reference input, and an open-drain power good indicator. Lastly the device has a fixed internal VIN under voltage lockout and externally adjustable UVLO using a resistor divider at the EN pin.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54J060EVM-067	V_{IN} = 4 V to 16 V	0 A to 6 A
TPS54J061EVM-067	V_{IN} = 4 V to 16 V	0 A to 6 A

1.2 Performance Specification Summary

A summary of the TPS54J060EVM-067 and TPS54J061EVM-067 performance specifications is provided in Table 1-2. Specifications are given for an ambient temperature of 25°C, input voltage of V_{IN} = 12 V, internal VCC and an output voltage of 1.8V, unless otherwise noted. The TPS54J060EVM-067 and TPS54J061EVM-067 are designed for V_{IN} = 8 V to 16 V, however, operation with a lower input voltage is possible by modifying the adjustable under voltage lockout (UVLO) or by forcing the EN pin above its turn on threshold.

Table 1-2. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} voltage range			8	12	16	V
V_{IN} turn on voltage	R2 = 499 kΩ, R5 = 100 kΩ			7.4		V
V_{IN} turn off voltage	R2 = 499 kΩ, R5 = 100 kΩ			6.2		V
V_{IN} input current	FCCM, V_{IN} = 12 V, I_O = 0 A			10.2		mA
	DCM, V_{IN} = 12 V, I_O = 0 A, Internal VCC			1.1		mA
	V_{IN} = 8 V, I_O = 6 A			1.48		A
Output voltage				1.8		V
Output current range	V_{IN} = 4 V to 16 V		0		6	A
Load and line regulation	V_{IN} = 4 V to 16 V, I_O = 6 A			+/– 0.1%		
Load transient response	I_O = 0.1 A to 3.1 A , 1 A/µs	Voltage change		20		mV
		Recovery time		<10		µs
	I_O = 0.1 A to 3.1 A , 1 A/µs	Voltage change		20		mV
		Recovery time		<10		µs
Loop Bandwidth	V_{IN} = 12 V, I_O = 3 A CC			103		kHz
Phase Margin	V_{IN} = 12 V, I_O = 3 A CC			72.6		degree
Input voltage ripple	V_{IN} = 12 V, I_O = 6 A			90		mV_{PP}
Output voltage ripple	V_{IN} = 12 V, I_O = 6 A			5		mV_{PP}
IC case temperature	V_{IN} = 12 V, I_O = 6 A			52		°C
Soft start time	TPS54J060, C_{SS} = 22 nF			2		ms
Soft start time	TPS54J061, C_{SS} = 22 nF			1.5		ms
Switching frequency	MODE pin short to VCC or short to AGND			1100		kHz
Valley current limit	R_{TRIP} = 4.99 kΩ			6		A

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54J060 and TPS54J061. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage is set by a resistor divider network of R3 and R7. Keeping R7 fixed and change the output voltage of the EVM by changing the value of resistor R3. Changing the value of R3 will change the output voltage above the reference voltage V_{INTREF}.

The value of R3 for a specific output voltage can be calculated using Equation 1

$$R_{FB\_HS} = \frac{V_O - V_{INTREF}}{V_{INTREF}} \times R_{FB\_LS} \quad (1)$$

V_{INTREF}= 0.9 V for TPS54J060

V_{INTREF}= 0.6 V for TPS54J061

R_{FB_HS} = R3

R_{FB_LS} = R7

1.3.2 Frequency and Operation Mode Setting

To change the frequency and operation mode of the part, the MODE pin is used. J4 and the surrounding circuitry allows for an easy change to the frequency and operation mode setting. All 6 options offered by J4 are shown in Table 1-3.

Default setting: Short to VCC 1.1MHz, DCM.

Table 1-3. Switching Frequency and Mode

Switching Frequency (f_{sw})	Operation Mode Under Light Load	Mode Pin Connections	
		Connection	Jumper Setting
1100 kHz	Skip Mode	Short to VCC	Short Pins 1 and 2
2000 kHz	Skip Mode	243 kΩ +/- 10% to AGND	Short Pins 3 and 4
600 kHz	Skip Mode	121 kΩ +/- 10% to AGND	Short Pins 5 and 6
600 kHz	Forced CCM	60.4 kΩ +/- 10% to AGND	Short Pins 7 and 8
2000 kHz	Forced CCM	30.1 kΩ +/- 10% to AGND	Short Pins 9 and 10
1100 kHz	Forced CCM	Short to AGND	Short Pins 11 and 12

1.3.3 Enable Pin Selection

The controller can be disabled by J3.

Default setting: J3 open connecting EN pin to VIN through resistor divider.

Table 1-4. Enable Pin Selection

Set On Connection	Enable Selection
Open	EN pin connected to VIN pin through resistor divider
Pins 1-2 Shorted	EN pin connected to PGND

1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using the resistor divider to the EN pin, R2 and R5. See the device datasheet to get detailed instructions for setting the external UVLO.

For operation below 8-V input, modify the resistor divider or use the EN pin test point to pull the EN pin above it's threshold with another voltage source.

2 Test Setup and Results

This section first describes how to properly connect, set up, and use the TPS54J060EVM-067 and TPS54J061EVM-067 . This section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transient, loop response, output ripple, start-up, and current limit.

Measurements are given for an ambient temperature of 25°C, input voltage of 12 V, and internal VCC unless otherwise noted.

2.1 Input/Output Connections

The TPS54J060EVM-067 and TPS54J061EVM-067 are provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 6 A must be connected to J1 through a pair of 20-AWG or higher wires. The load must be connected to J2 through a pair of 20-AWG or higher wires. The maximum load current capability is 6-A.

Wire lengths must be minimized to reduce losses in the wires. VIN_SNS+ provides a place to monitor the VIN input voltages with VIN_SNS- providing a convenient ground reference. VOUT is used to monitor the output voltage with PGND as the ground reference.

Table 2-1. Connections and Test Points

TEST POINTS	DESCRIPTION
J1	VIN, PGND (see Table 1-1 for input voltage range)
J2	VOUT, PGND: 5.5 V at 6-A maximum
J3	EN jumper (seeTable 1-4 for settings)
J4	MODE jumper (see Table 1-3 for settings)
VIN_SNS+, VIN_SNS-	VIN voltage sensing test points
VOUT, PGND	VOUT voltage sensing test points
VCC, PGND	VCC voltage sensing test points
PGOOD	PGOOD output test point
EN	EN test point
AGND	AGND test point
BODE+, BODE-	Loop measurement test points (BODE+ is at the same net as VOUT, but is closer to FB divider and IC)
MODE	MODE test point
SW	SW test point

2.2 Start Up Procedure

1. Make sure the EN jumper (J3) is open to connect the EN pin to the resistor divider from VIN.
2. (Optional) Apply appropriate external bias voltage on VCC and PGND test points. If no external bias, please go directly to step 3. The external bias range is 3.1 V to 3.6 V.
3. Apply appropriate VIN voltage to the VIN and PGND terminal J1.

2.3 Efficiency

The below images show the efficiency measured using the TPS54J061EVM-067. The TPS54J061EVM-067 will have slightly improved efficiency at very light loads with its higher resistance FB divider. Figure 2-1 through Figure 2-3 shows the efficiency in FCCM mode for different input voltages when using internal VCC and external 3.3-V VCC. Figure 2-4 through Figure 2-6 shows the improved light load efficiency in DCM mode with internal VCC and external 3.3-V VCC. Lastly, Figure 2-7 and Figure 2-8 shows the improved efficiency with the switching frequency reduced to 600 kHz with internal VCC in FCCM and DCM mode, respectively.

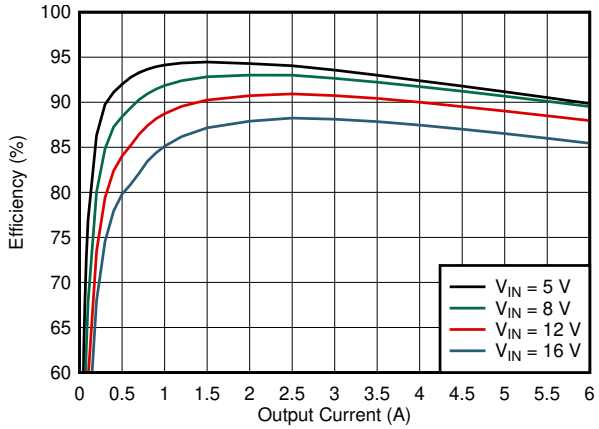

Figure 2-1. Efficiency – FCCM, Internal VCC, f_{SW} = 1100 kHz

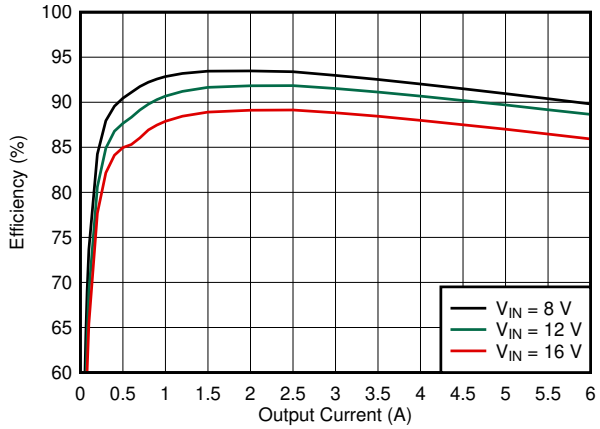

Figure 2-2. Efficiency – FCCM, External 3.3-V VCC, f_{SW} = 1100 kHz, R13 = 4.7 Ω

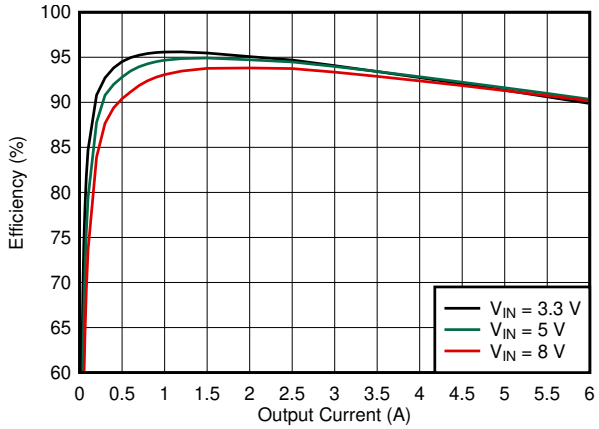

Figure 2-3. Efficiency – FCCM, External 3.3-V VCC, f_{SW} = 1100 kHz, R13 = 0 Ω

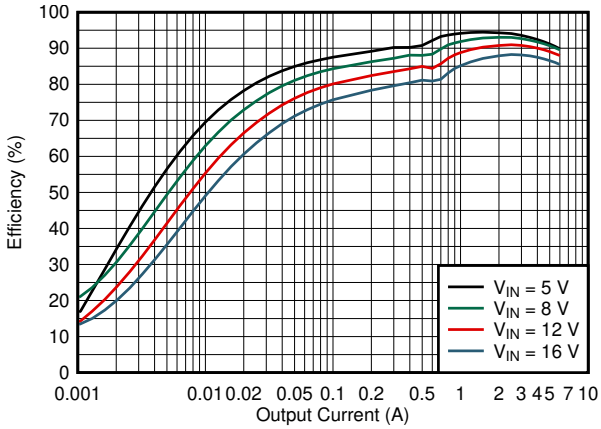

Figure 2-4. Efficiency – DCM, Internal VCC, f_{SW} = 1100 kHz

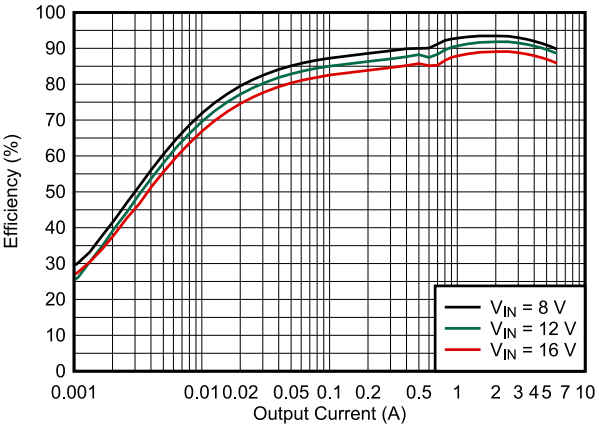

Figure 2-5. Efficiency – DCM, External 3.3-V VCC, f_{SW} = 1100 kHz, R13 = 4.7 Ω

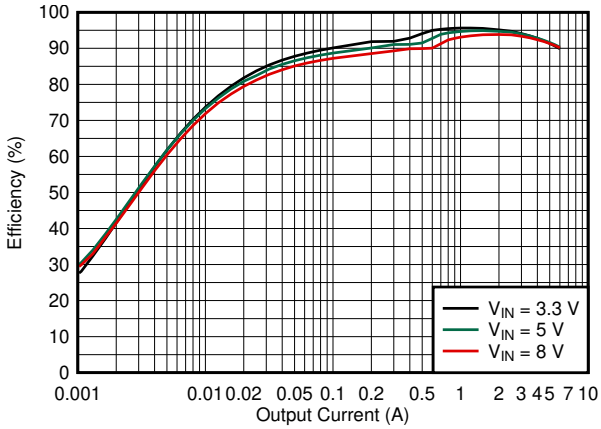

Figure 2-6. Efficiency – DCM, External 3.3-V VCC, f_{SW} = 1100 kHz, R13 = 0 Ω

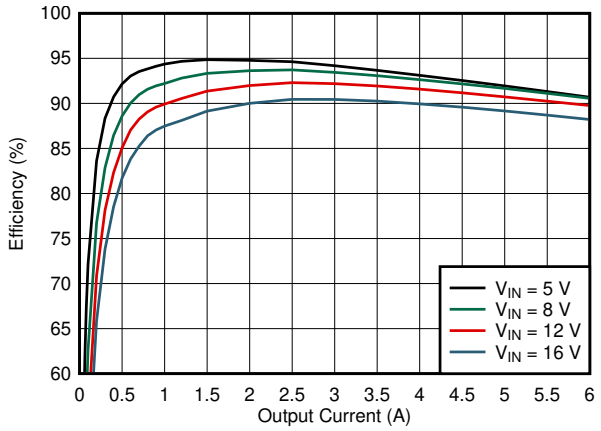

Figure 2-7. Efficiency – FCCM, Internal VCC, f_{SW} = 600 kHz

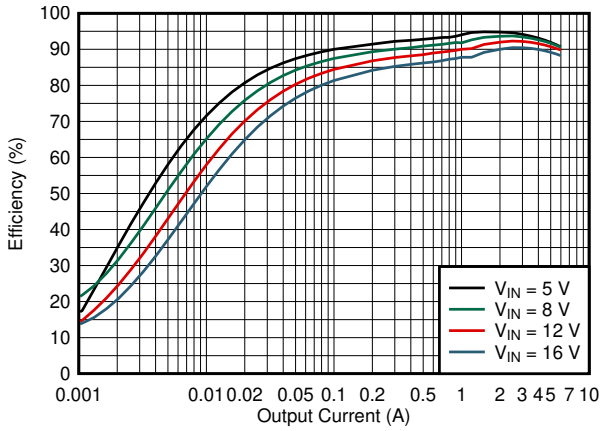

Figure 2-8. Efficiency – DCM, Internal VCC, f_{SW} = 600 kHz

2.4 Load and Line Regulation

Figure 2-9 and Figure 2-10 shows the load regulation measured on the TPS54J060EVM-067. The output voltage of the TPS54J061EVM-067 is only slightly higher at 1.81V typical due to the different feedback divider.

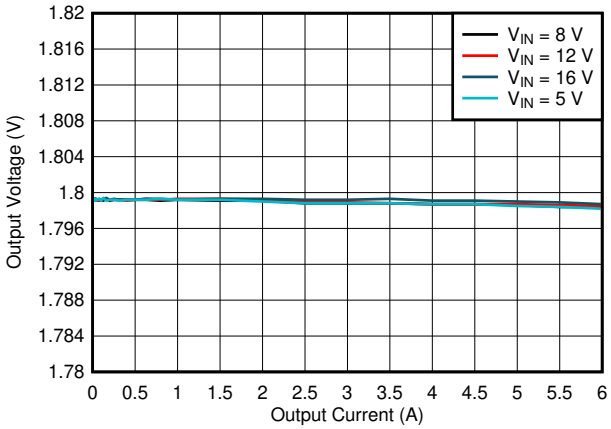

Figure 2-9. Load Regulation – FCCM

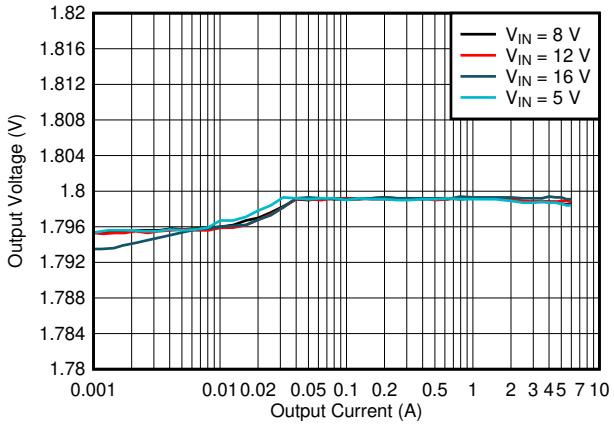

Figure 2-10. Load Regulation – DCM

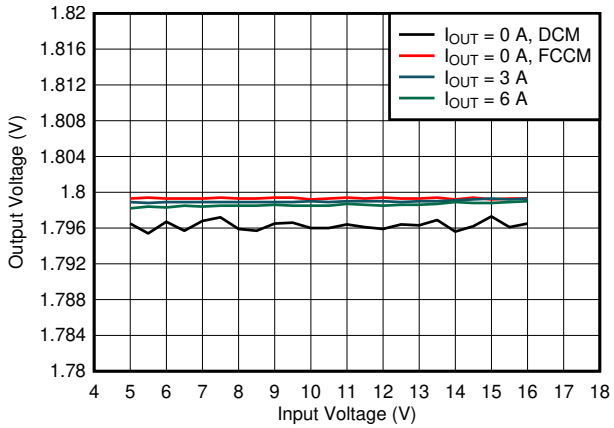

Figure 2-11. Line Regulation

2.5 Load Transients

Figure 2-12 and Figure 2-13 shows how the TPS54J060EVM-067 and TPS54J061EVM-067 responds to load transients in FCCM and DCM respectively. The current step is from 0.1 to 3.1 A load. The current step slew rate is 1 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

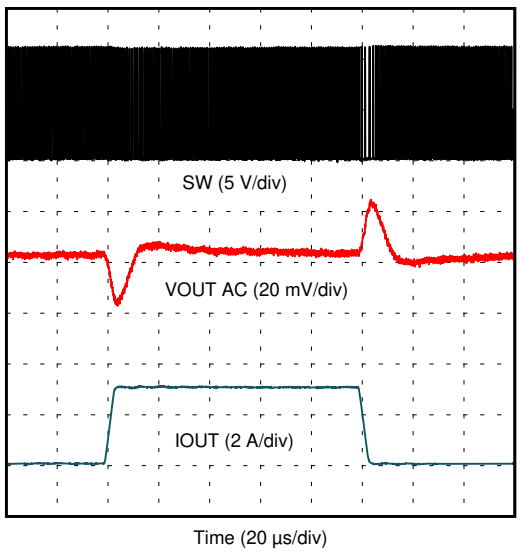

Figure 2-12. Load Transient Response – FCCM

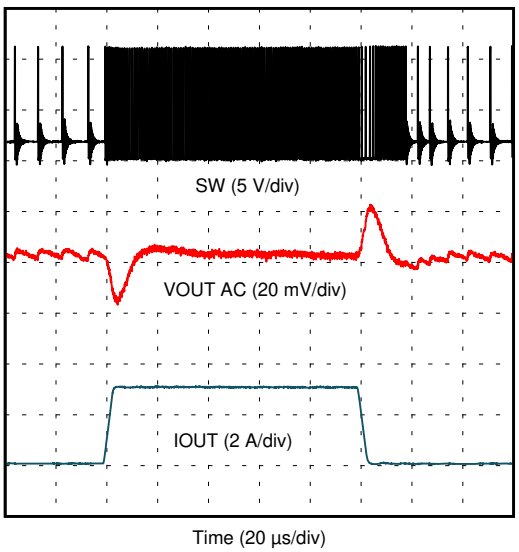

Figure 2-13. Load Transient Response – DCM

2.6 Loop Characteristics

Figure 2-14 shows the TPS54J060EVM-067 and TPS54J061EVM-067 frequency-response characteristics. Gain and phase plots are shown for input voltage of 12 V with 3 A constant current load.

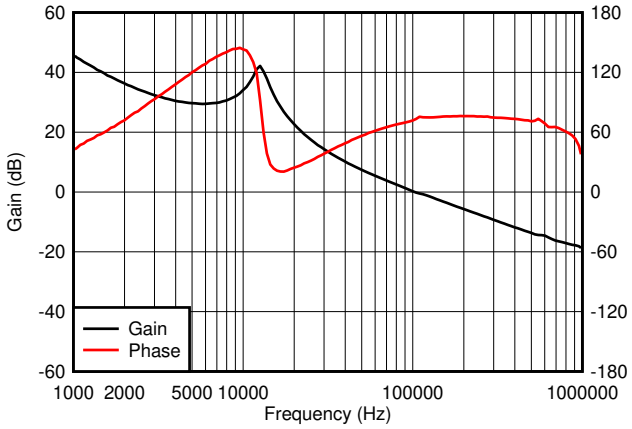

Figure 2-14. Bode Plot

2.7 Output Voltage Ripple

Figure 2-15, Figure 2-16, and Figure 2-17 show the TPS54J060EVM-067 and TPS54J061EVM-067 output voltage ripple for V_{IN} = 12 V. The ripple voltage is measured directly across the last ceramic output capacitor.

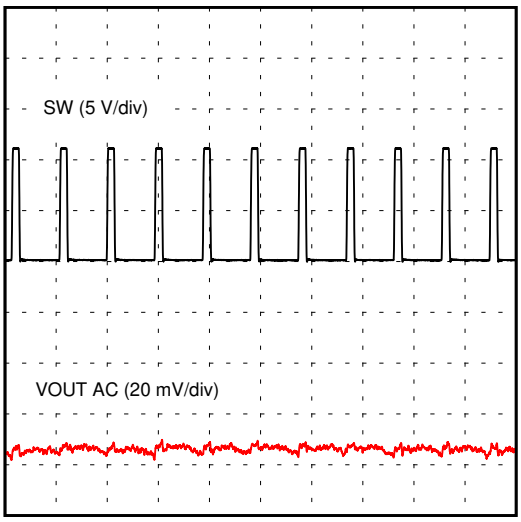

Figure 2-15. Output Ripple – FCCM, 0.1-A Load

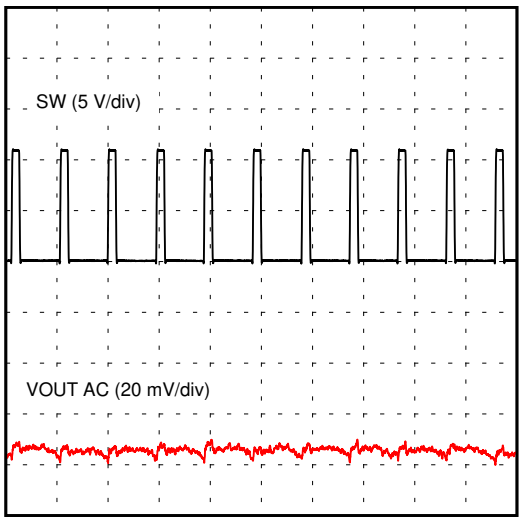

Figure 2-16. Output Ripple – FCCM, 6-A Load

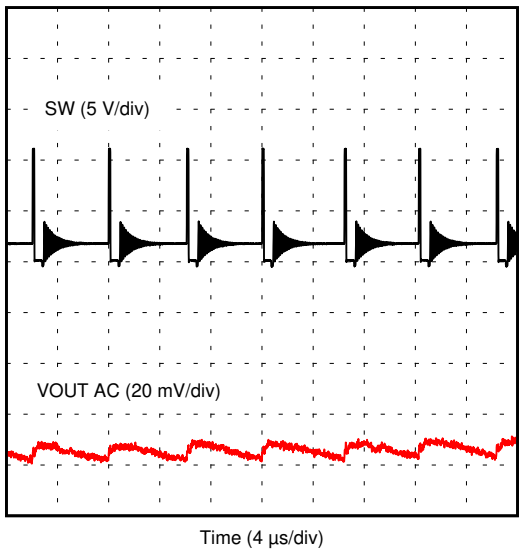

Figure 2-17. Output Ripple – DCM, 0.1-A Load

2.8 Input Voltage Ripple

Figure 2-18, Figure 2-19, and Figure 2-20 show the TPS54J060EVM-067 and TPS54J061EVM-067 input voltage ripple for V_{IN} = 12 V. The ripple voltage is measured directly across the ceramic input capacitor closest to the input terminal.

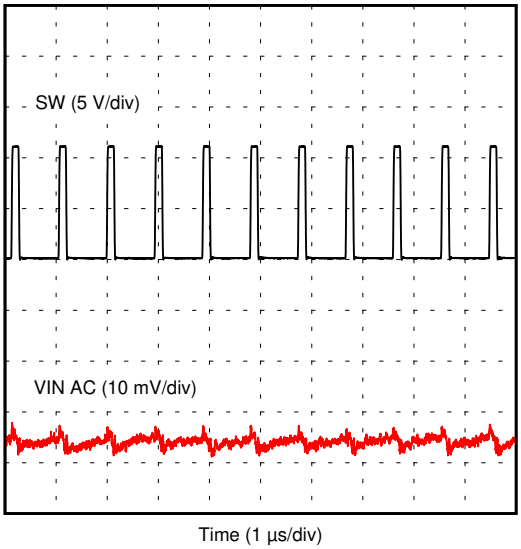

Figure 2-18. Input Ripple – FCCM, 0.1-A Load

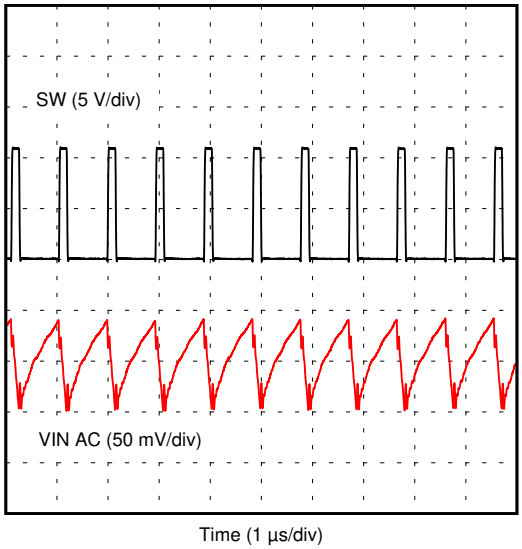

Figure 2-19. Input Ripple – FCCM, 6-A Load

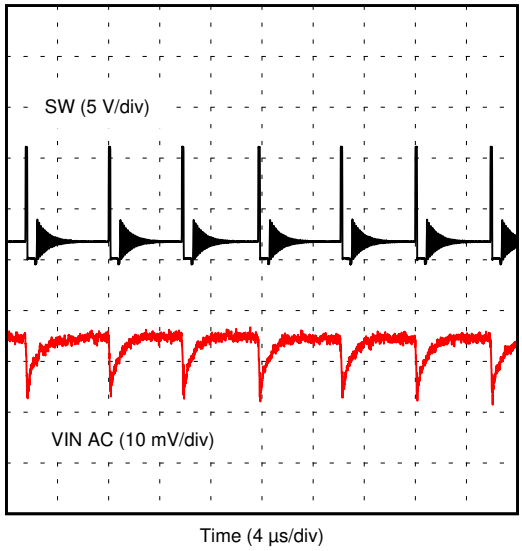

Figure 2-20. Input Ripple – DCM, 0.1-A Load

2.9 Powering Up and Down with EN

Figure 2-21 and Figure 2-22 show the start-up waveforms for the TPS54J060EVM-067 with V_{IN} = 12 V. The TPS54J061EVM-067 has similar behavior and the only difference is the soft-start time is shorter at 1.5 ms typical as a result of the lower 0.6-V reference. The start-up sequence begins as soon as the EN voltage is increased above the enable threshold voltage, and the output voltage ramps up to the set value.

Figure 2-23 shows the TPS54J060EVM-067 shutdown with V_{IN} = 12 V.

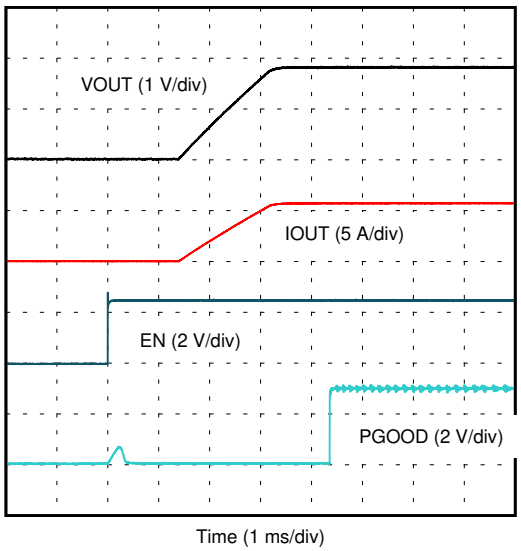

Figure 2-21. EN Start-up With 0.3-Ω Load

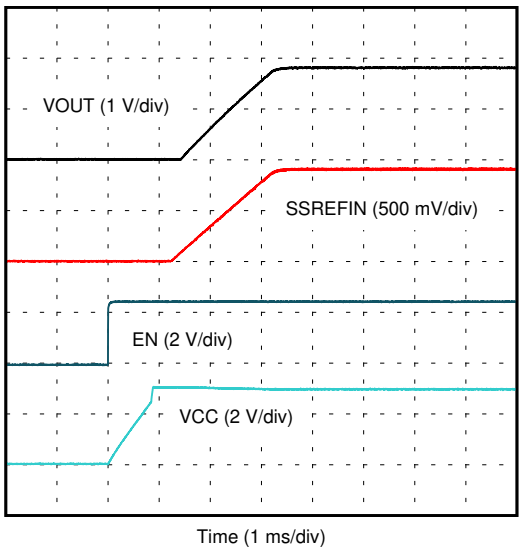

Figure 2-22. EN Start-up With 0.3-Ω Load, VCC and SSREFIN

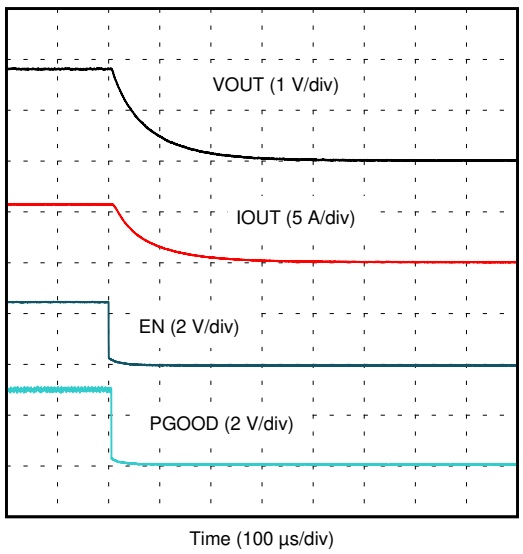

Figure 2-23. EN Shutdown With 0.3-Ω Load

2.10 Powering Up and Down With VIN

Figure 2-24 shows the start-up waveforms for the TPS54J060EVM-067 with V_{IN} ramping up to 12 V. The TPS54J061EVM-067 has similar behavior and the only difference is the soft-start time is shorter at 1.5 ms typical as a result of the lower 0.6-V reference. The start-up sequence begins as soon as the EN voltage is increased above the enable threshold voltage and the output voltage ramps up to the set value.

Figure 2-25 shows the TPS54J060EVM-067 shutdown with V_{IN} ramping down from 12 V.

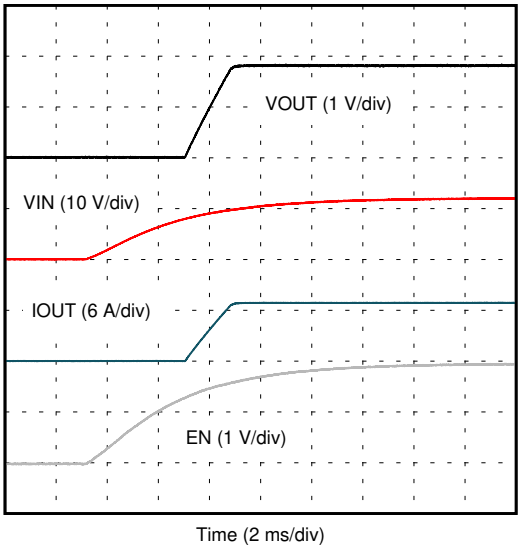

Figure 2-24. VIN Start-up With 0.3-Ω Load

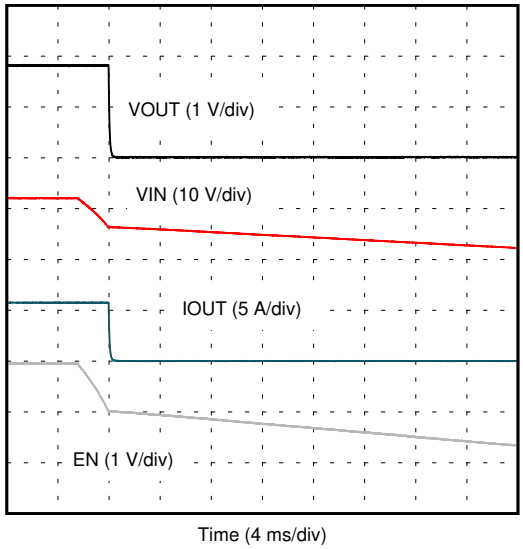

Figure 2-25. VIN Shutdown With 0.3-Ω Load

2.11 Start-Up Into Pre-Bias

Figure 2-26 shows the TPS54J060EVM-067 starting up into a pre-biased output. The TPS54J061EVM-067 has similar behavior and the only difference is the soft-start time is shorter as a result of the lower 0.6-V reference. The output voltage is pre-biased to 1 V by toggling the EN at ~30 Hz.

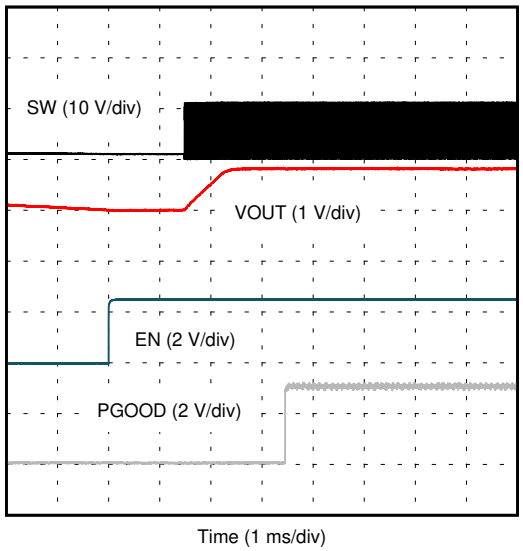

Figure 2-26. Start-up Into Pre-Biased Output With No Load

2.12 Current Limit

Figure 2-27 shows the latch off current limit of the TPS54J060EVM-067. The output current ramps up to a constant current of 7.5 A set by the electronic load and the output voltage begins to drop due to the valley current limit of the TPS54J060. When the output voltage drops below the under voltage protection threshold, the TPS54J060 latches off. As a result of the latch off protection, the output will only recover after pulling EN pin low then high or turning the input voltage off then on.

Figure 2-28 and Figure 2-29 shows the hiccup current limit of the TPS54J061EVM-067. When the output voltage drops below the UVP threshold, the TPS54J061 stops switching and after the hiccup timeout period attempts to restart. When the overload is removed the output of the TPS54J061 recovers.

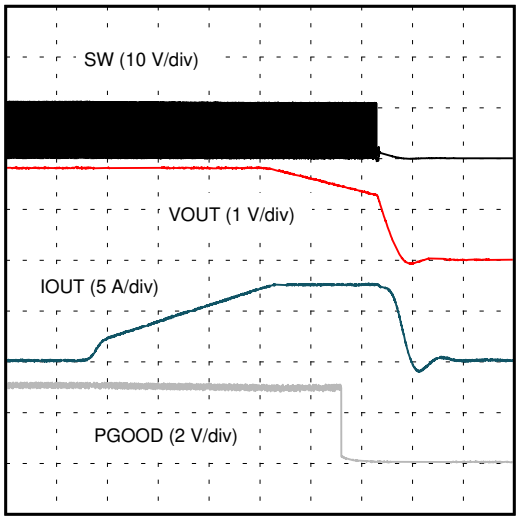

Figure 2-27. TPS54J060EVM-067 Latch Off Current Limit

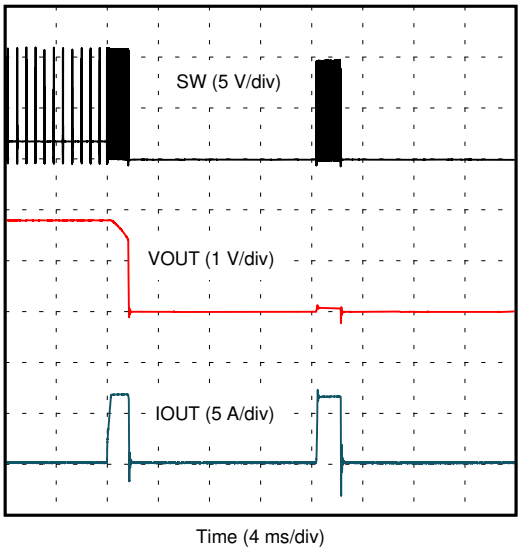

Figure 2-28. TPS54J061EVM-067 Entering Hiccup

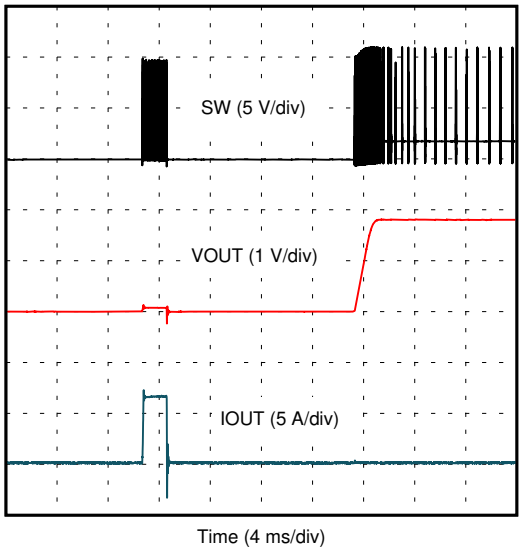

Figure 2-29. TPS54J061EVM-067 Recovering From Hiccup

3 Schematic, List of Materials, and Layout

This section provides the schematic, bill of materials and a description of the BSR067 board layout with layer illustrations.

3.1 Schematic

Figure 3-1 is the schematic for the TPS54J060EVM-067. Figure 3-2 is the schematic for the TPS54J061EVM-067.

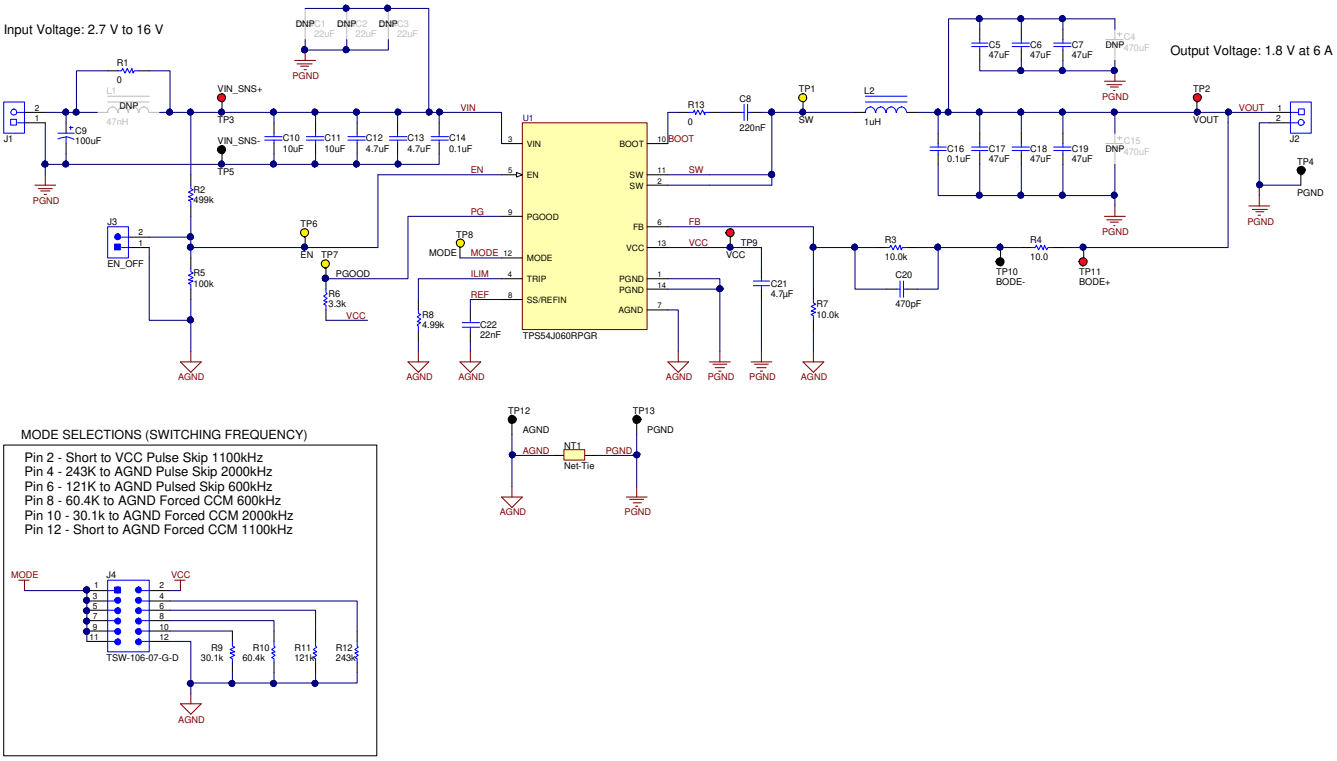

Figure 3-1. TPS54J060EVM-067 Schematic

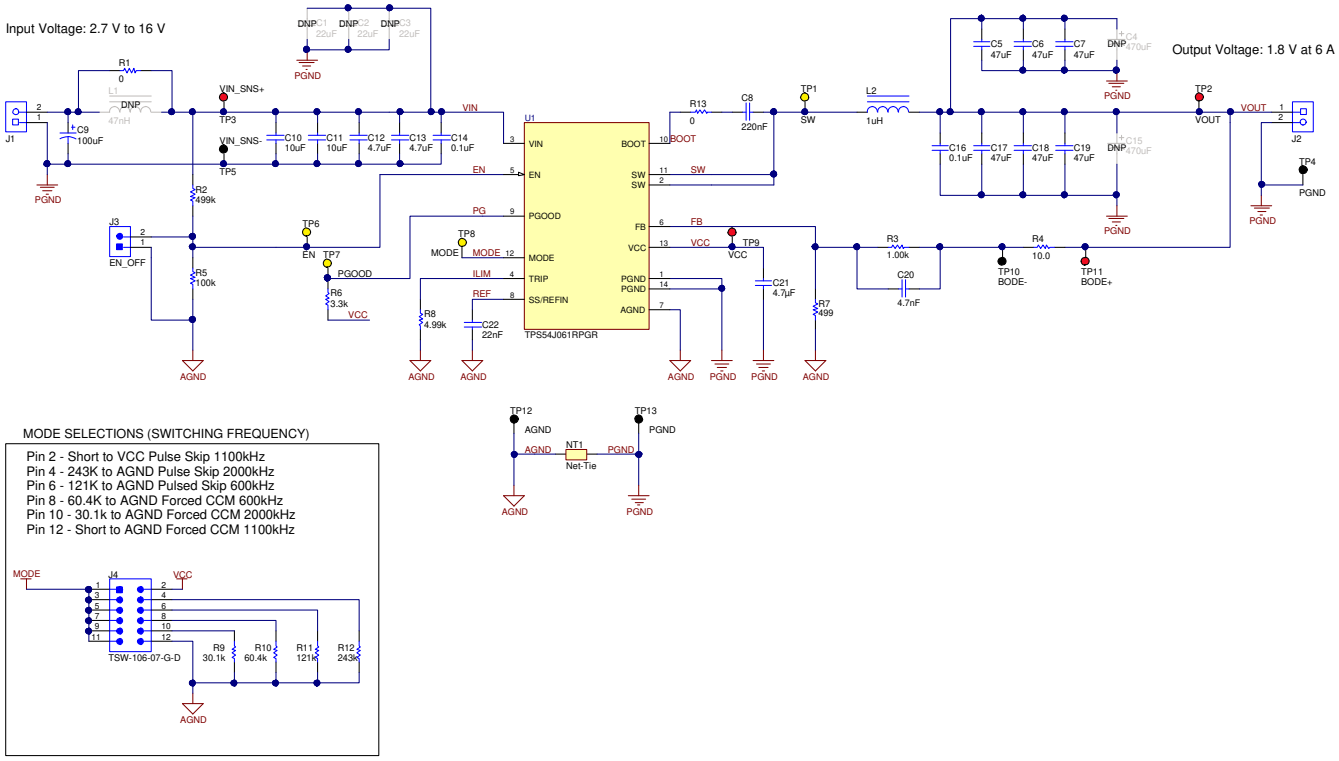

Figure 3-2. TPS54J061EVM-067 Schematic

3.2 List of Materials

Table 3-1 presents the list of materials for the TPS54J060EVM-067 and Table 3-2 presents the list of materials for the TPS54J061EVM-067.

Table 3-1. TPS54J060EVM-067 List of Materials

DES	QTY	DESCRIPTION	PARTNUMBER	MANUFACTURER
!PCB1	1	Printed Circuit Board	BSR067	Any
C5, C6, C7, C17, C18, C19	6	Capacitor ceramic, 47 µF, 6.3 V, ± 20%, X5R, 0805	GRM219R60J476ME44D	MuRata
C8	1	Capacitor ceramic, 0.22 µF, 25 V, ±10%, X7R, 0603	C1608X7R1E224K080AC	TDK
C9	1	CAP, AL, 100 uF, 35 V, ±20%, 0.16 ohm, AEC-Q200 Grade 2, SMD, SMT Radial F	EEE-FK1V101P	Panasonic
C10, C11	2	Capacitor ceramic, 10 µF, 25 V, ±10%, X7R, 1206	GRM31CR71E106KA12L	MuRata
C12, C13	2	Capacitor ceramic, 4.7 µF, 25 V, ±10%, X6S, 0603	GRM188C81E475KE11D	MuRata
C14	1	Capacitor ceramic, 0.1 µF, 25 V, ±20%, X7R, 0402	C1005X7R1E104M050BB	TDK
C16	1	Capacitor ceramic, 0.1 µF, 6.3 V, ±10%, X7R, 0402	GRM155R70J104KA01D	MuRata
C20	1	Capacitor ceramic, 470 pF, 50 V, ±10%, X7R, 0603	C0603C471K5RACTU	Kemet
C21	1	Capacitor ceramic, 4.7 µF, 6.3 V, ±10%, X7R, 0603	JMK107BB7475MA-T	Taiyo Yuden
C22	1	Capacitor ceramic, 0.022 µF, 25 V, ±10%, X7R, 0603	C0603C223K3RACTU	Kemet
H1, H2, H3, H4	4	Bumpon, transparent, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2x1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 100 mil, 2x1, gold, TH	TSW-102-07-G-S	Samtec
J4	1	Header, 100 mil, 6x2, gold, TH	TSW-106-07-G-D	Samtec
L2	1	Inductor, 1 µH, 14.4 A, 0.0064 ohm, SMD, 6.95x2.8x6.6mm	CMLE063T-1R0MS	Cyntec
LBL1	1	Thermal transfer printable labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
R1	1	Resistor, 0 Ω, 1%, 0.5 W, 1206	5108	Keystone
R2	1	Resistor, 499 kΩ, 1%, 0.1 W, 0603	RC0603FR-07499KL	Yageo
R3, R7	2	Resistor, 10.0 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
R4	1	Resistor, 10.0 Ω, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060310R0FKEA	Vishay-Dale
R5	1	Resistor, 100 kΩ, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
R6	1	Resistor, 3.3 kΩ, 5%, 0.1 W, 0603	RC0603JR-073K3L	Yageo
R8	1	Resistor, 4.99 kΩ, 1%, 0.1 W, 0603	RC0603FR-074K99L	Yageo
R9	1	Resistor, 30.1 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale
R10	1	Resistor, 60.4 kΩ, 1%, 0.1 W, 0603	RC0603FR-0760K4L	Yageo
R11	1	Resistor, 121 kΩ, 1%, 0.1 W, 0603	RC0603FR-07121KL	Yageo
R12	1	Resistor, 243 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603243KFKEA	Vishay-Dale
R13	1	Resistor, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GE0R00X	Panasonic
SH-JP1, SH-JP2	2	Shunt, 100mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP6, TP7, TP8	4	Test point, multipurpose, yellow, TH	5014	Keystone
TP2, TP3, TP9, TP11	4	Test point, multipurpose, red, TH	5010	Keystone
TP4, TP5, TP10, TP12, TP13	5	Test point, multipurpose, black, TH	5011	Keystone
U1	1	18-V single synchronous buck converter with adaptive on-time D-CAP3(TM) mode control, RPG0014A (VQFN-HR-14)	TPS54J060RPGR	Texas Instruments
C1, C2, C3	0	Capacitor ceramic, 22 µF, 25 V, ±10%, X7R, 1210	GRM32ER71E226KE15L	MuRata
C4, C15	0	Capacitor, tantalum polymer, 470 µF, 6.3 V, ±20%, 0.01 ohm, 7343-40 SMD	6TPF470MAH	Panasonic
FID1, FID2, FID3, FID4, FID5, FID6	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
L1	0	Inductor, wirewound, ceramic, 47 nH, 0.5 A, 0.31 Ω, SMD, 0805	0805CS-470XJLB	Coilcraft

Table 3-2. TPS54J061EVM-067 List of Materials

DES	QTY	DESCRIPTION	PARTNUMBER	MANUFACTURER
!PCB1	1	Printed Circuit Board	BSR067	Any
C5, C6, C7, C17, C18, C19	6	Capacitor ceramic, 47 µF, 6.3 V, ± 20%, X5R, 0805	GRM219R60J476ME44D	MuRata
C8	1	Capacitor ceramic, 0.22 µF, 25 V, ±10%, X7R, 0603	C1608X7R1E224K080AC	TDK
C9	1	CAP, AL, 100 uF, 35 V, ±20%, 0.16 ohm, AEC-Q200 Grade 2, SMD, SMT Radial F	EEE-FK1V101P	Panasonic
C10, C11	2	Capacitor ceramic, 10 µF, 25 V, ±10%, X7R, 1206	GRM31CR71E106KA12L	MuRata
C12, C13	2	Capacitor ceramic, 4.7 µF, 25 V, ±10%, X6S, 0603	GRM188C81E475KE11D	MuRata
C14	1	Capacitor ceramic, 0.1 µF, 25 V, ±20%, X7R, 0402	C1005X7R1E104M050BB	TDK
C16	1	Capacitor ceramic, 0.1 µF, 6.3 V, ±10%, X7R, 0402	GRM155R70J104KA01D	MuRata
C20	1	Capacitor ceramic, 4700 pF, 50 V, ± 10%, X7R, 0603	C0603C472K5RACTU	Kemet
C21	1	Capacitor ceramic, 4.7 µF, 6.3 V, ±10%, X7R, 0603	JMK107BB7475MA-T	Taiyo Yuden
C22	1	Capacitor ceramic, 0.022 µF, 25 V, ±10%, X7R, 0603	C0603C223K3RACTU	Kemet
H1, H2, H3, H4	4	Bumpon, transparent, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2x1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 100 mil, 2x1, gold, TH	TSW-102-07-G-S	Samtec
J4	1	Header, 100 mil, 6x2, gold, TH	TSW-106-07-G-D	Samtec
L2	1	Inductor, 1 µH, 14.4 A, 0.0064 ohm, SMD, 6.95x2.8x6.6mm	CMLE063T-1R0MS	Cyntec
LBL1	1	Thermal transfer printable labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
R1	1	Resistor, 0 Ω, 1%, 0.5 W, 1206	5108	Keystone
R2	1	Resistor, 499 kΩ, 1%, 0.1 W, 0603	RC0603FR-07499KL	Yageo
R3	1	Resistor, 1.00 k, 1%, 0.1 W, 0603	CRCW06031K00FKEA	Vishay-Dale
R4	1	Resistor, 10.0 Ω, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060310R0FKEA	Vishay-Dale
R5	1	Resistor, 100 kΩ, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
R6	1	Resistor, 3.3 kΩ, 5%, 0.1 W, 0603	RC0603JR-073K3L	Yageo
R7	1	Resistor, 499, 1%, 0.1 W, 0603	CRCW0603499RFKEA	Vishay-Dale
R8	1	Resistor, 4.99 kΩ, 1%, 0.1 W, 0603	RC0603FR-074K99L	Yageo
R9	1	Resistor, 30.1 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale
R10	1	Resistor, 60.4 kΩ, 1%, 0.1 W, 0603	RC0603FR-0760K4L	Yageo
R11	1	Resistor, 121 kΩ, 1%, 0.1 W, 0603	RC0603FR-07121KL	Yageo
R12	1	Resistor, 243 kΩ, 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603243KFKEA	Vishay-Dale
R13	1	Resistor, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GE0R00X	Panasonic
SH-JP1, SH-JP2	2	Shunt, 100mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP6, TP7, TP8	4	Test point, multipurpose, yellow, TH	5014	Keystone
TP2, TP3, TP9, TP11	4	Test point, multipurpose, red, TH	5010	Keystone
TP4, TP5, TP10, TP12, TP13	5	Test point, multipurpose, black, TH	5011	Keystone
U1	1	18-V single synchronous buck converter with adaptive on-time D-CAP3(TM) mode control, RPG0014A (VQFN-HR-14)	TPS54J061RPGR	Texas Instruments
C1, C2, C3	0	Capacitor ceramic, 22 µF, 25 V, ±10%, X7R, 1210	GRM32ER71E226KE15L	MuRata
C4, C15	0	Capacitor, tantalum polymer, 470 µF, 6.3 V, ±20%, 0.01 ohm, 7343-40 SMD	6TPF470MAH	Panasonic
FID1, FID2, FID3, FID4, FID5, FID6	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
L1	0	Inductor, wirewound, ceramic, 47 nH, 0.5 A, 0.31 Ω, SMD, 0805	0805CS-470XJLB	Coilcraft

3.3 Layout

The board layout for the BSR067 PCB is shown in Figure 3-3 through Figure 3-10. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and SW. Also on the top layer are connections for the remaining pins of the device and the majority of the signal traces. The top layer has a dedicated ground plane for quiet analog ground that is connected to the main power ground plane at a single point. Both internal planes contain a large ground plane. The bottom layer is another ground plane with two additional traces for the input and output voltage sense lines and various signals routed to test points and headers. There are also additional V_{IN} and V_{OUT} planes on the bottom layer. The top-side ground traces are connected to the bottom and internal ground planes with multiple via groupings placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. Critical analog circuits that are noise sensitive are terminated to the quiet analog ground island on the top layer.

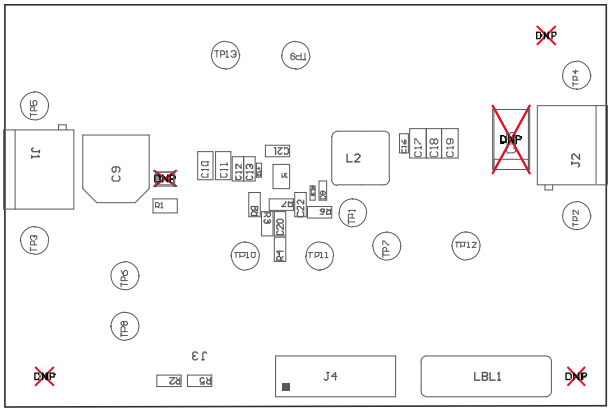

Figure 3-3. Top-Side Assembly

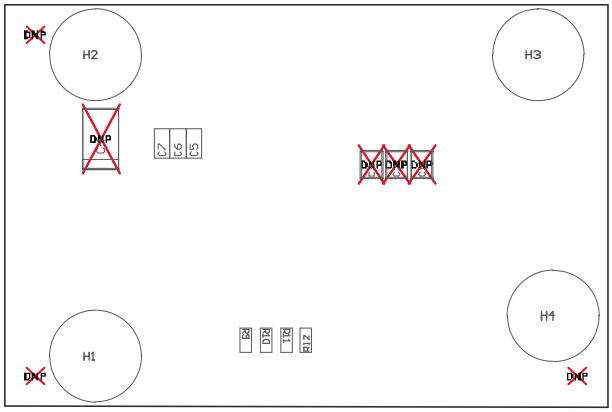

Figure 3-4. Bottom-Side Assembly (Viewed From Bottom)

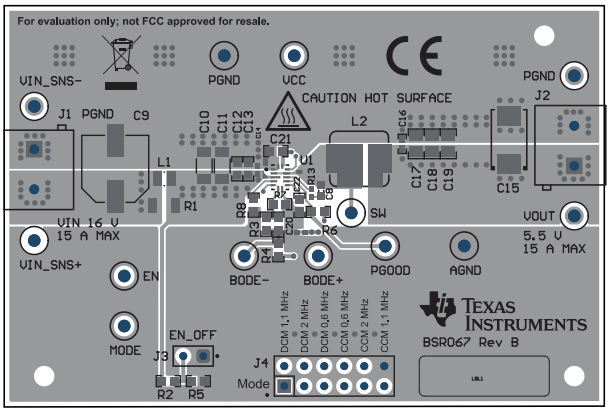

Figure 3-5. Top-Side Composite View

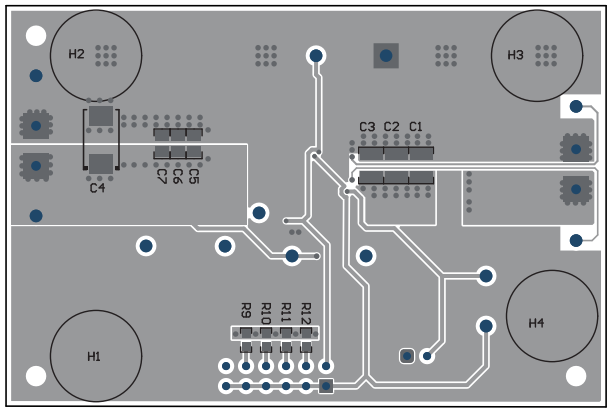

Figure 3-6. Bottom-Side Composite View (Viewed From Bottom)

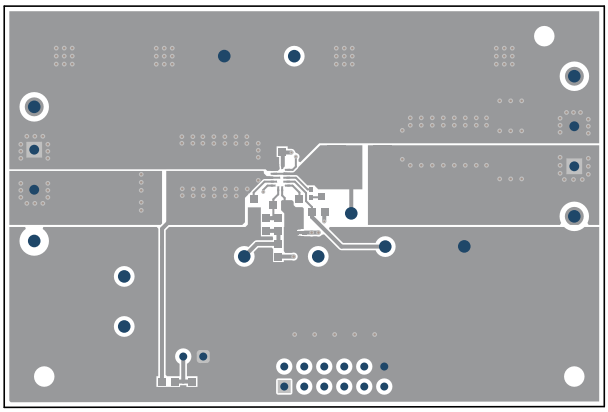

Figure 3-7. Top-Side Layout

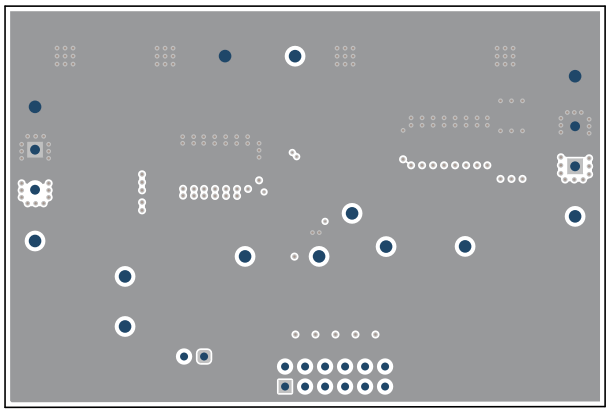

Figure 3-8. Internal Layer-1 Layout

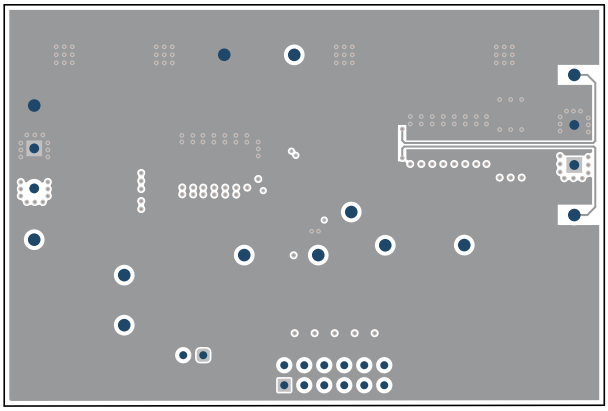

Figure 3-9. Internal Layer-2 Layout

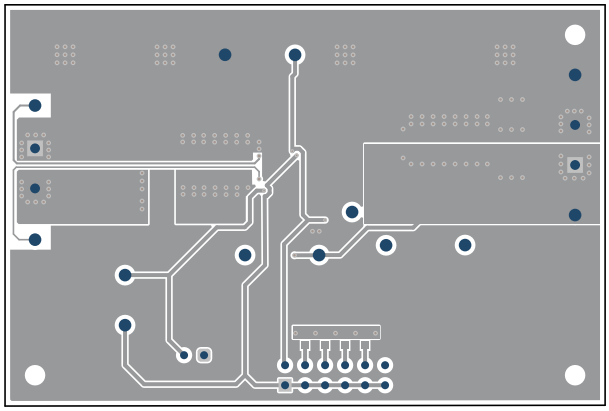

Figure 3-10. Bottom-Side Layout (Viewed From Top)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2020) to Revision B (May 2021)	Page
• Updated user's guide title	3

Changes from Revision * (March 2020) to Revision A (September 2020)	Page
• Added TPS54J061 throughout the document	3
• Added TPS54J061EVM-067 throughout the document	3
• Added TPS54J061 to Table 1-1	3
• Added TPS54J061 and added line in Table 1-2 for TPS54J061 soft-start time	4
• Changed text to include TPS54J061 considerations	5
• Changed TPS54J060 to device	5
• Changed Figure 2-1 through Figure 2-8 to match latest measurements	7
• Changed the title of Figure 2-17 from No Load to 0.1-A load	11
• Changed the title of Figure 2-20 from No Load to 0.1-A load	12
• Added paragraph describing TPS54J061 hiccup current limit, Figure 2-28 and Figure 2-29	15
• Changed TPS54J060EVM-067 to BSR067	16
• Updated Figure 3-1 to latest version with R13 and Added Figure 3-2 for the TPS54J061EVM-067	16
• Updated Table 3-1 to latest version with R13 and added Table 3-2 for the TPS54J061EVM-067	18
• Changed TPS54J060EVM-067 to BSR067. Changed Figure 3-3 to Figure 3-10 for added R13 in BSR067B layout	20

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