



ABSTRACT

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, LP875761ARNFRQ1.

1 Introduction

This technical reference manual can be used as a reference for the LP875761A-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the [LP875761-Q1 Four-Phase 3-MHz 1-V 16-A DC/DC Buck Converter With Integrated Switches data sheet](#).

[Table 1-1](#) lists the main OTP settings for power rails. [Table 2-1](#) lists the register bits loaded from OTP memory.

Table 1-1. Main OTP Settings for Power Rails

Description		Bit Name	LP875761ARNFRQ1 Value
Device identification	OTP configuration	OTP_ID	23h
BUCK0, BUCK1, BUCK2, BUCK3	Output voltage	N/A	1000 mV
	Enable, EN pin, or I ² C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	EN1
	Force PWM	N/A	Yes
	Force multiphase	N/A	Yes
	Peak current limit per phase	N/A	5 A
	Maximum load current	N/A	16 A
	Slew rate	N/A	3.8 mV/μs
Switching frequency		N/A	3 MHz
I ² C address		N/A	60h

Note

The maximum total output capacitance (local + POL) per phase (BUCK0, BUCK1, BUCK2, and BUCK3) depends on the slew rate setting. Check the data sheet for the allowed capacitance value.

2 Register Bits Loaded From OTP Memory

[Table 2-1](#) lists the register bit values loaded from the OTP memory during device start-up.

Table 2-1. Summary of Registers Bits

Address	Register Name	Bit	LP875761ARNFRQ1 Value
0x01	OTP_REV	OTP_ID[7:0]	23h
0x02	BUCK0_CTRL1	EN_BUCK0	1h
0x02	BUCK0_CTRL1	EN_PIN_CTRL0	1h
0x02	BUCK0_CTRL1	BUCK0_EN_PIN_SELECT[1:0]	0h
0x12	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	0h
0x12	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	0h

Table 2-1. Summary of Registers Bits (continued)

Address	Register Name	Bit	LP875761ARNFRQ1 Value
0x16	GPIO2_DELAY	GPIO2_SHUTDOWN_DELAY[3:0]	0h
0x16	GPIO2_DELAY	GPIO2_STARTUP_DELAY[3:0]	0h
0x17	GPIO3_DELAY	GPIO3_SHUTDOWN_DELAY[3:0]	0h
0x17	GPIO3_DELAY	GPIO3_STARTUP_DELAY[3:0]	0h
0x19	CONFIG	DOUBLE_DELAY	0h
0x19	CONFIG	CLKIN_PD	1h
0x19	CONFIG	EN3_PD	1h
0x19	CONFIG	TDIE_WARN_LEVEL	0h
0x19	CONFIG	EN2_PD	1h
0x19	CONFIG	EN1_PD	1h
0x21	TOP_MASK1	SYNC_CLK_MASK	1h
0x21	TOP_MASK1	TDIE_WARN_MASK	0h
0x21	TOP_MASK1	I_LOAD_READY_MASK	1h
0x22	TOP_MASK2	RESET_REG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK1_PG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK1_ILIM_MASK	1h
0x23	BUCK_0_1_MASK	BUCK0_PG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK0_ILIM_MASK	1h
0x24	BUCK_2_3_MASK	BUCK3_PG_MASK	1h
0x24	BUCK_2_3_MASK	BUCK3_ILIM_MASK	1h
0x24	BUCK_2_3_MASK	BUCK2_PG_MASK	1h
0x24	BUCK_2_3_MASK	BUCK2_ILIM_MASK	1h
0x28	PGOOD_CTRL1	PG3_SEL[1:0]	0h
0x28	PGOOD_CTRL1	PG2_SEL[1:0]	0h
0x28	PGOOD_CTRL1	PG1_SEL[1:0]	0h
0x28	PGOOD_CTRL1	PG0_SEL[1:0]	3h
0x29	PGOOD_CTRL2	HALF_DELAY	0h
0x29	PGOOD_CTRL2	EN_PG0_NINT	0h
0x29	PGOOD_CTRL2	PGOOD_SET_DELAY	0h
0x29	PGOOD_CTRL2	EN_PGFLT_STAT	0h
0x29	PGOOD_CTRL2	PGOOD_WINDOW	0h
0x29	PGOOD_CTRL2	PGOOD_OD	1h
0x29	PGOOD_CTRL2	PGOOD_POL	0h
0x2B	PLL_CTRL	PLL_MODE[1:0]	0h
0x2B	PLL_CTRL	EXT_CLK_FREQ[4:0]	1h
0x2C	PIN_FUNCTION	EN_SPREAD_SPEC	1h
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO3	1h
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO3	0h
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO2	1h
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO2	0h
0x2C	PIN_FUNCTION	GPIO3_SEL	0h
0x2C	PIN_FUNCTION	GPIO2_SEL	0h
0x2C	PIN_FUNCTION	GPIO1_SEL	0h
0x2D	GPIO_CONFIG	GPIO3_OD	1h
0x2D	GPIO_CONFIG	GPIO2_OD	1h
0x2D	GPIO_CONFIG	GPIO1_OD	1h
0x2D	GPIO_CONFIG	GPIO3_DIR	1h
0x2D	GPIO_CONFIG	GPIO2_DIR	1h
0x2D	GPIO_CONFIG	GPIO1_DIR	1h

Table 2-1. Summary of Registers Bits (continued)

Address	Register Name	Bit	LP875761ARNFRQ1 Value
0x2F	GPIO_OUT	GPIO3_OUT	0h
0x2F	GPIO_OUT	GPIO2_OUT	0h

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