User's Guide

TPS389006Q1EVM Multichannel Voltage Supervisor with I²C

ABSTRACT

This user's guide describes the operational use of the TPS389006Q1EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor. This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The TPS389006Q1EVM is an evaluation module (EVM) for the TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor. Test points are provided to give the user additional access, if needed, for oscilloscope or multi-meter measurements.

TPS389006Q1EVM comes with TPS389006004RTERQ1 pre-populated on pad U1 or depending on availability TPS389006Q1EVM can be fitted with socket J7 to house TPS389006004RTERQ1. This IC variant is configured for six integrated multichannel window inputs to monitor six distinct input voltage rails with two remote sense pins. The device also includes internal glitch immunity and noise filters to eliminate false resets resulting from erroneous signals. The TPS389006-Q1 device does not require any external resistors for setting overvoltage and undervoltage reset thresholds which optimizes and improves the reliability for safety systems.

I²C functionality gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. This device offers CRC error checking, sequence logging during turn ON or turn OFF, and a built-in ADC for voltage readouts to provide redundant error checking. In addition, TPS389006-Q1 offers a sync feature for tagging rails coming up. Rail tagging works across multiple instances of TPS389006-Q1 devices. If users need a different TPS389006-Q1 variant, the existing device must be removed from the board. The EVM board is designed to support all possible options by changing jumper configurations and is capable of daisy-chaining, through 10-pin ribbon, up to three evaluation boards.

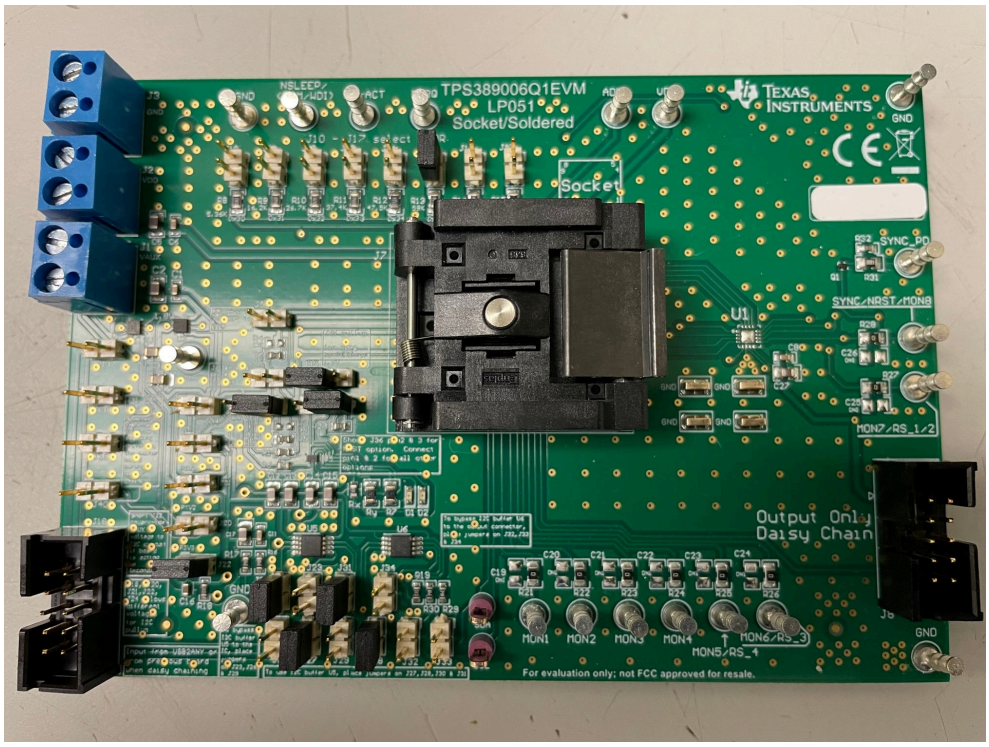

Figure 1-1. TPS389006Q1EVM Board Top

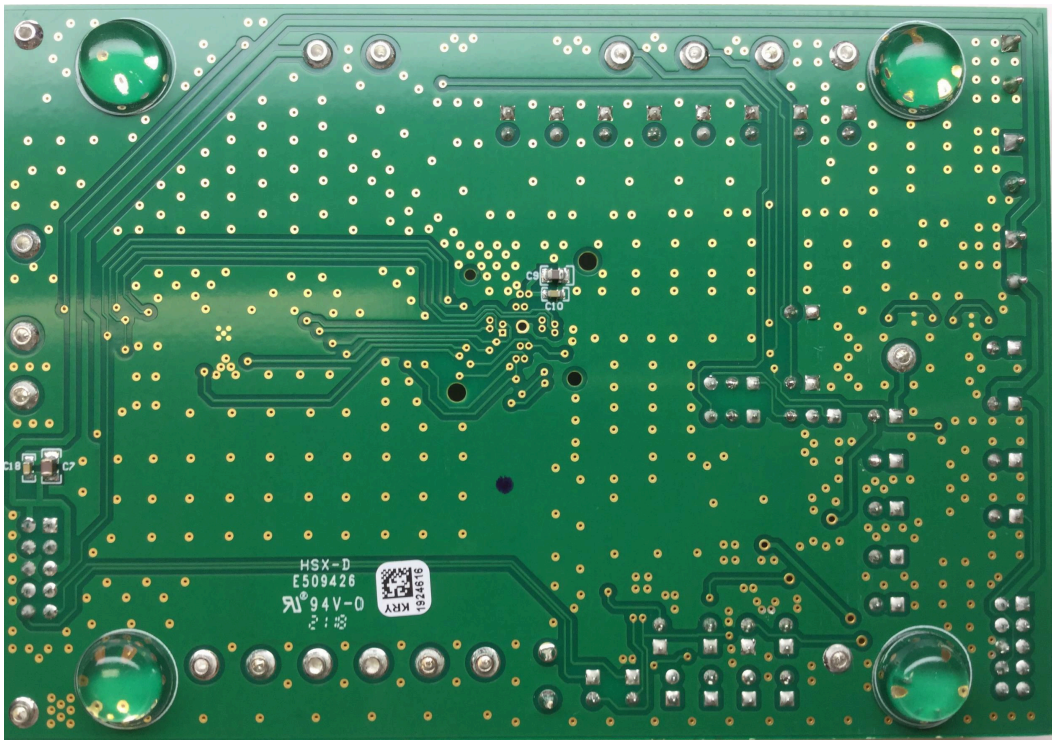

Figure 1-2. TPS389006Q1EVM Board Bottom

1.1 Related Documentation

Data sheet: *TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor*

1.2 TPS389006-Q1 Applications

- Advanced Driver Assistance System (ADAS)
- Sensor fusion
- Medical robotics
- Industrial robotics

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TPS389006Q1EVM schematic, bill of materials (BOM), and layout.

2.1 TPS389006Q1EVM Schematic

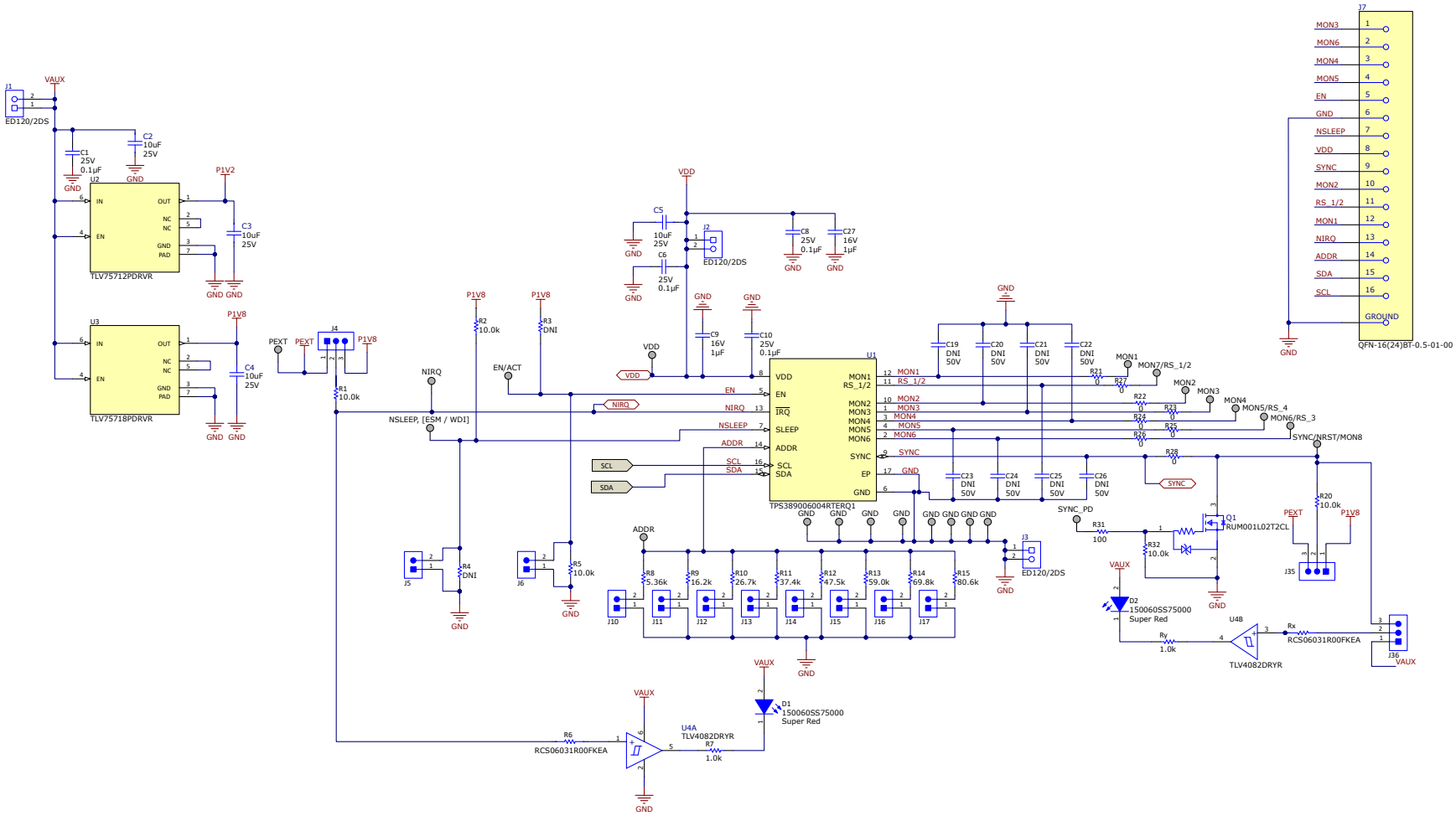

Figure 2-1. TPS389006Q1EVM Main Schematic

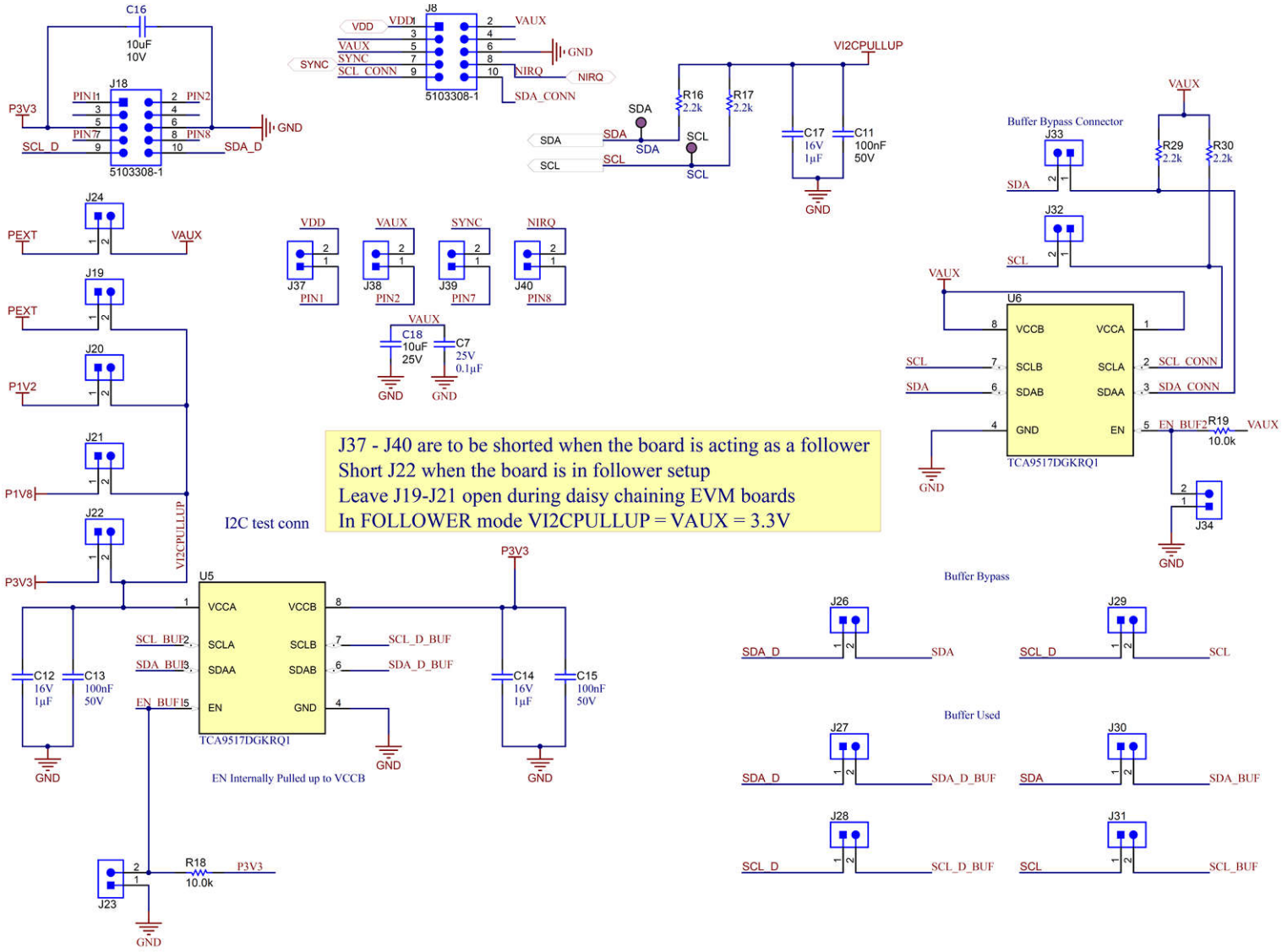

Figure 2-2. TPS389006Q1EVM I²C Schematic with Buffers

2.2 TPS389006Q1EVM Bill of Materials

Table 2-1. Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
PCB	1	LP051	Printed Circuit Board		TPS389006Q1EVM	Any
C1, C6, C7, C8, C10	5	0.1 µF	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X5R, 0603	0603	CL10A104KA8NNNC	Samsung Electro-Mechanics
C2, C3, C4, C5, C18	5	10 µF	10 µF ±10% 25 V Ceramic Capacitor X7S 0805 (2012 Metric)	0805	C2012X7S1E106K125AC	TDK
C9, C12, C14, C17, C27	5	1 µF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	0805	C0805C105K4RACAUTO	Kemet
C11	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX
C13, C15, C19(DNI), C20(DNI), C21(DNI), C22(DNI), C23(DNI), C24(DNI), C25(DNI), C26(DNI)	2	0.1 µF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0805 (C19 - C26 DO NOT POPULATE)	0805	C0805C104K5RACTU	Kemet
C16	1	10 µF	10 µF ±10% 10 V Ceramic Capacitor X5R 0603 (1608 Metric)	0603	C1608X5R1A106K080AC	TDK
D1, D2	2	Super Red	LED, Super Red, SMD	LED_0603	150060SS75000	Wurth Elektronik
EN/ACT, MON1, MON2, MON3, MON4, MON5/ RS_4, MON6/ RS_3, MON7, NIRQ, NSLEEP/, SYNC/NRST/ MON8, SYNC_PD, TP6a, TP6b, TP6c, TP6d, TP_ADDR, TP_EXT, VDD	19	Turret	Terminal, Turret, TH, Triple	Keystone 1598-2	1598-2	Keystone
GND1, GND2, GND3, GND4	4	Test Point (SMD)	Test Point, Miniature, SMT	Miniature, SMT	5019	Keystone
H1, H2, H3, H4	4	Bumpon Pad	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3	3	Terminal Block	Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J4, J35, J36	3	Header	Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J5, J6, J10, J11, J12, J13, J14, J15, J16, J17, J19, J20, J21, J22, J23, J24, J26, J27, J28, J29, J30, J31, J32, J33, J34, J37, J38, J39, J40	29	Header	Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J7	1(1)	Socket(1)	QFN CLAMSHELL 16 PIN RTE THRU HOLE WITH CENTER GND	16-Pin Socket	QFN-16(24)BT-0.5-01	Enplas
J8, J18	2	Shrouded Header	Header (shrouded), 100mil, 5x2, Gold, TH	5x2 Shrouded header	5103308-1	TE Connectivity

Table 2-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
Q1	1	MOSFET	MOSFET N-CH 20 V, 0.1 A, VMT3	SOT723	RUM001L02T2CL	ROHM Semiconductor
R1, R18, R19, R32	4	10 kΩ	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R2, R5, R20	3	10 kΩ	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	RCG060310K0FKEA	Vishay Draloric
R3(DNI)	0	10 kΩ	RES, DNP, 1%, 0.1 W, 0603 (DO NOT POPULATE)	0603	RCG060310K0FKEA	Vishay Draloric
R4(DNI)	0	21 kΩ	RES, DNP, 1%, 0.1 W, 0603 (DO NOT POPULATE)	0603	RC0603FR-0721KL	Yageo
R6, Rx	2	1 Ω	1 Ohms ±1% 0.25 W, ¼ W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	0603	RCS06031R00FKEA	Vishay
R7, Ry	2	1 kΩ	RES, 1.0 kΩ, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEYJ102V	Panasonic
R8	1	5.36 kΩ	RES, 5.36 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF5361V	Panasonic
R9	1	16.2 kΩ	RES, 16.2 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1622V	Panasonic
R10	1	26.7 kΩ	RES, 26.7 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF2672V	Panasonic
R11	1	37.4 kΩ	RES, 37.4 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF3742V	Panasonic
R12	1	47.5 kΩ	RES, 47.5 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF4752V	Panasonic
R13	1	59 kΩ	RES, 59 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF5902V	Panasonic
R14	1	69.8 kΩ	RES, 69.8 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF6982V	Panasonic
R15	1	80.6 kΩ	RES, 80.6 kΩ, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF8062V	Panasonic
R16, R17, R29, R30	4	2.2 kΩ	RES, 2.2 kΩ, 5%, 0.1 W, 0603	0603	RC0603JR-072K2L	Yageo
R21, R22, R23, R24, R25, R26, R27, R28	8	0 Ω	RES, 0 Ω, 5%, 0.125 W, 0805	0805	RC0805JR-070RL	Yageo
R31	1	100 Ω	RES, 100 Ω, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEYJ101V	Panasonic
SCL, SDA	2	Test Points	Test Point, Multipurpose, Purple, TH	Purple Multipurpose Testpoint	5129	Keystone
U1	0	IC	ASIL-D Multichannel Overvoltage and Undervoltage I2C Programmable Voltage Supervisor and Monitor	WQFN16	TPS389006004RTERQ1	TI
U2	1	IC	1 A Low-Quiescent-Current Low-Dropout (LDO) Regulator, 1.2 V, DRV0006A (WSON-6)	WSON-6	TLV75712PDRVR	TI
U3	1	IC	1 A Low-Quiescent-Current Low-Dropout (LDO) Regulator, 1.8 V,DRV0006A (WSON-6)	WSON-6	TLV75718PDRVR	TI
U4	1	IC	Dual-Channel, Low-Power Comparator with Integrated Reference	SON6	TLV4082DRYR	TI
U5, U6	2	IC	Automotive, Level-Shifting I^2C Bus Repeater, DGK0008A (VSSOP-8)	VSSOP-8 (DGK0008A)	TCA9517DGKRQ1	TI

Table 2-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

(1) Dependent on availability, if J7 is not available the U1 device is installed on the U1 pad.

2.3 Layout and Component Placement

Figure 2-3 and Figure 2-4 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 2-5 and Figure 2-6 show the top and bottom layouts, Figure 2-7 and Figure 2-8 show the top and bottom layers, and Figure 2-9 and Figure 2-10 shows the top and bottom solder masks of the EVM.

2.4 Layout

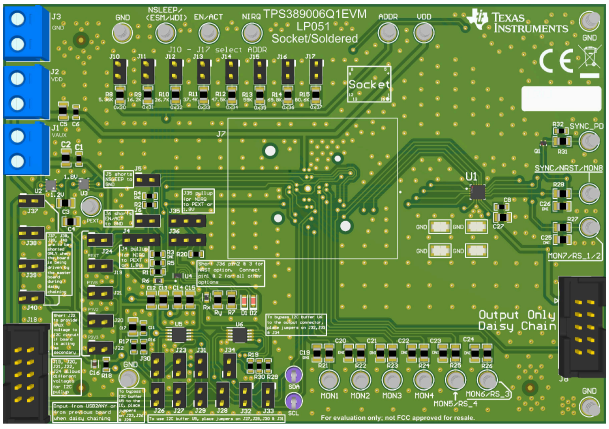

Figure 2-3. Component Placement—Top Assembly

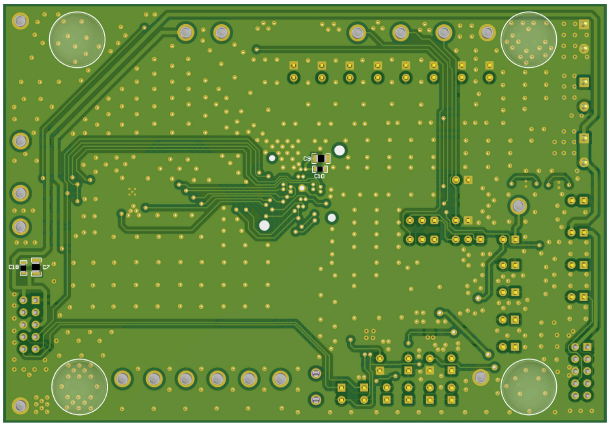

Figure 2-4. Component Placement—Bottom Assembly

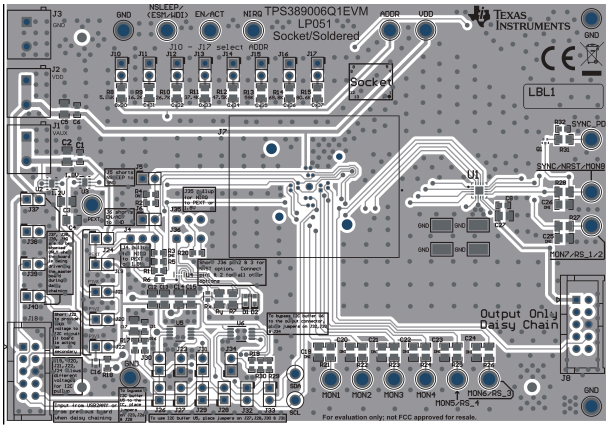

Figure 2-5. Layout—Top

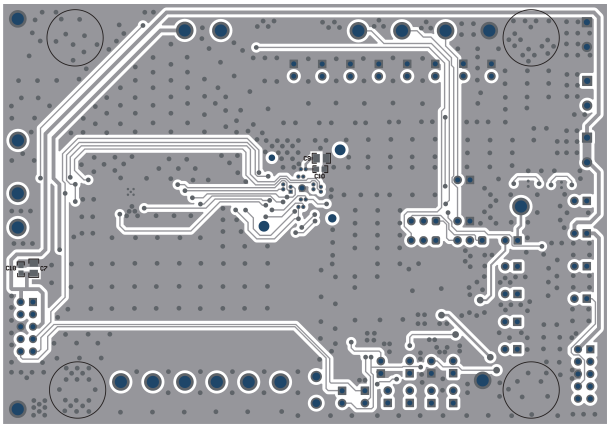

Figure 2-6. Layout—Bottom

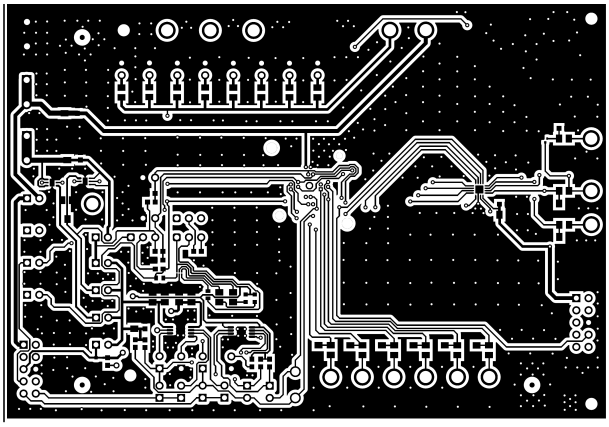

Figure 2-7. Top Layer

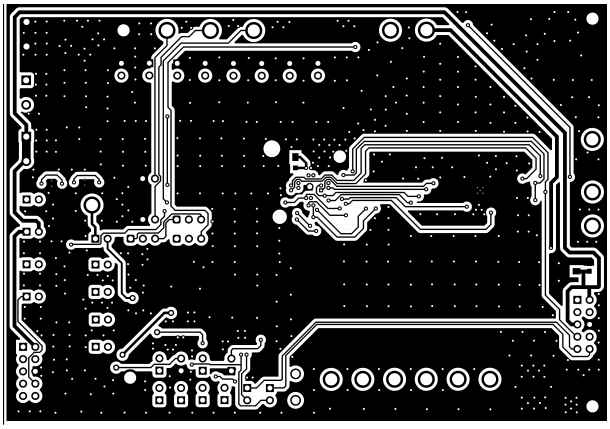

Figure 2-8. Bottom Layer

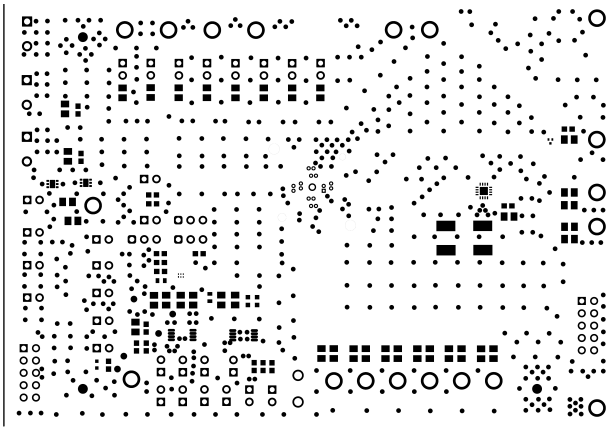

Figure 2-9. Top Solder Mask

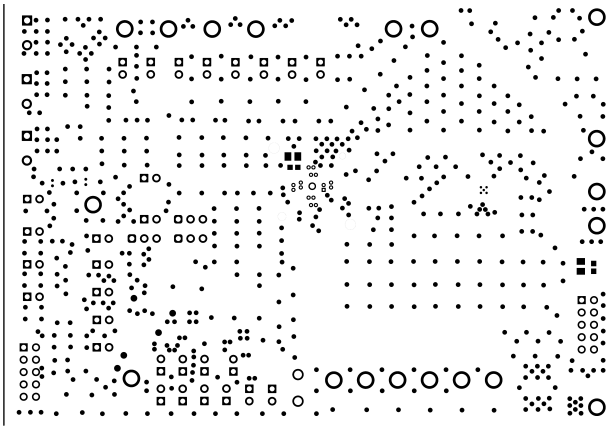

Figure 2-10. Bottom Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the EVM test points as well as their functional descriptions. All TPS389006-Q1 pins have a corresponding test point on the EVM. These test points are located close to the pins for more accurate measurements. In addition to the test points listed below, the EVM also has four additional GND test points.

Table 3-1. Test Points

TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
MON1	Connection to MON1 pin	Allows the user to monitor voltage rail #1
MON2	Connection to MON2 pin	Allows the user to monitor voltage rail #2
MON3	Connection to MON3 pin	Allows the user to monitor voltage rail #3
MON4	Connection to MON4 pin	Allows the user to monitor voltage rail #4
MON5/RS_4	Connection to MON5 pin	Allows the user to monitor voltage rail #5
MON6/RS_3	Connection to MON6 pin	Allows the user to monitor voltage rail #6
MON7/RS_1/2	Connection to RS_1/2 pin	Allows the user to remote sense MON1 or MON2
SYNC/NRST/MON8	Connection to SYNC pin	SYNC pin indicates the number of monitored rails that have exited fault status and assigns tag values to each monitor voltage rail
SYNC_PD	Connection to SYNC_PD	Forcing the SYNC pin to toggle during test and increments an internal tag counter for each of the monitored channel (for debug purposes only)
ADDR	Connection to ADDR pin	Allows the user to measure the I^2C address voltage
NIRQ	Connection to NIRQ pin	Allows the user to monitor the interrupt (NIRQ) output
EN/ACT	Connection to ACT pin	Allows the user to set the ACT input to VDD or GND
$\overline{\text{SLEEP}}$/ESM/WDI	Connection to $\overline{\text{SLEEP}}$ pin	Allows the user to set $\overline{\text{SLEEP}}$ input
SCL	Connection to SCL pin	Allows the user to monitor the clock signal input
SDA	Connection to SDA pin	Allows the user to monitor the data signal input
PEXT	External power supply	Allows the user to apply a power supply voltage that is not provided from the EVM
GND	GND for EVM	GND for EVM

3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TPS389006Q1EVM. As ordered, the EVM has thirty-five (35) jumpers installed. Figure 3-1 is provided as visual aid.

Table 3-2. List of On-board Jumpers

JUMPER	JUMPER CONFIGUATION	DESCRIPTION
J1	VAUX	For connecting VAUX power to the EVM
J2	VDD	For connecting VDD power to the EVM
J3	GND	For connecting GND to the EVM
J4	Shunted (default) Pin 2 to Pin 3	For connecting ACT, NIRQ, and $\overline{\text{SLEEP}}$ to P1V8 or PEXT (Any external power)
J5 and J6	Open	For manually pulling down $\overline{\text{SLEEP}}$ and ACT pins to GND
J10, J11, J12, J13, J14, J15, J16, and J17	J15 shunted	Shunting any one of J10-J17 jumpers selects the I^2C address for TPS389006-Q1 IC on the EVM
J19, J20, and J21	Open	For connecting to the on-board I^2C buffer and pull-up voltage rail to either P1V8, PEXT or P1V2. Only shunt one of these jumpers at a time. Please remove the shunt of J22 when using one of these jumpers.
J22	Shunt	For connecting to the on-board, buffer I^2C and pull-up voltage rail to P3V3. During *daisy-chain* configuration, J22 needs to be shunted and J19, J20, and J21 needs to be open on the secondary EVMs.
J23	Shunted	Disables (U5) I^2C buffer
J24	Open	Connects PEXT to VAUX
J26 and J29	Shunted	Shunting both J26 and J29 bypasses the I^2C (U5) buffer for SDA and SCL signal lines
J27, J28, J30, and J31	Open	Shunting these jumpers buffers SCL and SDA I^2C signal lines by using the on-board (U5) buffer.
J32 and J33	Shunted	Shunting both J32 and J33 bypasses the I^2C (U6) buffer for SDA and SCL signal lines
J34	Shunted	Disables (U6) I^2C buffer
J35	Shunted (default) Pin 1 to Pin 2	SYNC pin is pulled up to P1V8
J36	Shunted (default) Pin 2 to Pin 3	Input to one of (U4) comparators to indicate the SYNC pin has *tagged* a voltage rail that is not in a fault condition
J37, J38, J39, J40	Open	If multiple EVMs are connected in a *daisy-chain* configuration, then the following EVM boards needs to have J37, J38, J39, and J40 all shunted. By shunting these jumpers, VDD, VAUX, SYNC, and NIRQ signals is provided as inputs from the primary EVM board. Also, J22 needs to be shunted and J19, J20, and J21 needs to be open on the secondary EVMs during *daisy-chain* configuration.

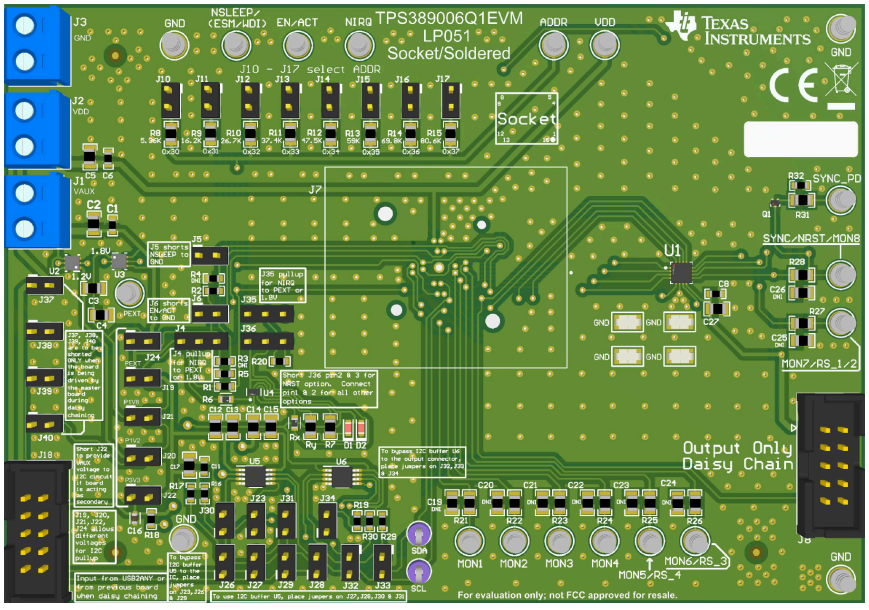

Figure 3-1. TPS389006Q1EVM Jumper Locations

4 EVM Setup and Operation

This section describes the functionality and operation of the TPS389006Q1EVM. Refer to the TPS389006-Q1 Multichannel Overvoltage and Undervoltage I^{2}C Programmable Voltage Supervisor and Monitor data sheet for details on the electrical characteristics of the device.

The TPS389006Q1EVM comes with the TPS389006004RTERQ1 IC meaning the device is capable of monitoring up to six separate voltage rails. The EVM is capable of many different configurations to fully evaluate the functionality of all the TPS389006-Q1 device variants. The default jumper configuration of the TPS389006Q1EVM is mentioned in Table 3-2.

The TPS389006Q1EVM comes with USB to GPIO connector, I^{2}C bus repeaters, comparators, two LDOs, socket and solder down footprints, the ability to monitor up to eight (8) voltage rails, the option to daisy-chain up to three EVMs at a time via 10-pin connector, jumper selectable I^{2}C address, I^{2}C pullup voltage options, and TPS389006004RTERQ1 IC. The TPS389006Q1EVM also provides the ability for each monitored rail to be voltage divided down by resistor dividers on each of the monitored and input lines. The user must choose appropriately sized resistors such that the divided voltage is above, below or within the window of the voltage threshold depending on the type of input sensing topology is setup for each monitored input channel. Consult the Device Threshold Table in the TPS389006-Q1 data sheet to verify proper voltage monitored values.

The TPS389006Q1EVM is designed to be daisy-chain where the primary board is connected to the USB to GPIO connector (J18) and the output connector (J8) provides VDD, VAUX, SYNC, SCL, SDA, NIRQ, and GND to the (J18) connector of the secondary board through a 10-pin ribbon cable. When the daisy-chain option is being used, jumpers on the secondary board (J19-J22 and J37-J40) must be configured properly or else possible damage to the IC or EVM can occur. Jumper settings of J19, J20, and J21 must be left open whereas J22, J37, J38, J39, and J40 need to be shunted with jumpers for proper setup of the secondary board during daisy-chain setup. Also, the I^{2}C rail voltage for the secondary board in the daisy-chain mode is defined as VI2CPULLUP = VAUX = 3.3 V. See Figure 2-2 for reference.

Equipment Needed for TPS389006Q1EVM Evaluation:

- TPS389006Q1EVM
- TI's USB Interface Adapter (with ribbon cable)
- Power Supply (3.3 V)
- Multimeters
- Multi-channel Oscilloscope (review evaluation waveforms)
- Jumper Wires/Cables

4.1 Setup and GUI Installations

4.1.1 TPS389006Q1EVM Hardware Setup

Follow the steps below for TPS389006Q1EVM hardware setup:

1. Connect VAUX (J1) and VDD (J2) to 3.3 V from the power supply.
2. Connect GND (J3) to ground from the power supply.
3. Make sure the jumpers are connected as per the guidelines in the Table 3-2.
4. Before allowing the output of the power supply to be engaged, check if the power supply voltage is set at 3.3 V and the power supply output current is limited to 10 mA.
5. Connect the TI's USB Interface Adapter to J18 (USB2GPIO Connector) using a 10-pin ribbon cable.
6. Connect the TI's USB Interface Adapter to the computer's USB port.
7. Connect any voltage supply rail that needs monitoring to any of the voltage monitoring inputs (MON1 - MON8).
8. The description of the TPS389006Q1EVM connections can be found in Figure 4-1.

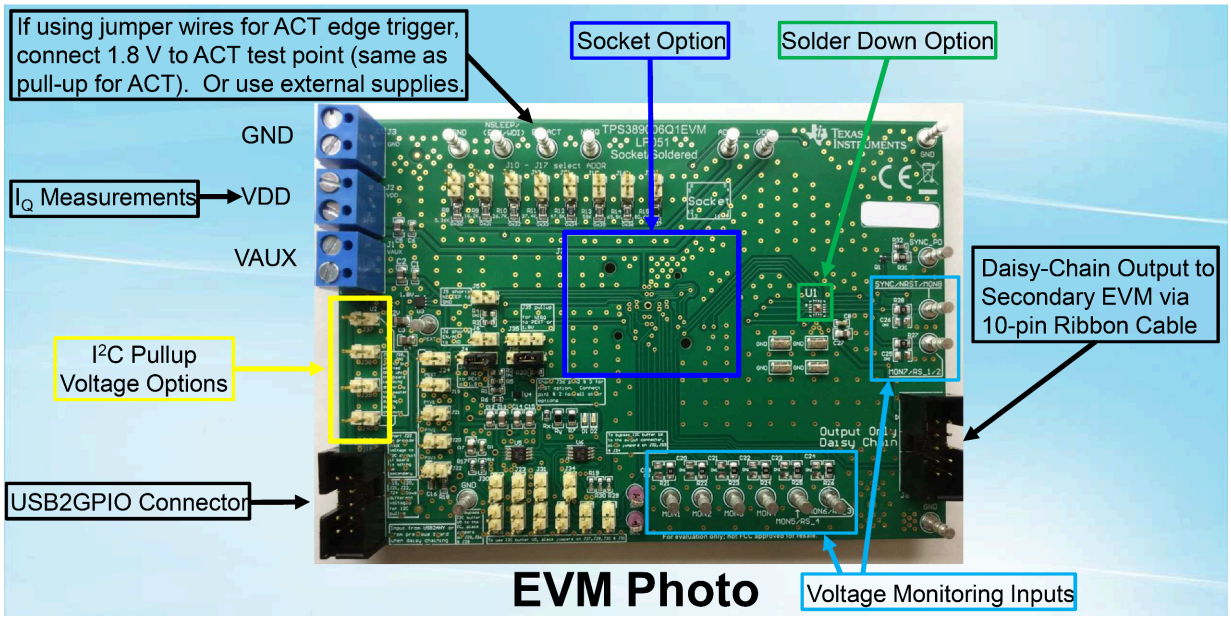

Figure 4-1. TPS389006Q1EVM Connection Description

4.1.2 TPS389006Q1EVM Software Setup

Follow the steps below for TPS389006Q1EVM GUI software installation:

1. Download the Fusion Digital Power Designer Platform GUI for TPS389006Q1EVM.
2. Open the downloaded file.
3. In the Welcome Wizard window, click *Next*.
4. Accept the license agreement and then click *Next*.

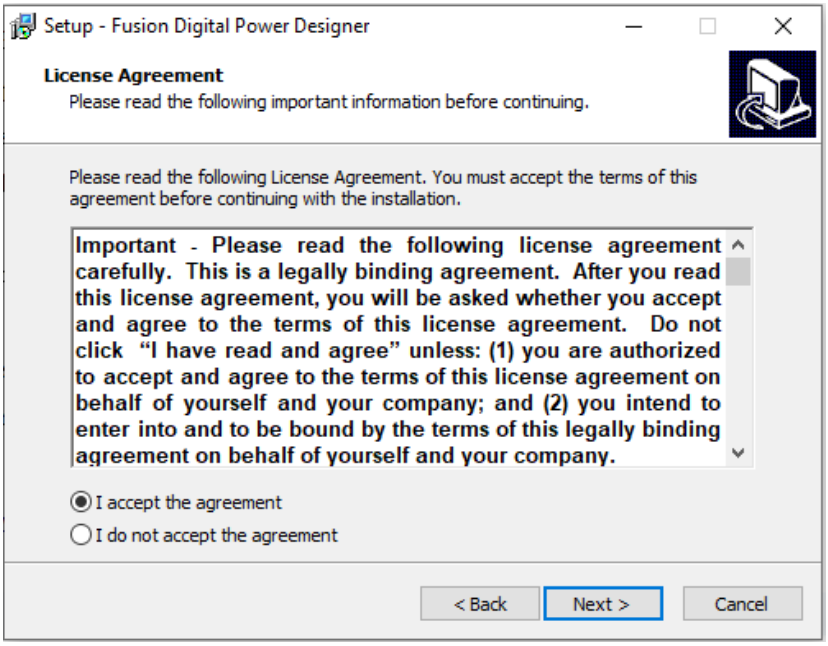

Figure 4-2. Setup License Agreement Window

5. The default destination folder works best. Click *Next*.

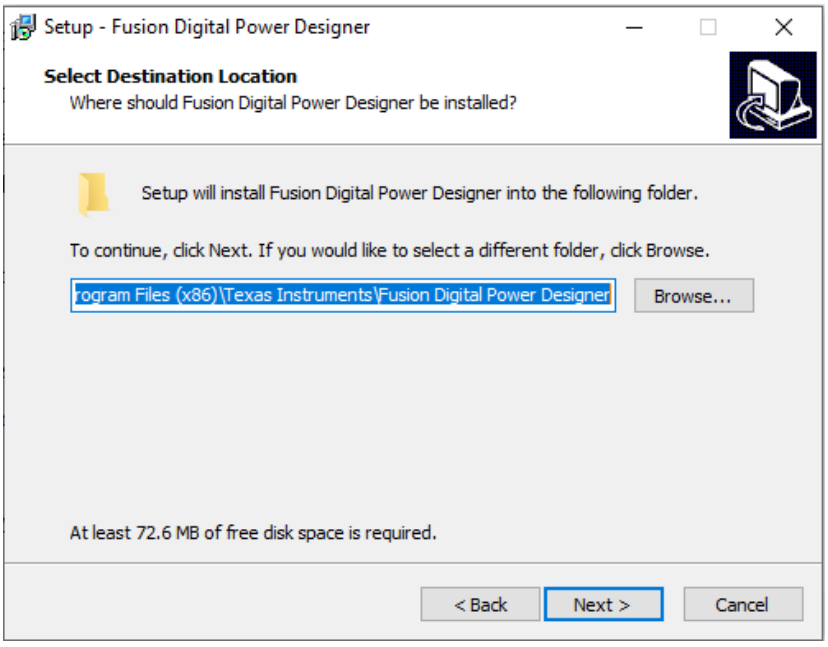

Figure 4-3. Setup Destination Window

6. Click *Next* for the Select Start Menu Folder option.

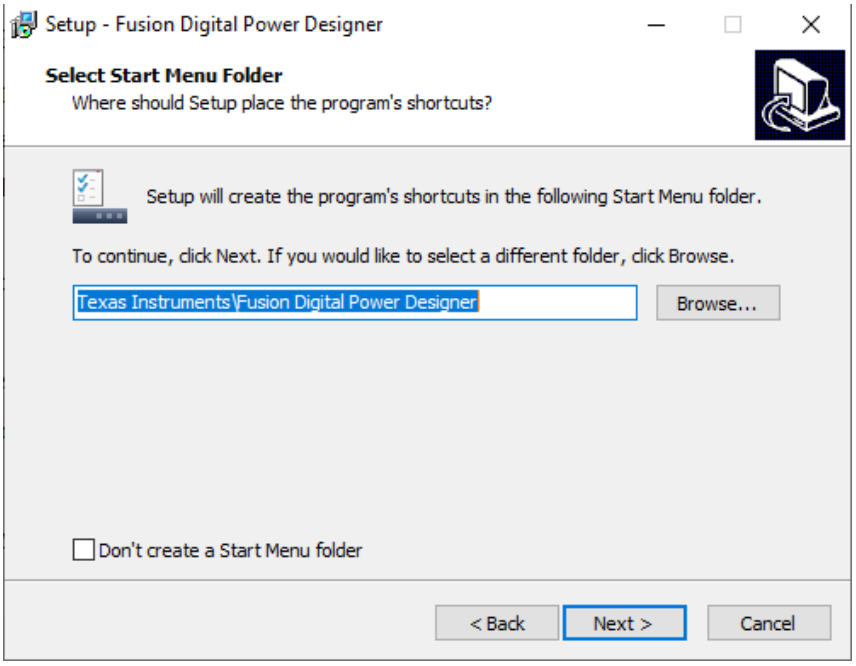

Figure 4-4. Setup Window - Start Menu Selection

7. There is no need to install additional options for this EVM. Click *Next*.

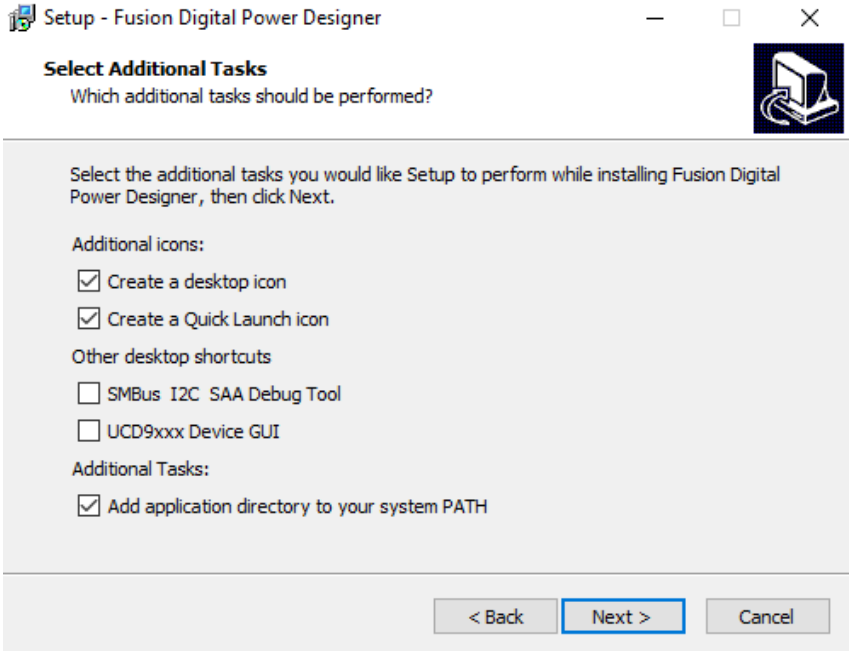

Figure 4-5. Setup Window - Additional Tasks

8. Finally click *Install* to install the Fusion software.

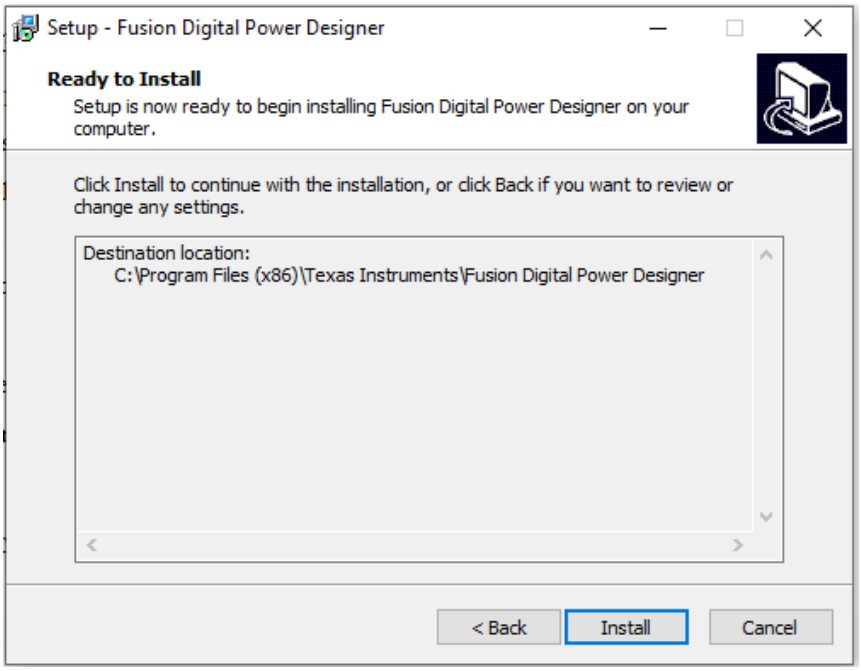

Figure 4-6. Setup Installation Window

9. Click on *Finish* to complete the installation setup and launch the software.

Figure 4-7. Installation Complete Window

4.2 Quick Start to TPS389006Q1EVM GUI

Please follow the steps below precisely to quickly evaluate the TPS389006-Q1. In this quick start, the TPS389006Q1EVM is set up to monitor several power supply rails after the ACT pin is triggered.

1. Make the hardware connections and software installation described in Section 4.1 have been completed. Feel free to skip the GUI installation if the *Fusion Digital Power Designer* for TPS389006Q1EVM GUI has been installed already.
2. Power the EVM by turning on the power supply. Note that the voltage and current limits at the power supply is set at 3.3 V and 10 mA.
3. Once the TI's USB Interface Adapter is connected to EVM and the laptop, launch the evaluation software *Fusion Digital Power Designer*.
4. Click on *I2C GUI* on the bottom right of GUI.

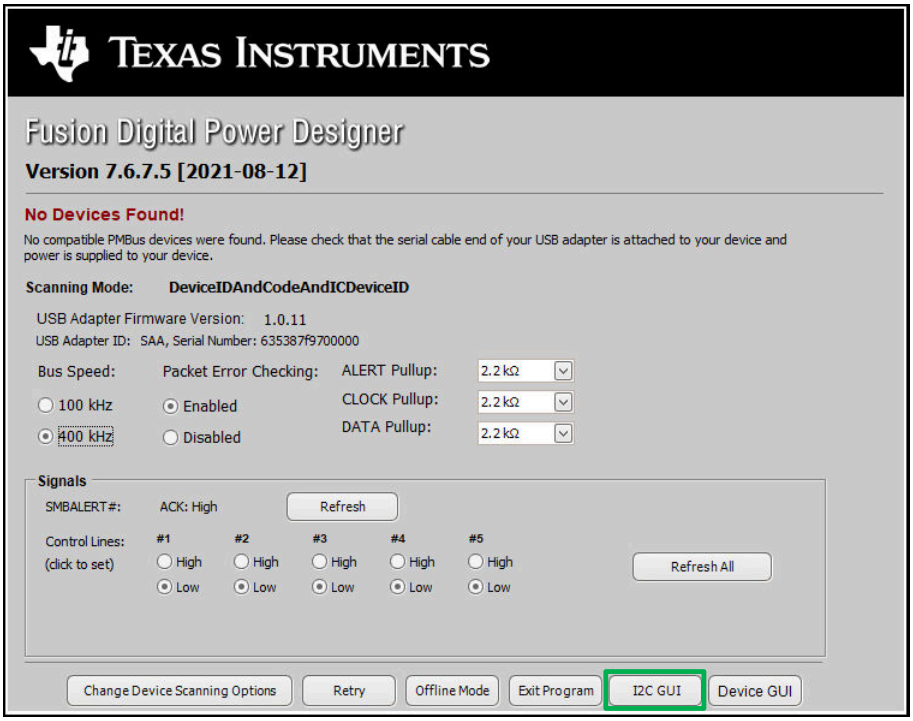

Figure 4-8. Fusion Welcome Window

5. Click on *Change Scan Mode* to select *TPS389xxx* and then click *OK*.

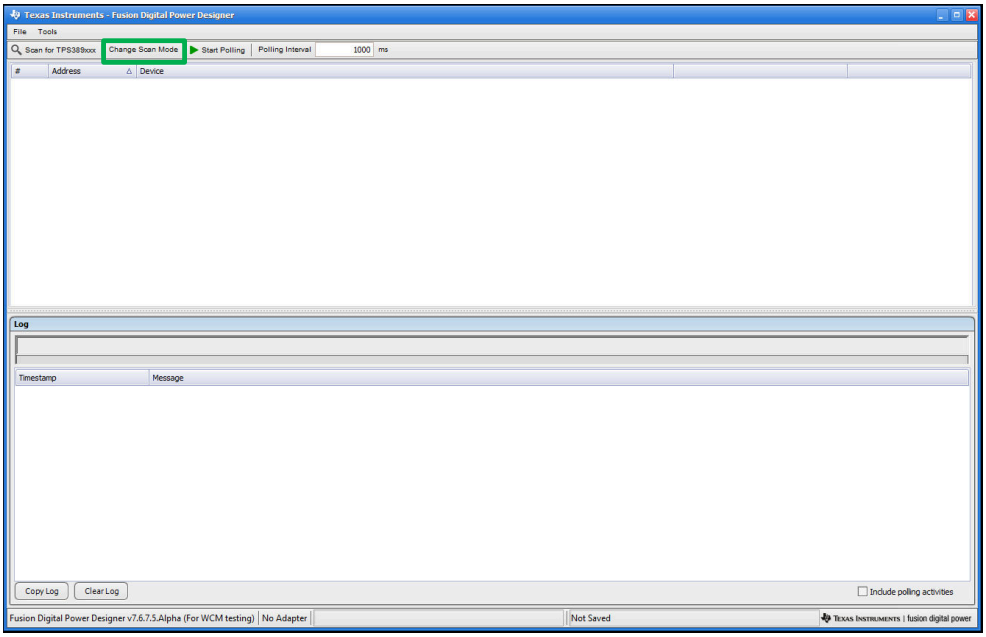

Figure 4-9. Fusion Scan Window

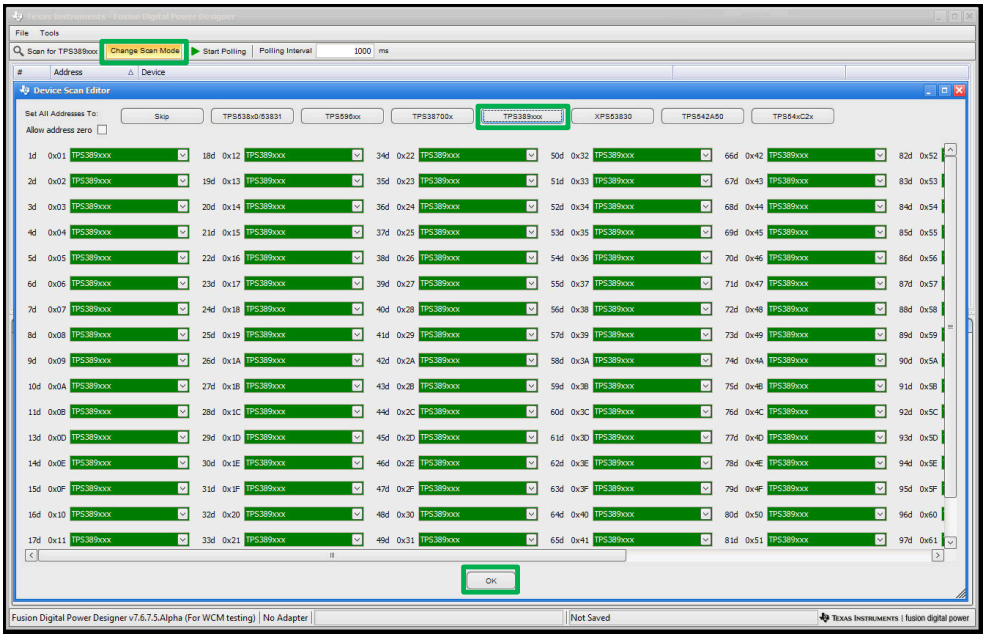

Figure 4-10. Fusion Scan Selection Window

6. Scan for the TPS389006Q1EVM by clicking on *Scan for TPS389xxx* on top left of the window.

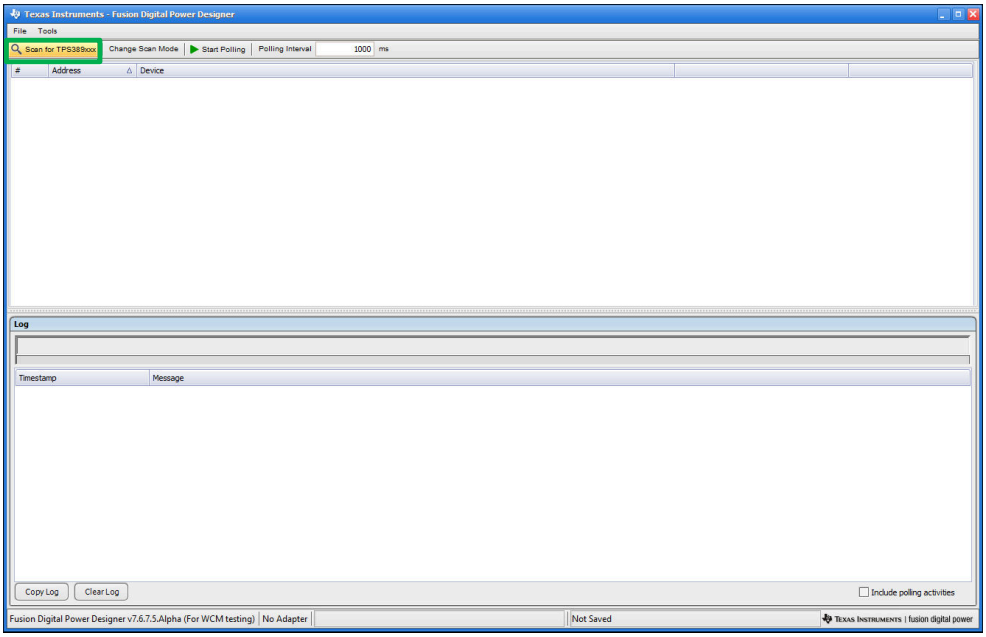

Figure 4-11. Fusion Scan Window - Scanning for TPS389006Q1EVM

7. Once the EVM is discovered, select *Click to Configure*.

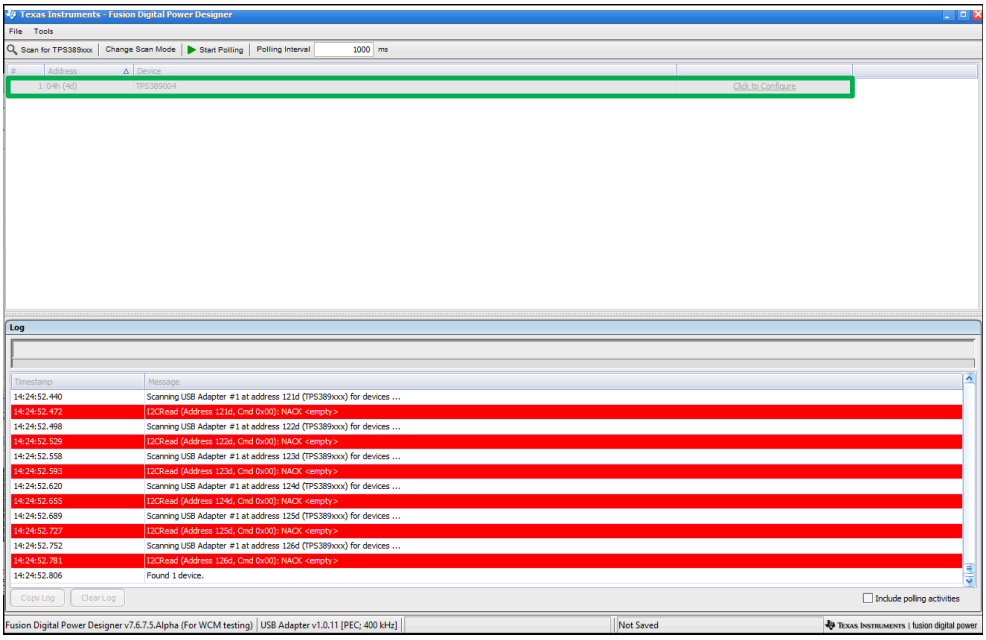

Figure 4-12. Fusion Scan Window - Scan for TPS389006Q1EVM Completed

8. Once the *Click to Configure* box has been selected, the Fusion Digital Power Device GUI for the TPS389006-Q1 appears as shown below. The GUI image shows the *General Config*, *Sequencing*, *Clear/Reset*, *Telmetry*, and Polling (Plotting the monitored voltage rails) sub-windows.

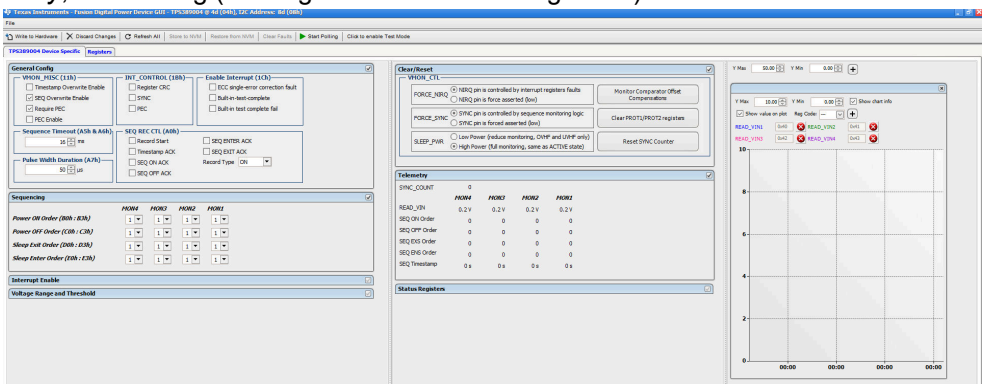

Figure 4-13. Fusion Digital Power Device GUI - TPS389006Q1EVM (Image #1)

9. The GUI image below continues to show the additional sub-windows that are in the GUI for the TPS389006-Q1. The GUI image includes the *Interrupt Enable*, *Voltage Range and Threshold*, *Status Registers*, and Polling (plotting the monitored voltage rails) sub-windows.

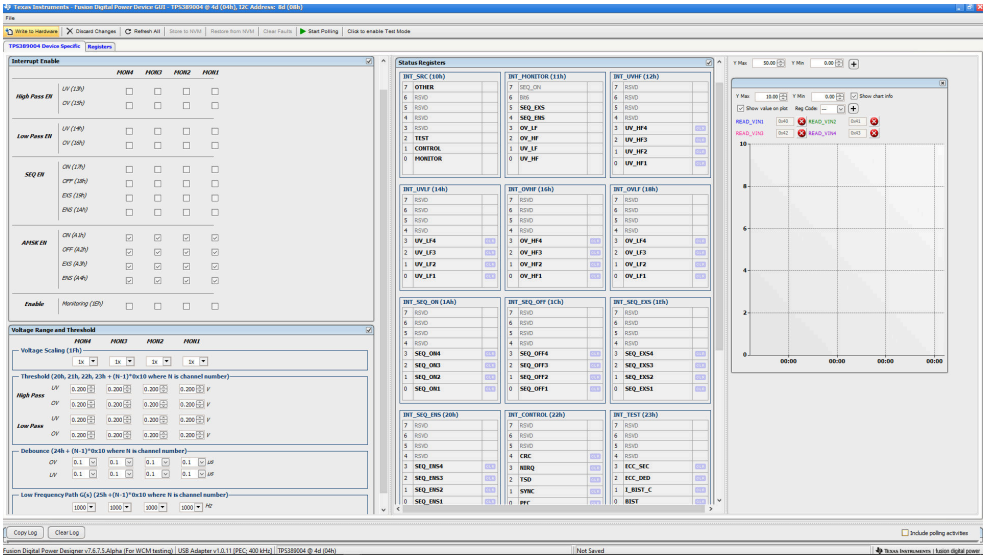

Figure 4-14. Fusion Digital Power Device GUI - TPS389006Q1EVM (Image #2)

10. The last GUI image below shows the last five registers in the *Status Registers* sub-window.

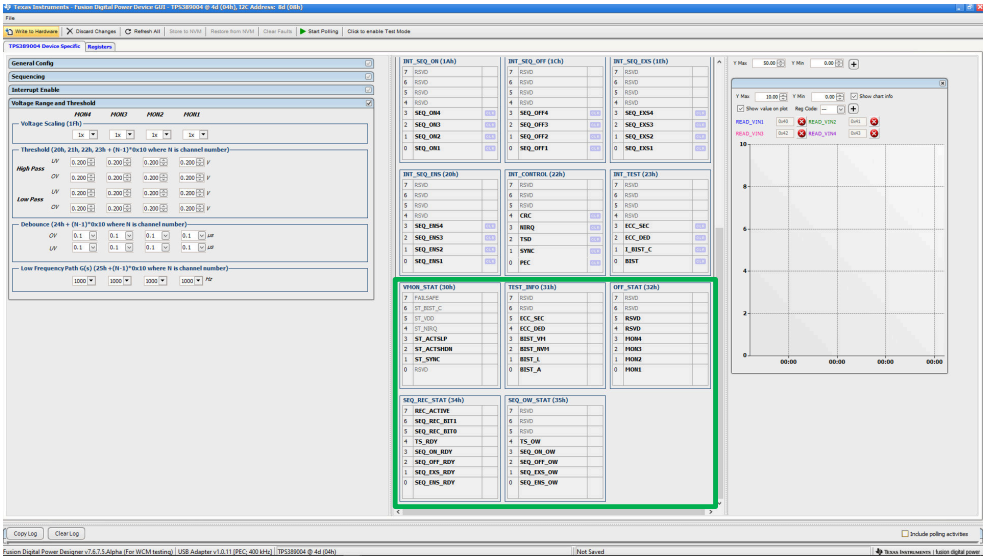

Figure 4-15. Fusion Digital Power Device GUI - TPS389006Q1EVM (Image #3)

4.3 Example Operation of TPS389xxx-Q1

The example below shows a TPS389004-Q1 monitoring four voltage supply rails on the TPS389006Q1EVM. Please follow the steps in Section 4.1.1 and Section 4.1.2 before evaluating the TPS389004-Q1. In this example, the TPS389006Q1EVM is set up to monitor several power supply rails after the ACT pin is asserted. Below, Figure 4-16 shows how the TPS389006Q1EVM was setup to monitor four voltage supply rails.

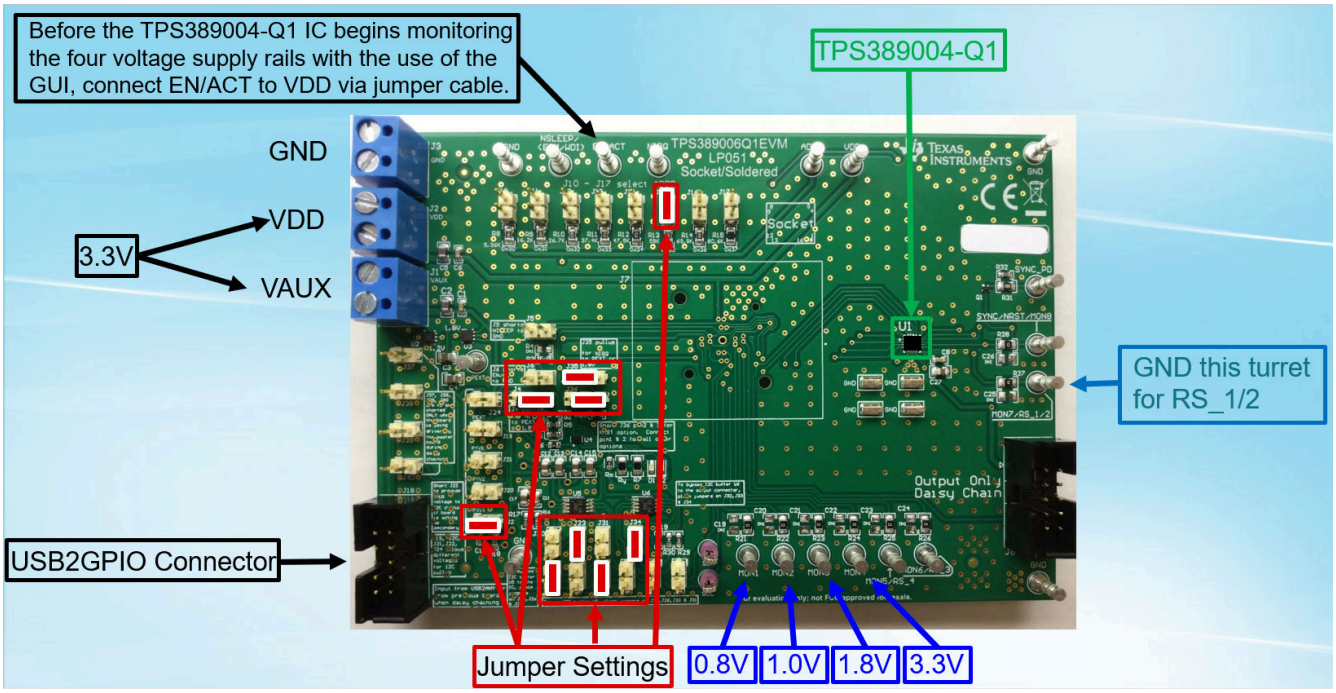

Figure 4-16. TPS389006Q1EVM Monitoring Four Voltage Supply Rails

1. Connect the TPS389006Q1EVM VDD and VAUX inputs to a 3.3 V external power supply. Note that the voltage and current limits of the power supply must be set at 3.3 V and 10 mA.
2. Connect the TPS389006Q1EVM with TI's USB Interface Adapter ribbon to J18 (USB2GPIO connector). Connect the USB plug from the USB Interface Adapter to the USB port of the computer. The TI USB Interface Adapter communicates to the TPS389004-Q1 IC via I^2C protocols.
3. Verify that the jumper settings, highlighted in red in Figure 4-16, are set on the TPS389006Q1EVM.
4. Ground turret *(MON7/RS_1/2)*.
5. Apply 0.8 V to MON1, 1.0 V to MON2, 1.8 V to MON3, 3.3 V to MON4 to the turrets of TPS389006Q1EVM.
6. Final Connections must look similar to Figure 4-16.
7. Open up the Fusion Digital Power Designer GUI on the computer and follow Section 4.2.
8. Once the EVM is discovered and *Click to Configure* has been selected, the GUI is similar to Figure 4-13, Figure 4-14, Figure 4-15.
9. Scroll to the bottom of the *Interrupt Enable* sub-window and enable all four monitoring inputs by clicking the empty boxes. The GUI image, Figure 4-17 below, shows all the monitoring inputs being selected in the highlighted "black-box".
10. In the *Voltage Range and Threshold* sub-window, enter the undervoltage (UV) and overvoltage (OV) threshold values for the monitoring inputs. One thing to note, any monitoring inputs that are higher than 1.5 V needs to select *4x* in the *Voltage Scaling (1Fh)* field. The GUI image below, highlighted by a *yellow-box*, shows is described above.
11. Once steps 9 and 10 are completed, press *Write to Hardware* and the USB Interface Adapter communicates to the TPS389004-Q1 IC. Next, press *Start Polling* and both the Telemetry (shown in the highlighted orange-box) and the graphical waveform of the monitored inputs (shown in the highlighted red-box) is shown in the GUI.
12. If one of the monitored inputs senses a fault, then an interrupt indicator is displayed (illumination of a red LED) on the TPS389006Q1EVM. Also, one of the bit registers found in the *Status Registers* sub-window, highlighted in the green-box, also shows a fault in red color.

13. To clear the fault interrupt, press *Stop Polling*, go to the *Status Registers* sub-window, locate the red color fault interrupt and click on *CLR*. Then click on *Write to Hardware*. This procedure clears the fault interrupt and allows the device to continue to monitor the input channels.
14. Steps 8 through 13 refers to Figure 4-17 below.

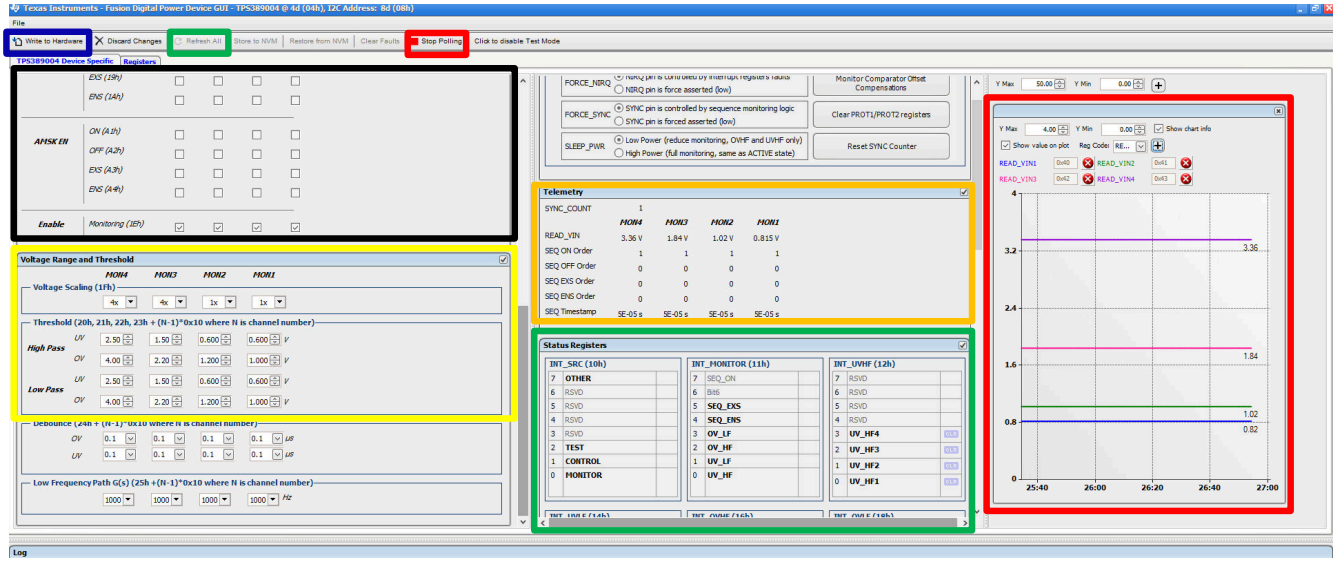

Figure 4-17. TPS389006Q1EVM GUI Setup for Monitoring Four Voltage Supply Rails

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2023) to Revision B (August 2023)	Page
• Changed the OPN to TPS389006004RTERQ1 from TPS389006Q1 in Section 1	3
• Added statement clarifying the availability of socket J7 in Section 1	3
• Added table note to clarify availability of J7	8
• Changed the OPN to TPS389006004RTERQ1 from TPS389006Q1 in Section 4	15

Changes from Revision * (February 2022) to Revision A (May 2023)	Page
• Changed the OPN to TPS389006004RTERQ1 from TPS389006Q1 in *TPS389006Q1EVM Main Schematic*	6
• Changed the OPN to TPS389006004RTERQ1 from TPS389006Q1 in *Bill of Materials* table	8

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